Use of WNx as diffusion barrier for copper airbridged low noise GaAs PHEMT

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A low noise pseudomorphic high electron mobility transistor (PHEMT) with copper airbridges using sputtered WNx as the diffusion barrier has been developed. Both the material system and the copper airbridged PHEMT with WNx as the diffusion barrier did not decay even after thermal annealing at 250°C for 20 h. The results show that the copper airbridges with WNx diffusion barrier can be used as the interconnects for low noise GaAs PHEMTs.

Introduction: The copper metallisation process has become increasingly popular in the silicon integrated circuit industry ever since IBM scientists announced a new advance in the semiconductor process of copper metallisation in September 1997 [1–3]. However, only a few studies of the copper metallisation process on GaAs devices have been reported, and Ta and TaN were used as the diffusion barriers in these papers [4–6]. In this Letter, we use WNx as the diffusion barrier between Cu and GaAs which was successfully applied to the Cu metallisation of the airbridge interconnects of the AlGaAs/InGaAs low noise pseudomorphic high electron mobility transistors (LN-PHEMTs).

Traditionally, plated gold was used for airbridges on GaAs devices, including metal-semiconductor field-effect transistors (MESFETs) and high electron mobility transistors (HEMTs). Plated gold has high electrical conductivity, is resistant to oxidation and is ductile. However, gold is expensive, which causes the high cost for the GaAs device fabrication. In this work, copper replaces gold as the material used for the airbridges in the GaAs PHEMTs and WNx was used as the diffusion barrier. The goal is to find a reliable diffusion barrier for copper metallisation of GaAs devices in order to reduce the production cost of the GaAs devices and to provide better thermal and electrical conductivities for the interconnects. Copper airbridges were formed by electroplating 2.5 µm copper on the thin layers of the sputtered Cu seed layer and the WNx barrier layer on the gold-contacted PHEMTs. The fabricated low noise PHEMTs with copper airbridges were thermally annealed in order to evaluate the thermal stability of WNx as the barrier between copper and underlying gold-based contacts.

Experiment: The low noise PHEMTs were grown by molecular beam epitaxy (MBE) on a 3-inch (1 0 0) oriented semi-insulating GaAs substrate. The epilayers of the device, from the bottom to the top, are composed of a 600 nm buffer, a 15 nm InGaAs channel, a 2 nm undoped AlGaAs spacer, a 42 nm Si-doped AlGaAs donor layer and a 45 nm Si-doped GaAs capping layer.

After mesa isolation, the source and drain ohmic metals (Au/Ge/Ni/Au) were deposited and formed by rapid thermal annealing at 410°C for 20 s. T-shaped Ti/Pt/Au gates were fabricated by electron beam direct writer and lift-off process. The gate length was 0.25 µm. A passivation film of silicon nitride was deposited on the device by plasma enhanced chemical vapour deposition (PECVD) process at a substrate temperature of 250°C. The nitride via was plasma-etched by CF_4/O_2 gases.

The photo resist thickness of the first airbridge layer determines the spacing between the bridge and the materials beneath. Hence, the thickness of the selected resist in this layer should be thick enough to reduce the parasitic coupling effect during high frequency operation. In this study, the thickness of the two airbridge resist layers was up to 2.6 µm. After hard baking of the resists, the thin film layers, including the diffusion barrier and the Cu seed layer, were subsequently sputtered on the wafer. The 40 nm-thick sputtered WNx was used as the diffusion barrier between the copper and the underlying gold-based contacts and the 100 nm-thick sputtered copper was used as the seed layer to conduct electrical currents for electroplating. The second photo process of the airbridges process masked the areas beyond the plating area and 2.2 µm-thick copper was electroplated on the sputtered Cu layer. Copper airbridges were formed after the unplated areas of the Cu/WNx layers and the resists were removed. The fabricated LN-PHEMTs with copper airbridges were then furnace annealed at 250°C for 20 h in the atmosphere of nitrogen. The device characteristics before and after thermal annealing were compared to evaluate the thermal stability of the WNx barrier in the low noise PHEMT fabricated with copper-metallised airbridges. As judged from the data of Auger electron spectroscopy (AES), the WNx film between gold-contact and copper was thermally very stable even after 350°C 30 min annealing; there is no atomic diffusion between this material system (Fig. 1).

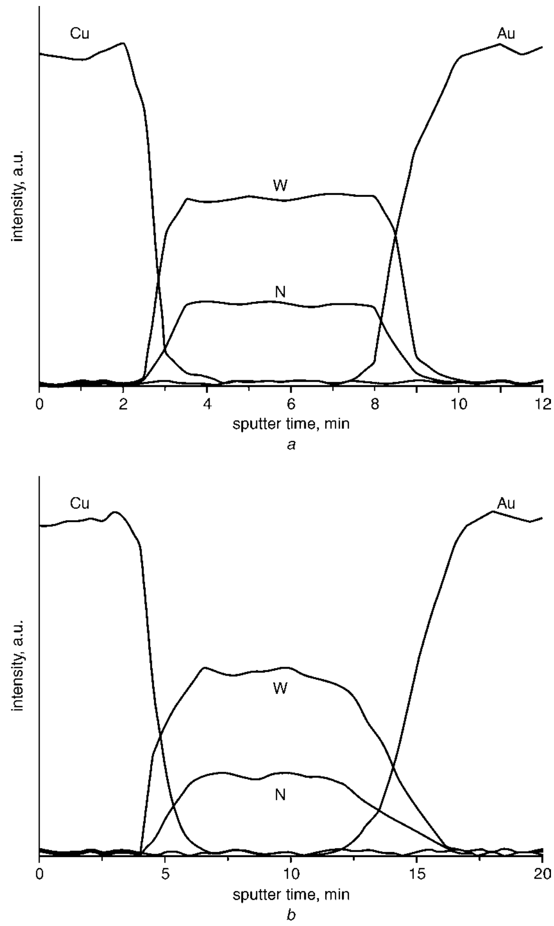

Fig. 1 *AES depth profiles of Au/WNx/Cu samples*

a as deposited
b After 350°C 30 min annealing

Results: The fabricated low noise PHEMT has a saturation drain current of 140 mA/mm and a transconductance of 375 mS/mm at $V_{DS} = 1.5$ V. The performance of the device after thermal annealing at 250°C for 20 h was also evaluated. The IV characteristics taken before and after thermal annealing were plotted in the same Figure for comparison (Figs. 2*a* and *b*). The DC performance shows very little change after thermal annealing (less than 5% change in saturation current and transconductance) as shown in Fig. 2.

The RF performance of the device after thermal annealing at 250°C for 20 h was also evaluated and is shown in Fig. 3. The noise figure for the 160 µm gate-width device is ~0.83 dB and the associated gain is 11.1 dB at 12 GHz before annealing. The gain of the device did not drop after thermal annealing at 250°C for 20 h, and the noise figure remained at 0.83 dB at 12 GHz. The device shows no obvious degradation after thermal annealing, the result is consistent with the AES results from Fig. 1 and demonstrates that the WNx barrier is an effective barrier to impede the copper diffusion during thermal annealing.

Conclusions: The sputtered WNx were successfully applied as the diffusion barrier to the fabrication of the copper airbridged AlGaAs/InGaAs low noise PHEMT. The fabricated copper airbridged low noise PHEMT with WNx diffusion barrier has a saturation drain current of 140 mA/mm and a transconductance of 375 mS/mm at $V_{DS} = 1.5$ V. The noise figure for the 160 µm gate-width device is ~0.83 dB and the associated gain is up to 11.1 dB at 12 GHz. The performance of the device did not decay even after thermal annealing at 250°C for 20 h. These results show that tungsten nitride is a thermally stable barrier for copper metallisation of GaAs devices and that the copper-metallised airbridges with WNx as the diffusion barrier can be used as the interconnects for the low noise GaAs based PHEMTs.

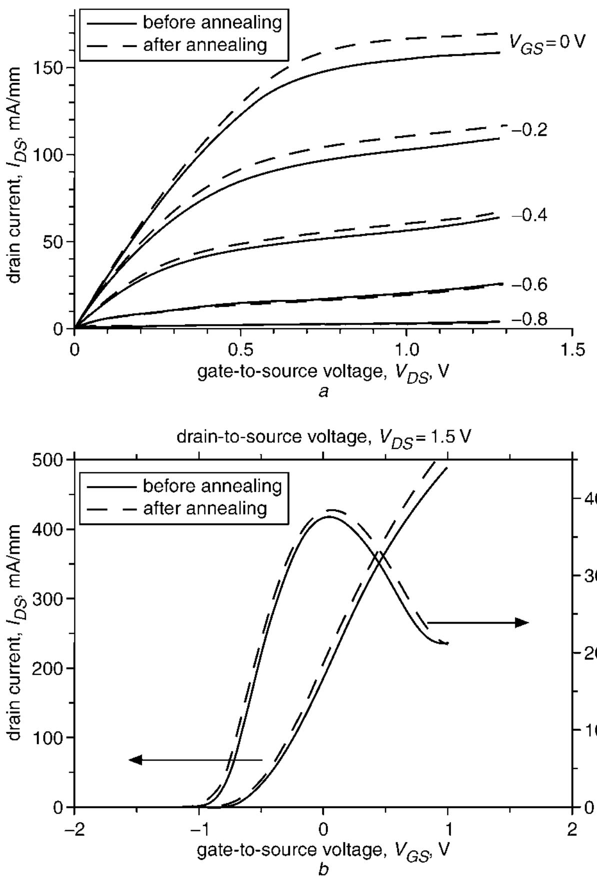

Fig. 2 *I-V characteristics and transconductance against gate bias characteristics of 0.25 × 160 μm LN-PHEMT before and after thermal annealing at 250°C for 20 h in nitrogen atmosphere*

a I-V characteristics

b Transconductance against gate bias characteristics

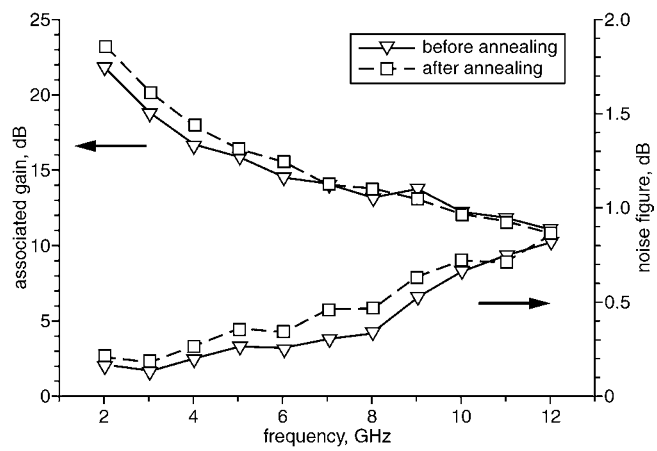

Fig. 3 *Noise figure and associated gain against frequency for 0.25 × 160 μm LN-PHEMT with copper-metallised airbridges and WNx diffusion barrier before and after thermal annealing at 250°C 20 h*

Acknowledgment: The work was sponsored jointly by the Ministry of Education, ROC, under contract X91016.

30 September 2003

Electronics Letters Online No: 20031133

DOI: 10.1049/el:20031133

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References

1 HOLLOWAY, K., and FRYER, P.M.: 'Tantalum as a diffusion barrier between copper and silicon', *Appl. Phys. Lett.*, 1990, **57**, (17), pp. 1736–1738

2 HOLLOWAY, K., *et al.*: 'Tantalum as a diffusion barrier between copper and silicon: failure mechanism and effect of nitrogen additions', *J. Appl. Phys.*, 1992, **71**, (11), pp. 5433–5444

3 YOON, D.S., BAIK, H.K., and LEE, S.M.: 'Effect on thermal stability of a Cu/Ta/Si heterostructure of the incorporation of cerium oxide into the Ta barrier', *J. Appl. Phys.*, 1998, **83**, (12), pp. 8074–8076

4 CHEN, C.Y., *et al.*: 'Thermal stability of Cu/Ta/GaAs multilayers', *Appl. Phys. Lett.*, 2000, **77**, (21), pp. 3367–3369

5 CHEN, C.Y., *et al.*: 'Backside copper metallisation of GaAs MESFETs', *Electron. Lett.*, 2000, **36**, (15), pp. 1318–1319

6 CHEN, C.Y., *et al.*: 'Backside copper metallization of GaAs MESFETs using TaN as the diffusion barrier', *IEEE Trans. Electron Devices*, 2001, **48**, (6), pp. 1033–1036