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Citation: Journal of Applied Physics **94**, 6735 (2003); doi: 10.1063/1.1621716
View online: http://dx.doi.org/10.1063/1.1621716
View Table of Contents: http://scitation.aip.org/content/aip/journal/jap/94/10?ver=pdfcov
Published by the AIP Publishing

Physical characteristics and electrical properties of $Sr_{0.8}Bi_{2+x}Ta_2O_9$ films on Al_2O_3/Si annealed at high temperature

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(Received 6 May 2003; accepted 4 September 2003)

Bismuth-containing layered perovskite $Sr_{0.8}Bi_{2+x}Ta_2O_9$ (SBT) thin films with $x=0-0.8$ were prepared to investigate annealing temperature effect, especially at high temperature, on physical characteristics and electrical properties of SBT films on Al_2O_3 (10 nm)/Si. At 800 °C, the $Sr_{0.8}Bi_2Ta_{2+x}O_9/Al_2O_3/Si$ exhibits ferroelectric mode and the width of memory window decreases with the increase of Bi content that is dependent on the effective coercive field. However, at a higher annealing temperature of 900 °C, a larger ferroelectric memory window was obtained for Bi-rich $Sr_{0.8}Bi_{2+x}Ta_2O_9$ ($x=0.4$ or 0.8) films compared to SBT film ($x=0$) that should be related to the reduced leakage current due to the formation of rod-shape grains and amorphous SBT composite layer. The leakage current of $Sr_{0.8}Bi_{2.4}Ta_2O_9/Al_2O_3/Si$ annealed at 900 °C is about 1.2×10^{-9} A/cm^2 that has two orders of magnitude lower than that of 800 °C-annealed SBT films measured at -100 kV/cm. However, the $Sr_{0.8}Bi_2Ta_2O_9$ ($x=0$) film on Al_2O_3/Si capacitor shows no obvious change with the increase of annealing temperature. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1621716]

I. INTRODUCTION

Although the metal/ferroelectric/semiconductors one-transistor memory has been studied for about 40 years,[1] the progress of this memory is still very slow because of the problems of interface reaction between ferroelectric material and Si.[2,3] In order to overcome these problems, an intermediate layer of SiO_2,[4] CeO_2,[5] or Y_2O_3 (Ref. 6) is inserted between ferroelectric material and Si to form metal/ferroelectric/insulator/semiconductors structure (MFIS).[7,8] However, it was found that the MFIS structure with these buffer layers have large absorption current due to the high density of crystalline defects or carrier traps existing in the interface of Si and buffer layer. Al_2O_3 has been considered as the candidate because the Al_2O_3 is amorphous and good diffusion barrier with low interface trap density.[9] Furthermore, taking process integration issues with next generation high performance and low voltage logic technology into account, ultrathin gate dielectrics with large capacitance are required. Recently, we have reported the results of one-transistor (1T) ferroelectric metal-oxide-semiconductor field effect transistor (FeMOSFET) memory, using ultrathin Al_2O_3 with thickness of 40 Å as both gate dielectric and diffusion barrier due to the high k and excellent diffusion barrier properties.[10,11] However, up to now, the discussions of annealing temperature effect on ferroelectric thin films have focused on low processing temperature because high temperature treatment may cause the ferroelectric property deterioration, especially for metal-ferroelectric-metal (MFM) structure. It is noticed that although a low temperature annealing is required for ferroelectric material used in one-transistor-one-capacitor ferroelectric random access memory, a high temperature stable ferroelectric is also necessary for the 1T FeMOSFET because of the process integration consideration. However, owing to the interdiffusion at the interface of ferroelectric/insulator/Si at high annealing temperature, it was commonly recognized that the electrical properties of the MFIS structure would be deteriorated. Therefore, up to now, only little work was focused on the issue of high annealing temperature effect on the electrical properties and structure change. Recently, Lee *et al.* reported that the memory window of SBT thin films on $Si_3N_4/SiO_2/Si$ capacitor was in the range of 0.75–1.2 V with annealing temperature from 800 to 900 °C.[12] Our group has also demonstrated that with increasing annealing temperature from 650 to 900 °C, a larger memory window size with a lower leakage current was obtained for BLT/Al_2O_3/Si capacitor.[13] However, no detailed explanation was proposed to elucidate the role of high annealing temperature in the electrical characteristics of MFIS structure. Therefore, the effect of high annealing temperature on electrical properties of SBT-based MFIS structure will be systematically studied in this work.

Furthermore, it is well known that the electrical properties of ferroelectric film are strongly influenced by composition and microstructure change. Previous reports in the literature demonstrated that the bismuth content shows strong influence on the ferroelectric properties of Bi-based MFM structure and that excess Bi is usually required to compensate for the loss of Bi due to the high volatility of Bi during processing and Bi diffusion into the bottom electrode during annealing.[14,15] However, for the Bi-based MFIS structure annealed at higher temperature, the effect of excess Bi on the electrical properties and structure change is more important and worthy of investigation. Therefore, in this work, the role

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of Bi content in electrical properties of SBT-based MFIS structure will also focused and discussed.

II. EXPERIMENT

4-in. Si *p*-type wafers were used in this study. After *in situ* native oxide desorption, amorphous Al layer was thermally evaporated on wafers. The Al layer was oxidized at a temperature of 400 °C for 2 h to form 10 nm Al_2O_3 and finally annealed at 800 °C for 30 min in nitrogen ambient. More detailed fabrication process can be found in our previous works.[16] The SBT precursors were prepared by metalorganic deposition process using strontium 2-ethylhexanotate $[Sr(C_8H_{15}O_2)_2]$, bismuth 2-ethylhexanoate $[Bi(C_8H_{15}O_2)_2]$, tantalum ethoxide $[Ta(OC_2H_5)_5]$ as the metalorganic precursors. The xylene was used as solvent to mix with metalorganic precursors to form the solution. The solutions with the compositions of $Sr_{0.8}Bi_{2+x}Ta_2O_9$ ($x=0-0.8$) were spin coated on the Al_2O_3/Si substrate at 4000 rpm for 30 s and then dried on a hot plate at a temperature of about 350 °C. This procedure was repeated for several times to obtain the desired film thickness about 340 nm. The as-deposited films were annealed at different temperatures from 650 to 900 °C for 30 min. After that, the Al electrodes were formed by thermal evaporation. The electrode area of the stacked capacitor is 3.14×10^{-4} cm^2. The crystal structure of SBT films was detected by MAC Science M18XHF x-ray diffractometer with Cu $K\alpha$ radiation. The crystal structures of the films were analyzed by using x-ray diffraction (XRD) with Cu $K\alpha$ radiation and a Ni filter. The chemical composition of the films was determined using inductively coupled plasma (ICP) mass spectroscopy. Three samples were performed for the ICP analysis and calculated with error deviation of ~5%. The surface morphology of the films was examined using Hitachi S-4000 scanning electron microscopy (SEM) and the total thickness of SBT films was measured by cross-sectional SEM images. Transmission electron microscopy (TEM, Philip Technai 20) was used to observe the microstructure and analyze the element distribution of the films. The electrical properties were characterized by $I-V$ and $C-V$ measurements using HP-4156 and HP-4284, respectively.

III. RESULTS AND DISCUSSION

A. Crystal phase and microstructure

Since the Sr-deficient SBT films have been reported to exhibit more excellent polarization compared to stoichiometric SBT film,[17] the compositions of Sr-deficient $Sr_{0.8}Bi_{2+x}Ta_2O_9$ (SBT) with $x=0-0.8$ were used in this work. The XRD patterns in Fig. 1(a) show that above 700 °C, the (115) diffraction peak of $Sr_{0.8}Bi_{2.4}Ta_2O_9$ films becomes sharper and perovskite SBT phase has been fully developed on Al_2O_3/Si substrates that is probably correlated with Bi-excess composition and layered perovskite structure of the SBT. Even annealing the $Sr_{0.8}Bi_{2.4}Ta_2O_9$ films at 800–900 °C, the obtained SBT films are polycrystalline and no other second or undesirable pyrochlore phases are detected. Similarly, for the $Sr_{0.8}Bi_{2+x}Ta_2O_9$ films with various Bi contents ($x=0-0.8$) annealed at 900 °C, the XRD patterns (not shown here) illustrate no apparent differences. In contrast, when the SBT was deposited on the $Pt/Ti/SiO_2/Si$ substrate, Fig. 1(b) shows that perovskite SBT phase was developed at 700 °C and with increasing annealing temperature up to 850 °C, besides the presence of the perovskite SBT, a small amount of pyrochlore phase was generated especially for the film with $x=0$.[18,19]

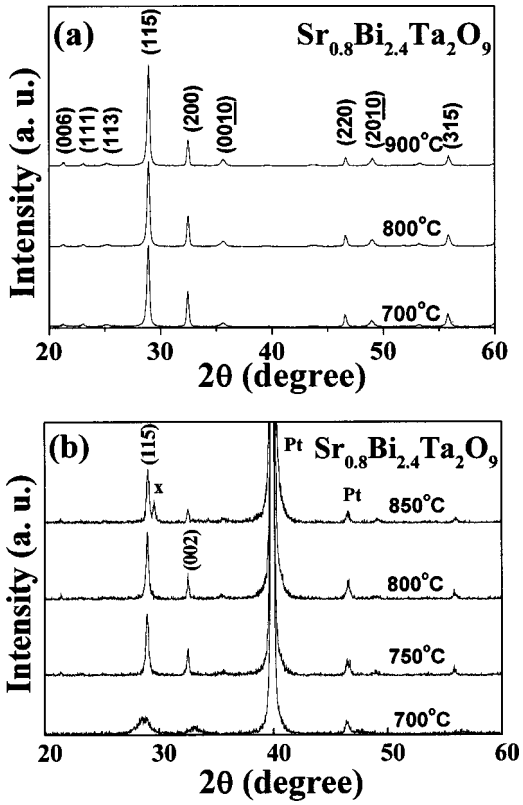

FIG. 1. XRD patterns of $Sr_{0.8}Bi_{2.4}Ta_2O_9$ films on (a) Al_2O_3/Si and (b) $Pt/Ti/SiO_2/Si$ as a function of annealing temperature.

The chemical compositions of $Sr_{0.8}Bi_{2+x}Ta_2O_9$ on $Pt/Ti/SiO_2/Si$ substrate were analyzed by ICP, showing that after annealed at 800 °C for 0.5 h, the molar ratio of Sr, Bi, and Ta in the film is very close to the composition in the precursor solutions except for a partial loss of Bi and an extra detectable Ti compared to those in precursor solutions. As the $Sr_{0.8}Bi_{2+x}Ta_2O_9$ film was further annealed at 850 °C for 0.5 h, the Sr/Bi/Ta ratio normalized in Ta=2 is approximately to 0.73/1.73/2.0, 0.75/1.97/2.0, and 0.74/2.21/2.11/2.0 for $x=0$, 0.2, and 0.4, respectively. This reveals the occurrence of Bi loss at such a higher annealing temperature and the importance of excess Bi for the SBT films.

Figure 2 illustrates the typical (FESEM) surface images of $Sr_{0.8}Bi_{2+x}Ta_2O_9$ ($x=0$ or 0.4) on Al_2O_3/Si at 800 and 900 °C, respectively. It was observed that the grain size of SBT thin films is strongly dependent on annealing temperature and bismuth content. As shown in Figs. 2(a) and 2(b) for SBT with $x=0$ and $x=0.4$ films annealed at 800 °C, respectively, the grain size is larger for Bi-rich $Sr_{0.8}Bi_{2.4}Ta_2O_9$ film compared to $Sr_{0.8}Bi_2Ta_2O_9$ film. The microstructure of $Sr_{0.8}Bi_{2.4}Ta_2O_9$ film presents rod-like grains and loose matrix. On the other hand, a dense microstructure consisting of finer and round grains was observed for the $Sr_{0.8}Bi_2Ta_2O_9$

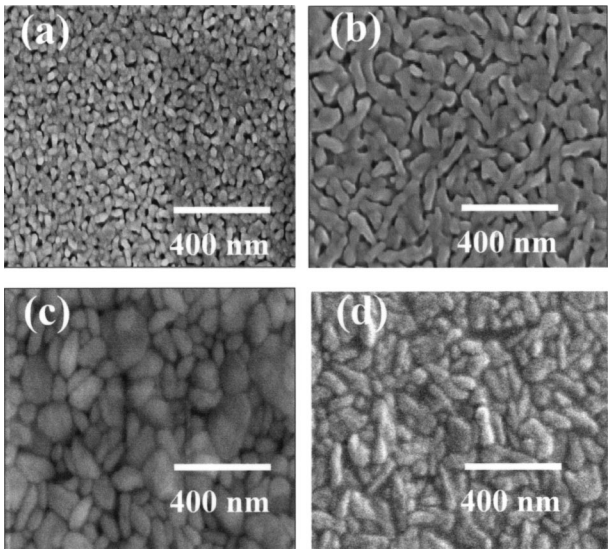

FIG. 2. SEM images of $Sr_{0.8}Bi_{2+x}Ta_2O_9$ films annealed at 800 °C for (a) $x=0$, (b) $x=0.4$ and 900 °C for (c) $x=0$, (d) $x=0.4$.

film. As increasing annealing temperature from 800 to 900 °C, a dense microstructure with larger grains was observed in Fig. 2(c) for the 900 °C-annealed $Sr_{0.8}Bi_2Ta_2O_9$ thin film. However, for Bi-rich $Sr_{0.8}Bi_{2.4}Ta_2O_9$ films shown in Fig. 2(d), a rod-grain or sheet-grain matrix interposed with smaller black areas in between grain boundaries was observed, which mostly shows up in the Bi-rich $Sr_{0.8}Bi_{2.4}Ta_2O_9$ films at high annealing temperatures.

Figure 3 shows that the cross-sectional TEM image of the $Sr_{0.8}Bi_{2+x}Ta_2O_9/Al_2O_3/Si$ structure annealed at 800–900 °C in the oxygen ambient. As shown in Figs. 3(a) and 3(b) for the SBT with $x=0$ and 0.4 films annealed at 800 °C, a sharp interface between Si and Al_2O_3 was observed. No apparent difference was seen. With increasing annealing temperature up to 900 °C, Fig. 3(c) illustrates that a little diffusion envelop (as marked with the arrow) was formed at the interface of Al_2O_3 insulator and Si for the SBT with $x=0$ film. According to EDS analysis (not shown here), the reaction layer is confirmed to contain the elements of Bi, Al, and Si. On the other hand, for Bi-rich $Sr_{0.8}Bi_{2.4}Ta_2O_9/Al_2O_3/Si$ structure annealed at 900 °C, as shown in Fig. 3(d), the Al_2O_3 layer becomes thinner and the SBT film on Al_2O_3/Si was separated into two layers. The top layer is composed of rod-shape SBT grains and the bottom layer becomes amorphous structure. As revealed by Auger electron spectroscopy (AES) (no shown here), the Si has been diffused into Al_2O_3. According to our previous study,[20] it is suggested that the amorphous structure is probable SBT composite insulator containing Sr, Bi, Ta, Si, and Al.

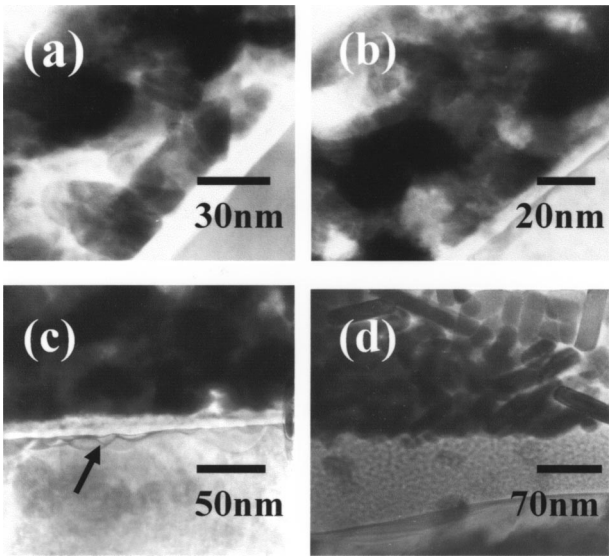

FIG. 3. Cross-sectional TEM images of $Sr_{0.8}Bi_{2+x}Ta_2O_9/Al_2O_3/Si$ structure annealed at 800 °C for (a) $x=0$, (b) $x=0.4$ and 900 °C for (c) $x=0$, (d) $x=0.4$.

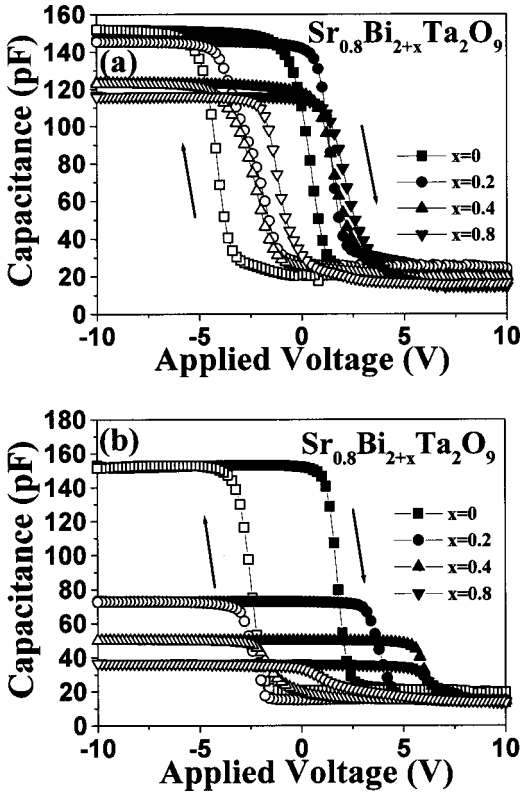

FIG. 4. $C-V$ curves of $Sr_{0.8}Bi_{2+x}Ta_2O_9/Al_2O_3/Si$ capacitors as a function of bismuth content at (a) 800 °C and (b) 900 °C.

B. $C-V$ and memory window characteristics

The $C-V$ characteristics of $SBT/Al_2O_3/Si$ capacitors were measured at 1 MHz. Figure 4 shows the typical $C-V$ curves and the memory windows of $SBT/Al_2O_3/Si$ with different Bi concentration annealed at 800–900 °C. The bias is swept from −10 to +10 V. The positive memory window value is related to a clockwise hysteresis loop attributed to the ferroelectric mode. It was found that with increasing Bi concentration, the $C-V$ loops were shifted toward right (positive voltage) that is attributed to a little diffusion of Bi into Si as evidenced from the TEM (Fig. 3). The diffusion of Bi into Si causes the enhanced acceptor concentration in the interface and therefore, the charge in the depleted area was increased that cause the shift of threshold voltage to the positive direction. In addition, the decrease in the capacitance

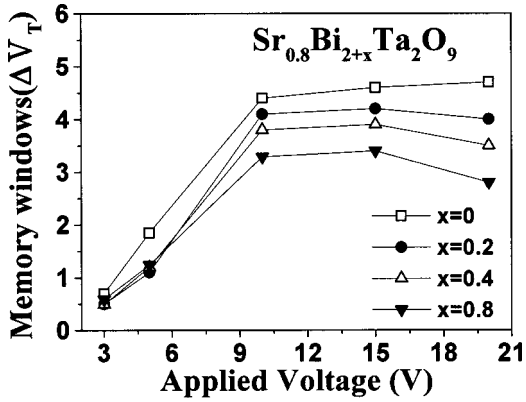

FIG. 5. Relationship between memory window and applied voltage for $Sr_{0.8}Bi_{2+x}Ta_2O_9/Al_2O_3/Si$ capacitors annealed at 800 °C.

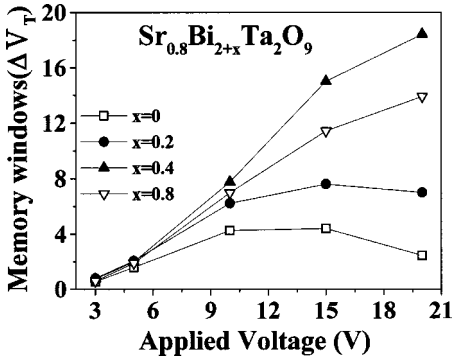

FIG. 7. Relationship between memory window and applied voltage for $Sr_{0.8}Bi_{2+x}Ta_2O_9/Al_2O_3/Si$ capacitors annealed at 900 °C.

with increasing the Bi concentration, especially for the MFIS structure annealed at 900 °C, is strongly related to the formation of amorphous SBT shown in Fig. 3(d). Figure 5 shows that the SBT films exhibit ferroelectric mode and the width of memory window becomes larger at higher write voltages up to ±15 V. Above that, the charge injection will be induced into the Al_2O_3 from Si since the electrons severely penetrate into the Al_2O_3. Therefore, according to the following relationships, the memory window will be reduced:

$$V_m = 2E_c - V_{ci}, \tag{1}$$

where V_m is the memory window, $2E_c$ the effective double coercive voltage, and V_{ci} the flat-band voltage shift due to charge injection. The larger memory window of SBT with $x=0$ compared to that of Bi-rich SBT ($x=0.4$) is primarily attributed to the decrease in V_{ci} and the increase in $2E_c$. As illustrated in Fig. 6 for the polarization versus electric field hysteresis loops of $Pt/SBT/Pt/Ti/SiO_2/Si$ structures, with increasing the Bi concentration from $x=0$ to $x=0.4$, the coercive field ($2E_c$) decreases from 145 to 107 kV/cm at the applied voltage of 6 V, indicating that the SBT with $x=0$ shows a larger memory window than that with $x=0.4$ on the same Al_2O_3/Si structure because the former has a larger coercive field than the latter based on Eq. (1).

As the $Sr_{0.8}Bi_{2+x}Ta_2O_9/Al_2O_3/Si$ was annealed at 900 °C, Fig. 7 demonstrates that the memory window increases with the applied voltage, and a saturated memory window of 4–7 V was attained for the SBT with $x=0$ and 0.2 films. In sharp contrast, for the Bi-rich SBT films ($x=0.4$ and 0.8), the memory window values become larger at higher applied voltages even up to ±20 V. A large memory window of 18 V was obtained for the 900 °C-annealed samples at the applied voltage of 20 V and this should be the largest ferroelectric memory window reported so far. Although the SiO_2 was probably formed, from the cross-sectional TEM image (not shown here), no obvious SiO_2 interface layer was detected even in the higher magnification. Therefore, the effect of SiO_2 on the effective field applied on the SBT can be neglected because it is too thin (<1 nm) to be detected. The enhancement of memory window can be elucidated by the electric field distribution between the SBT and Al_2O_3 as follows:

$$E_f = \left(\frac{\varepsilon_i}{\varepsilon_f d_i + \varepsilon_i d_f}\right) V_G, \tag{2}$$

where E, ε, and d are the effective applied to a capacitor, the dielectric constant, and the thickness, respectively. The subscripts of f and i stand for the ferroelectric and insulator, respectively, and V_G is the applied gate voltage. As one can see the cross-sectional TEM of Bi-rich $Sr_{0.8}Bi_{2.4}Ta_2O_9/Al_2O_3/Si$ in Fig. 3(d), the original SBT was separated into two layers consisting of high dielectric ($\varepsilon = 200-250$) perovskite SBT and low dielectric constant amorphous SBT structure. Therefore, the dielectric constant of the overall Bi-rich SBT can be decreased and more applied voltage is distributed over the SBT film compared to SBT with $x=0$ film. Furthermore, owing to the formation of amorphous SBT structure that is similar to the insulator, the $Sr_{0.8}Bi_{2+x}Ta_2O_9/Al_2O_3/Si$ can be applied under a higher voltage without dielectric breakdown. Therefore, a larger memory window can be obtained for the $Sr_{0.8}Bi_{2+x}Ta_2O_9$ ($x=0.4$ and 0.8)$/Al_2O_3/Si$.

The above results apparently reveal the importance of Bi content on memory characteristics of the $SBT/Al_2O_3/Si$ structure. In addition, as the SBT films were annealed at such a higher temperature, the Bi loss from either evaporation or diffusion would occur. As shown in the ICP results for SBT films on $Pt/Ti/SiO_2/Si$ substrates, the Bi concentration in the Bi-rich SBT ($x=0.4$) films is close to 2 ($x=0$). According to our results in Fig. 6 and the report of Watanabe *et al.*[21]

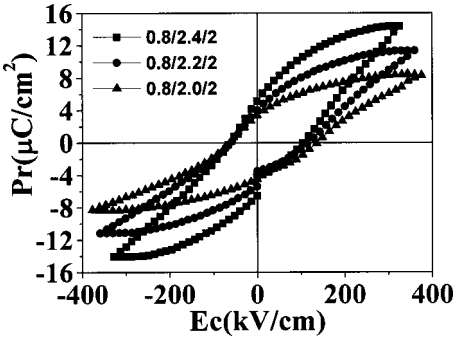

FIG. 6. $P-E$ hysteresis loops of $Sr_{0.8}Bi_{2+x}Ta_2O_9$ films with various bismuth contents on $Pt/Ti/SiO_2/Si$ annealed at 800 °C for 0.5 h under an applied voltage of 6 V.

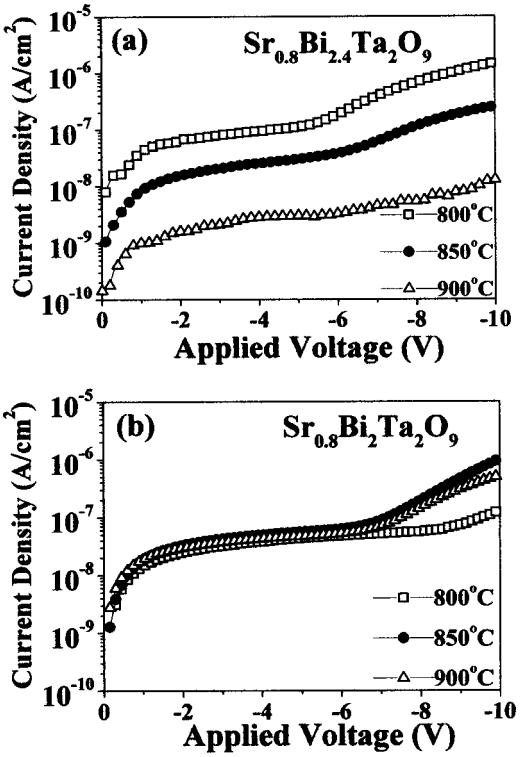

FIG. 8. Dependence of annealing temperatures on $J-V$ characteristics of (a) $Sr_{0.8}Bi_{2.4}Ta_2O_9$ and (b) $Sr_{0.8}Bi_2Ta_2O_9$ on Al_2O_3 /Si.

that the stoichiometric SBT film shows a larger coercive field compared to Bi-less and Bi-rich SBT films. Therefore, at 900 °C, a maximum memory window appears at the SBT film with $x=0.4$. This further demonstrates that the memory window is dominated by not only the annealing temperature but also the bismuth content in the SBT films.

C. Leakage current

We have also investigated the current–voltage characteristics because the leakage current is one of the most important properties for memory capacitor. Figure 8 illustrates $J-V$ curves of $Sr_{0.8}Bi_{2+x}Ta_2O_9/Al_2O_3/Si$ capacitors annealed at different temperatures. As shown in Fig. 8(a), the leakage current density of $Sr_{0.8}Bi_{2.4}Ta_2O_9/Al_2O_3/Si/Al_2O_3/Si$ annealed at 800 °C is 1.7×10^{-7} A/cm^2 at -100 kV/cm and it increases at high voltages. On the other hand, for the samples annealed at 900 °C, the leakage current (1.2×10^{-9} A/cm^2) reduces ~2 orders of magnitude at -100 kV/cm. In addition, no dielectric breakdown up to -10 V also implies that the Bi-rich SBT film annealed at high temperatures has better dielectric integrity than that annealed at 800 °C. This smaller leakage current and larger breakdown voltage for Bi-rich SBT films annealed at 900 °C may be related to the microstructure of rod-shape grains and the formation of insulator amorphous SBT that makes the leakage current lower. Similar trend was also observed in our previous research for ferroelectric BLT thin films on Al_2O_3/Si.[13] On the other hand, for $Sr_{0.8}Bi_2Ta_2O_9$ thin film annealed at 800 °C [Fig. 8(b)], a lower leakage current was obtained as compared to $Sr_{0.8}Bi_{2.4}Ta_2O_9$ film that is probably due to the diffusion of Bi or the formation of highly conductive Bi_2O_3 as revealed by Shimakawa *et al.*[14] At 900 °C, although the enhanced densification in the SBT films can reduce the leakage current, the increased grain size probably leads to the increase of leakage current. Therefore, with an increase of annealing temperature, no obvious change in the leakage current of Fig. 8(b) was observed for the SBT ($x=0$) film. However, the leakage current of the SBT ($x=0$) film at 900 °C is still higher than that of Bi-rich SBT ($x=0.4$) film based on the $Sr_{0.8}Bi_{2+x}Ta_2O_9/Al_2O_3/Si$ structure.

IV. CONCLUSION

In conclusion, we have studied the annealing temperature dependent characteristics of $Sr_{0.8}Bi_{2+x}Ta_2O_9/Al_2O_3/Si$. At 800 °C, the $Sr_{0.8}Bi_{2+x}Ta_2O_9/Al_2O_3/Si$ exhibits ferroelectric mode. With increasing annealing temperature up to 900 °C, it was found that Bi-rich SBT($x=0.4$)/Al_2O_3/Si presents a larger memory window compared to SBT film ($x=0$) that should be related to the reduced leakage current due to the formation of rod-shape grains and amorphous SBT layer. The leakage current of $Sr_{0.8}Bi_{2.4}Ta_2O_9/Al_2O_3/Si$ annealed at 900 °C is about 1.2×10^{-9} A/cm^2 at 100 kV/cm and reduced by two orders of magnitude lower than that annealed at 800 °C. All the results in this study demonstrate that the high annealing temperature makes the stack gate SBT/Al_2O_3/Si process compatible with current VLSI technology.

ACKNOWLEDGMENT

This work has been supported by the National Science Council Contract No. NSC-91-2215-E-009-051 of Taiwan.

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