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Dummy-Gate Structure to Improve Turn-on Speed of Silicon-Controlled Rectifier (SCR) Device for Effective Electrostatic Discharge (ESD) Protection

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Turn-on speed is the main concern for on-chip electrostatic discharge (ESD) protection device, especially in deep submicron complementary metal-oxide semiconductors (CMOS) processes with ultra-thin gate oxide. A novel dummy-gate-blocking silicon-controlled rectifier (SCR) device with substrate-triggered technique is proposed to improve the turn-on speed of SCR device for using in on-chip ESD protection circuit to effectively protect the much thinner gate oxide. From the experimental results, the switching voltage, turn-on resistance, and turn-on time of substrate-triggered SCR (STSCR) device with dummy-gate structure have been efficiently improved, as compared with the normal SCR with shallow trench isolation (STI) structure. [DOI: 10.1143/JJAP.42.L1366]

KEYWORDS: dummy gate, silicon controlled rectifier (SCR), substrate-triggered technique, electrostatic discharge (ESD), ESD protection

For deep submicron complementary metal-oxide semiconductors (CMOS) technologies, the gate oxide thickness has been scaled down to increase circuit operating speed, however, its time-to-breakdown, t_{BD}, or charge-to-breakdown, Q_{BD}, will also decrease. The ultra-thin gate oxide can not sustain the overstressed electrostatic discharge (ESD) pulse too long. ESD events will cause latent damages[1,2] or failure to core circuits, if the ESD protection circuits did not work in time. The excellent ESD protection device must have high enough ESD robustness and faster turn-on speed to effectively protect the thinner gate oxide of input stage from ESD overstress. With the best area efficiency, silicon-controlled rectifier (SCR) can sustain highest ESD level in a smallest layout area, as compared with other ESD protection devices. So, SCR had been used as on-chip ESD protection for a long time.[3,4] But, SCR still has a higher switching voltage (~20 V) in CMOS technology, which is generally greater than the gate-oxide breakdown voltage of the input stage. Some reports had presented the solutions to overcome this issue,[5–7] including the STSCR device.[8]

In this work, a novel dummy-gate structure is used to block the shallow trench isolation (STI) region in SCR device and to further enhance its turn-on speed. With suitable ESD-detection circuit, the STSCR with dummy-gate structure is designed to be kept off during the normal circuit operating conditions, and to be quickly triggered on during the ESD-zapping conditions. Therefore, the ultra-thin gate oxide in deep submicron CMOS processes can be effectively protected by the STSCR with dummy-gate structure.

The normal fully-silicided substrate-triggered SCR (STSCR) device with STI structure[8] is shown in Fig. 1(a). In a typical 130-nm CMOS process, the depth of STI is about ~0.4 μm, but the junction depth of P^+/N^+ diffusion is only about ~0.15 μm. The deeper STI region in SCR device causes a longer current path from the anode to the cathode, which also leads to a slower turn-on speed of SCR. In order to further enhance the turn-on speed of STSCR device, the STI structure must be blocked. In this work, a dummy-gate structure is proposed to block the silicide and STI between the diffusion regions in SCR device without adding extra process masks and increasing the fabrication costs. The proposed STSCR device with dummy-gate structure is shown in Fig. 1(b). The ESD current path in the STSCR with dummy-gate structure indicated by the dashed line in Fig. 1(b) is shorter than that in STSCR with STI in Fig. 1(a), because the dummy-gate structure is used to block the STI region in SCR device. The inserted P^+ diffusions are connected out as the p-trigger node of the STSCR. When a trigger current is applied into the trigger node, the STSCR can be triggered on into its latching state. For ESD protection purpose, the corresponding ESD-detection circuit has to be designed to control the turn-on of the STSCR.

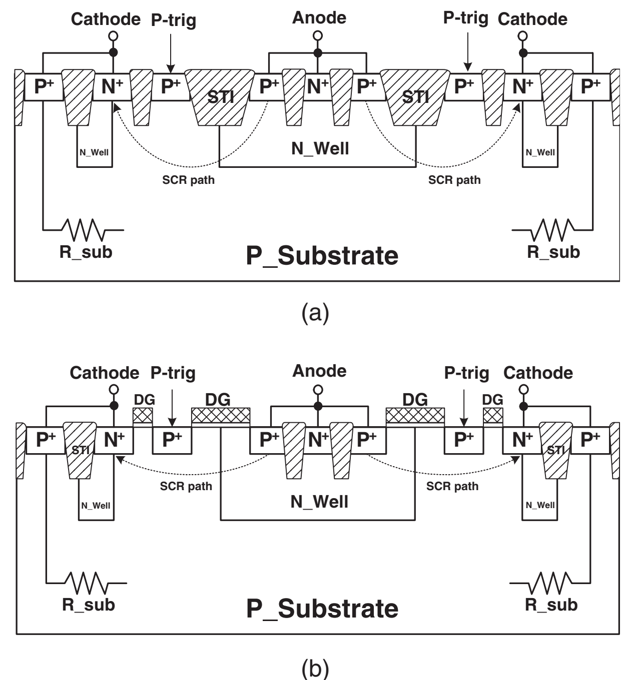

Fig. 1. Device structures of (a) the substrate-triggered SCR (STSCR) device with shallow trench isolation (STI), and (b) the STSCR device with dummy-gate structure.

(1) Device Characteristics

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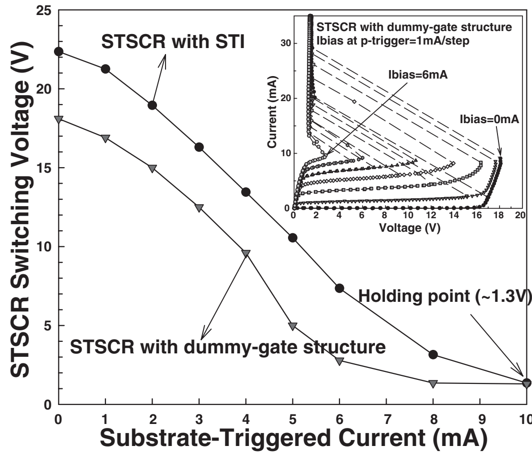

Fig. 2. The dependences of switching voltages of STSCR devices on the substrate-triggered current with the inset of *I-V* curves of STSCR with dummy-gate structure under different triggered currents.

The two fully-silicided STSCR devices with STI and dummy-gate structures have been fabricated with the same layout area in a 0.25-μm CMOS process. The dependences of switching voltages (V_{t1}) of STSCRs with STI and dummy-gate structures on the substrate-triggered current are compared in Fig. 2 and the inset of Fig. 2 is the DC *I-V* curves of STSCR with dummy-gate structure under different substrate-triggered currents. When the substrate-triggered current at the p-trigger node is increased from 0 to 6 mA, the V_{t1} of STSCR with STI is reduced from ~22 to ~7 V, whereas the V_{t1} of STSCR with dummy-gate structure is reduced from ~18 to ~3 V. If the trigger current is continually increased, the V_{t1} of the STSCRs will be nearly reduced to their holding voltages (~1.3 V). This result has proven that the V_{t1} of both STSCRs with STI and dummy-gate structure can be significantly reduced by the substrate-triggered technique. Moreover, the V_{t1} of STSCR with dummy-gate structure can be further reduced lower than that of STSCR with STI under the same trigger current. This is related to the current gain (β) of parasitic bipolar transistor in SCR structure, which will be discussed later. The SCR device with lower switching voltage can clamp ESD overstresses more quickly to effectively protect the thinner gate oxide of input circuits.

(2) Turn-on Speed

The turn-on time of STSCR is defined as the time for STSCR entering into its latching state. The measured turn-on times for STSCRs with STI and dummy-gate structures are shown in Figs. 3(a) and 3(b), respectively. The inset of Fig. 3(a) is its measurement setup. From Fig. 3(a), the turn-on time of STSCR with STI is reduced from 35, 20, to 11.2 ns, while the STSCR is triggering by the voltage pulse of 1.5, 2, and 4 V with 10-ns rise time into the trigger node. Moreover, from Fig. 3(b), the turn-on time of STSCR with dummy-gate structure is further reduced from 25.4, 13.6, to 9.8 ns under the same measurement conditions as those of Fig. 3(a). For CMOS integrated circuit (IC) applications with ultra-thin gate oxide, the STSCR with dummy-gate structure can be

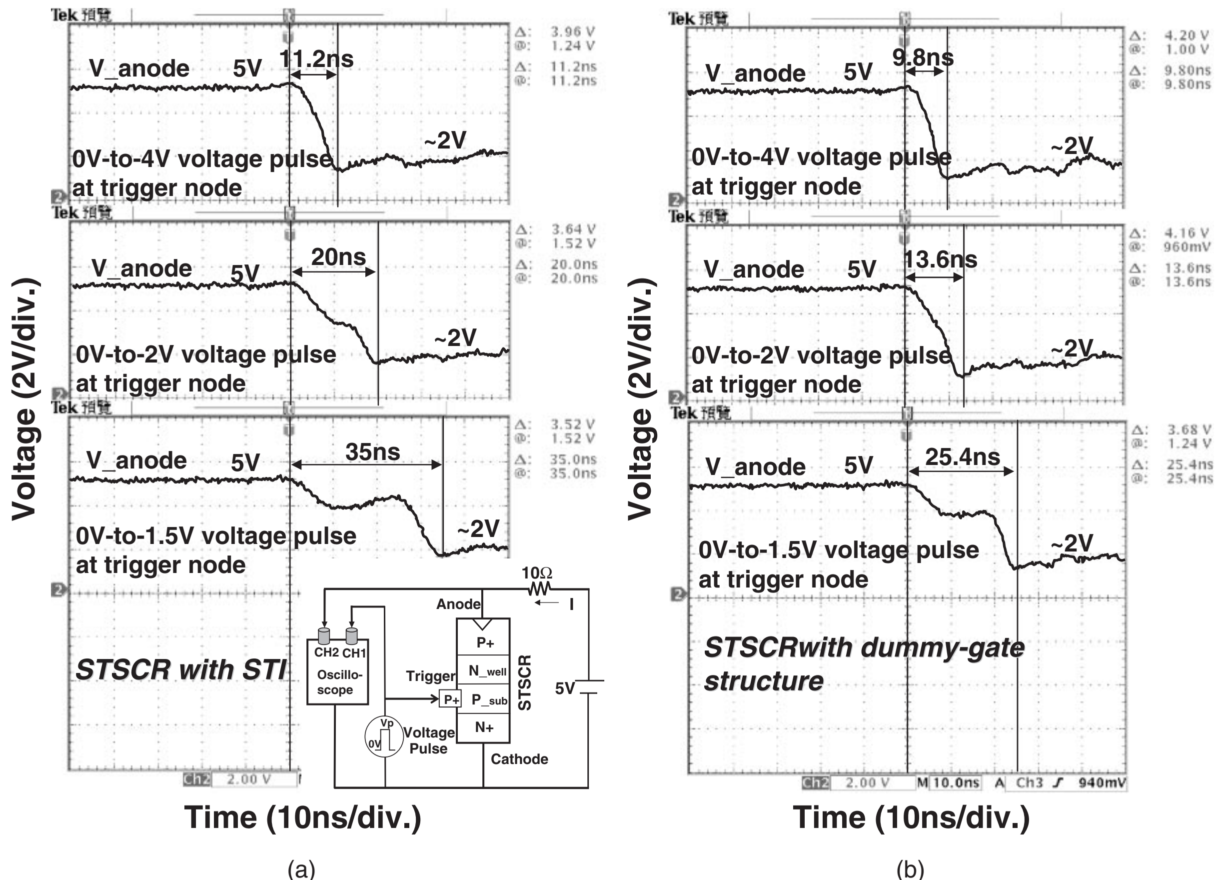

Fig. 3. The measured voltage waveforms of turn-on time on the anode of the STSCR with (a) STI, and (b) dummy-gate structure, under different voltage pulses with 10-ns rise time. The inset in (a) is the measurement setup.

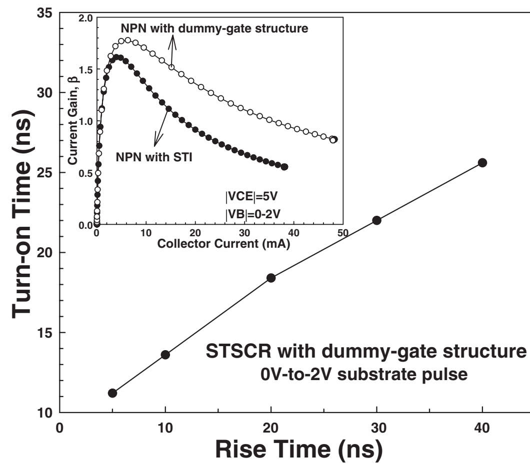

Fig. 4. The dependence of turn-on time of STSCR with dummy-gate structure on rise time of voltage pulse under 0-to-2 V substrate pulse condition. The inset is the dependence of current gains of the NPN bipolar transistors in the STSCR devices on its collector current.

designed to protect the core circuits from latent damages more efficiently than the STSCR with STI. The dependence of turn-on time of STSCR with dummy-gate structure on rise time of voltage pulse under 0-to-2 V substrate pulse condition is shown in Fig. 4. When a 2-V substrate pulse with rise time of 5 ns is applied to the p-trigger node, the turn-on time of the STSCR with dummy-gate structure can be shortened to only 10 ns. The turn-on time of such STSCR with dummy-gate structure can be reduced with the reduction of pulse rise time to efficiently protect the ultra-thin gate oxide, if the high enough voltage pulse has been applied to the STSCR device. The dependence of current gains of NPN bipolar transistors in the STSCR with STI and dummy-gate structure on the collector current under the measured conditions of $|V_{CE}| = 5\,V$ and $|V_B| = 0–2\,V$ is shown in the inset of Fig. 4. The current gain of NPN in the STSCR with dummy-gate structure is higher than that of NPN in the STSCR with STI. The switching voltage of STSCR device is in inverse proportion to the current gain,[9] so the STSCR with dummy-gate structure has the lower switching voltage. In addition, substrate bias used to trigger the NPN transistor in the STSCR device has significant effect to further reduce V_{t1} and turn-on time of STSCR with dummy-gate structure.

The novel dummy-gate structure in SCR device with substrate-triggered design has been successfully investigated in a 0.25-μm salicided CMOS process. The dummy-gate structure can indeed reduce the switching voltage, turn-on resistance, and turn-on time of STSCR device, as compared with the traditional SCR structure. With an improved turn-on speed, the proposed STSCR with dummy-gate structure can effectively protect the ultra-thin gate oxide against ESD damage in deep submicron CMOS integrated circuits.

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