# Design of a Sensorless Commutation IC for BLDC Motors

Kuang-Yao Cheng, *Student Member, IEEE*, and Ying-Yu Tzou, *Member, IEEE*

***Abstract*—This paper presents the design and realization of a sensorless commutation integrated circuit (IC) for brushless dc motors (BLDCMs) by using mixed-mode IC design methodology. The developed IC can generate accurate commutation signals for BLDCMs by using a modified back-EMF sensing scheme instead of using Hall-effect sensors. This IC can be also easily interfaced with a microcontroller or a digital signal processor (DSP) to complete the closed-loop control of a BLDCM. The developed sensorless commutation IC consists of an analog back-EMF processing circuit and a programmable digital commutation control circuit. Since the commutation control is very critical for BLDCM control, the proposed sensorless commutation IC provides a phase compensation circuit to compensate phase error due to low-pass filtering, noise, and nonideal effects of back-EMFs. By using mixed-mode IC design methodology, this IC solution requires less analog compensation circuits compared to other commercially available motor control ICs. Therefore, high maintainability and flexibility can be both achieved. The proposed sensorless commutation IC is integrated in a standard 0.35-$\mu$m single-poly four-metal CMOS process, and the realization technique of this mixed-mode IC has been given. The proposed control scheme and developed realization techniques provide illustrative engineering procedures for the system-on-a-chip solution for advanced digital motor control. Simulation and experimental results have been carried out in verification of the proposed control scheme.**

***Index Terms*—Brushless dc motors, digital motor control, mixed-mode IC design, phase compensation, sensorless commutation control, speed estimation, system-on-a-chip.**

## I. Introduction

In comparison to induction motors, brushless dc motors (BLDCMs) possess some distinct advantages such as higher power density, higher efficiency, and simpler controllability. Hence BLDCMs are becoming more and more attractive for many industrial applications, such as compressors, electrical vehicles, and DVD players etc. Since BLDCMs use permanent magnets for excitation, rotor position sensors are needed to perform electrical commutation. Usually, three Hall effect sensors are used as rotor position sensors for a BLDCM. However, the rotor position sensors present several disadvantages from the standpoint of total system cost, size, and reliability. For this reason, it is desired to eliminate these sensors from the motor, i.e. sensorless control. Many research working on controlling the motor speed of BLDCMs without rotor position sensors have been reported in the literatures [1]–[6].

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The authors are with the Power Electronics and Motion Control Laboratory, Department of Electrical and Control Engineering, National Chiao Tung University, Hsinchu, Taiwan, R.O.C. (e-mail: brian.ece88g@nctu.edu.tw; yytzou@cc.nctu.edu.tw).

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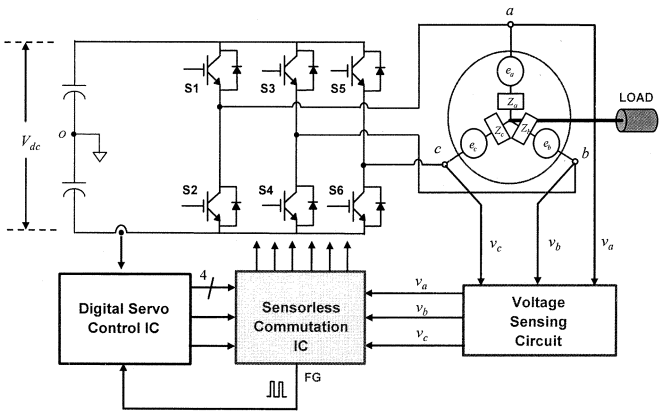



Fig. 1. Block diagram of a BLDCM servo control system with the proposed sensorless commutation IC.

There are many applications in using small motors (below 3 W) for speed or position control in consumer electronics, such as digital cameras, DVD players, image scanners, and electronics toys. Requirements in control performances of small motors will become more stringent in the future. A very tighten cost constraint imposes on the feasible solution for the control of small motors. DSP embedded or programmable logic based mixed-mode ASICs provide a possible solution for this issue.

Most conventional approaches in designing control ICs for small motors are using analog technology [7]. The advantage in using analog technology is low cost, however, suffers from limited functions. Programmability becomes important in modern motor control ICs in adaptation to various applications. Therefore, mixed-mode technology has been employed in design of today's motor control ICs. However, most of the commercial BLDCM control ICs are still fixed in structure and unable to be programmed [8]–[10].

The research goal of this paper is to design a sensorless commutation IC for BLDCMs by using mixed-mode IC design methodology. Fig. 1 shows the block diagram of a BLDCM speed control system using the proposed sensorless commutation IC. The overall control system consists of four major parts: a BLDCM with load, a pulse-width-modulation (PWM) inverter, a sensorless commutation IC, and a digital servo controller. The proposed sensorless commutation IC can generate accurate commutation signals for the BLDCM based on the modified back-EMF sensing principle, and can also generate the estimated speed to the digital servo controller for high performance speed regulation. Besides, the designed IC

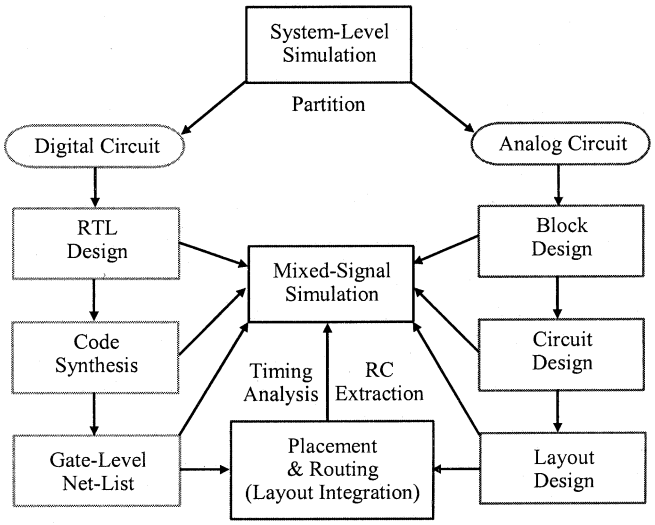



Fig. 2. Mixed-mode IC design flowchart.

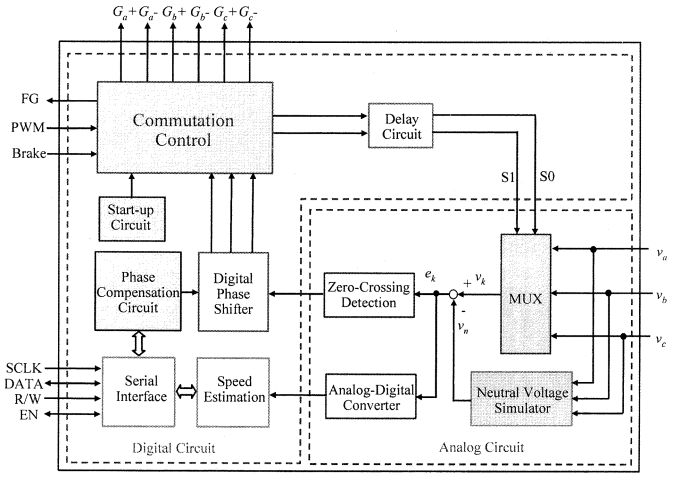



Fig. 3. Functional block diagram of the proposed sensorless commutation IC.

also provides a phase compensation function for efficiency optimization and flux-weakening control.

The organization of this paper is as follows. First, the mixed-mode IC design methodology is presented in Section II. Then, the sensorless commutation algorithm with the modified back-EMF sensing principle is detailed described in Section III. In Section IV, the realization issue of the proposed mixed-mode sensorless commutation IC is presented. Some simulation and experimental results are given in Section V to verify the effectiveness of the developed sensorless commutation IC. Finally, some concluding remarks are given in Section VI.

## II. Mixed-Mode IC Design Methodology

For a complicated system, the signal interface of each chip should be carefully designed to keep the system in normal operation and to make the system insensitive to noise. However, designing signal interface problems may take lots of time and may reduce the overall system reliability. The benefits of integrating analog and digital circuits using mixed-mode IC design methodology in a single chip are reducing parasitic problems, I/O driving loads, power dissipation, and chip size, and it can also simplify the signal interface for system integration. However, there exist some challenges in the system-on-a-chip (SoC) solution for digital motor control, such as high design complexity, high process complexity, signal coupling problems, and noise isolation problems. Using mixed-mode simulation techniques, which become an interest issue in recent years, can simulate these problems [11], [12]. Fig. 2 shows the top-down design flow chart of mixed-mode IC design methodology. In order to verify the system architecture before creating detailed design circuits, system-level simulation should be done firstly. After defining the system specifications, the system is separated into analog and digital circuits, which can be designed independently using simulation tools until the layout stage. During the layout stage, the analog and digital circuits are integrated, and the post-simulation is required to extract the time latency of each wire in the chip to complete the whole chip design.

## III. Sensorless Commutation Algorithm

Fig. 3 shows the functional block diagram of the proposed sensorless commutation IC, which consists of analog and digital circuits. The analog circuits include a back-EMF sensing circuit, a zero-crossing detection circuit, and a single channel analog to digital (A/D) converter. The digital circuits include a digital phase shifter, a phase compensation circuit, commutation control logic, and a speed estimator. The detailed sensorless commutation algorithm of the proposed IC is described in this section.

### A. Back-EMF Estimation

Assume the motor is in an electric balance condition, and the back-EMFs of the three phase windings are symmetrical. Three terminal voltages, $v_a$, $v_b$, and $v_c$, can be derived as

$$v_a = v_{an} + v_n = Ri_a + L\frac{di_a}{dt} + e_a(\theta_e) + v_n \quad (1a)$$

$$v_b = v_{bn} + v_n = Ri_b + L\frac{di_b}{dt} + e_b(\theta_e) + v_n \quad (1b)$$

$$v_c = v_{cn} + v_n = Ri_c + L\frac{di_c}{dt} + e_c(\theta_e) + v_n \quad (1c)$$

where $R$ and $L$ are the stator resistance and inductance, $v_{an}, v_{bn}$, and $v_{cn}$ are the phase voltages, and $v_n$ is the neutral voltage. $i_a$, $i_b$, and $i_c$ represent three phase currents, respectively. The three back-EMFs are $e_a$, $e_b$, and $e_c$, and $\theta_e$ is the electrical angle. From (1), the sum of three terminal voltages is

$$v_a + v_b + v_c = (v_{an} + v_{bn} + v_{cn}) + 3v_n. \quad (2)$$

For analyzing the effectiveness of the back-EMF estimation, the commutation from phase $a$-$b$ to phase $a$-$c$ is considered as an example. During the two-phase conducting period, two conducting phase currents are opposite and another one is zero, that is $i_b = -i_a$, $i_c = 0$. Therefore, from (1) and (2), the back-EMF of the nonexcited phase $c$ is

$$\begin{aligned} e_c(\theta_e) &= v_c - v_n \\ &= v_c - \frac{1}{3}\left[(v_a + v_b + v_c) - (e_a(\theta_e) + e_b(\theta_e) + e_c(\theta_e))\right]. \end{aligned} \quad (3)$$

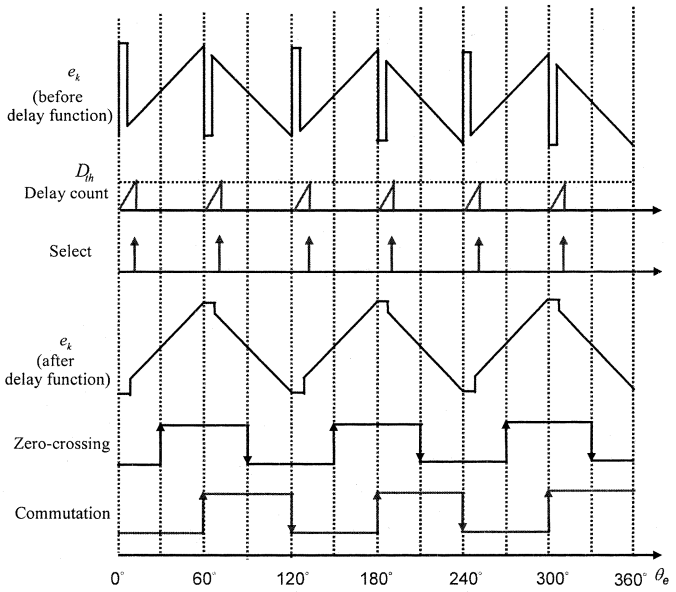



Fig. 4. Relationship between the estimated back-EMFs and the rotor position.

By simplifying (3), $e_c$ can be estimated as

$$e_c(\theta_e) = \frac{1}{2}\left[3v_c - (v_a + v_b + v_c) + (e_a(\theta_e) + e_b(\theta_e))\right]. \quad (4)$$

For an ideal trapezoidal back-EMF, $e_a(\theta_e) + e_b(\theta_e)$ is equal to zero. Hence, the nonexcited phase back-EMF can be fully estimated by (4) with only three terminal voltages. For the nonideal or distorted back-EMF [13], however, $e_a(\theta_e)$ is different from $-e_b(\theta_e)$, that is

$$e_a(\theta_e) + e_b(\theta_e) = e_n(\theta_e) \neq 0. \quad (5)$$

Due to this nonzero term, the back-EMF estimation algorithm in (4) would produce an electrical angle-dependent error, and cause a phase shift to the zero-crossing point of the real back-EMF. If the shapes of the back-EMFs can be known, this error can be compensated in advance. However, for unknown back-EMFs, this error would cause inaccurate commutation control. Therefore, a phase compensation circuit is realized in the proposed IC to provide the flexibility for on-line commutation phase correction, and some tuning strategies can be adopted [14], [15]. The detailed operation of the phase compensation circuit will be described in the following section.

During the commutation period, three phases are conducted until the decaying current reduces to zero. It should be noted that the estimation algorithm in (4) is only valid by assuming the nonexcited phase current is zero. Hence (4) would become a wrong estimation for back-EMFs during the three-phase conducting period. In this example, during the commutation from phase $a$-$b$ to phase $a$-$c$, the terminal voltage $v_b$ is equal to half dc-link voltage $(V_{dc}/2)$ due to the free-wheeling diode clamping effect. Hence, if (4) is applied for the estimation, then the estimated back-EMF of nonexcited phase b would be derived as

$$\hat{e}_b(\theta_e) = \frac{1}{2}\left[3v_b - (v_a + v_b + v_c) + e_n(\theta_e)\right] = \frac{V_{dc} + e_n(\theta_e)}{2}. \quad (6)$$

Obviously, $\hat{e}_b(\theta_e)$ differs from the real back-EMF $e_b(\theta_e)$. Since the back-EMF estimation can't be achieved during the commu-

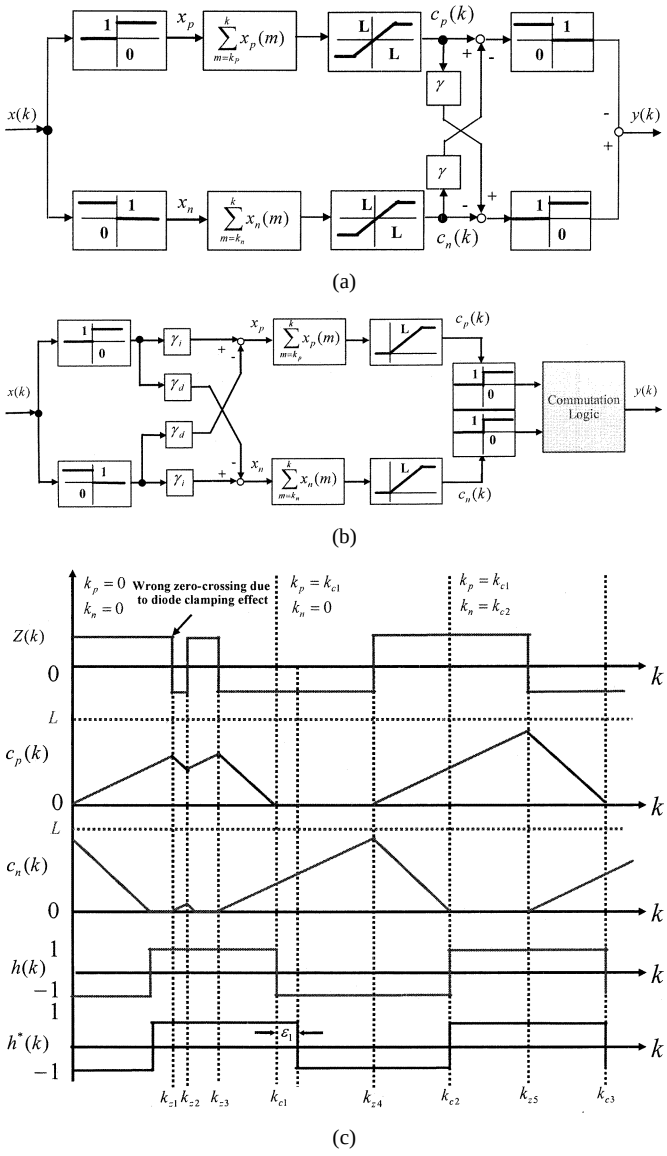



Fig. 5. Digital phase shifter. (a) FIPS [6]. (b) Modified FIPS. (c) Ideal operation waveforms of the proposed digital phase shifter.

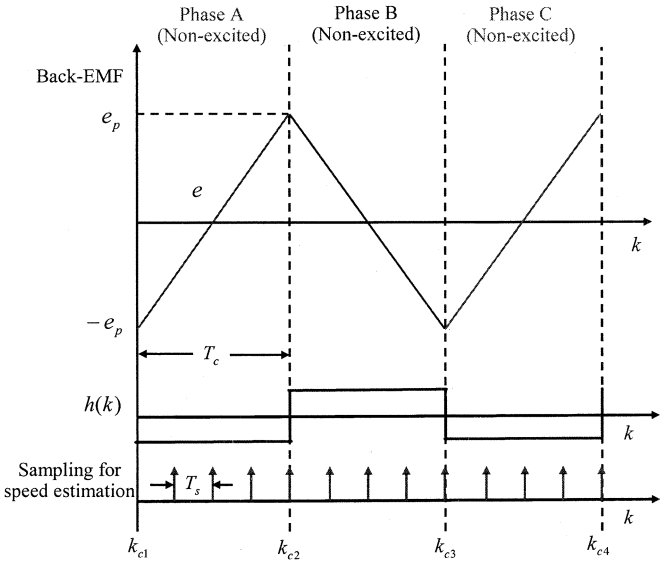



Fig. 6. Concatenate waveform of the ideal nonexcited phase back-EMFs.

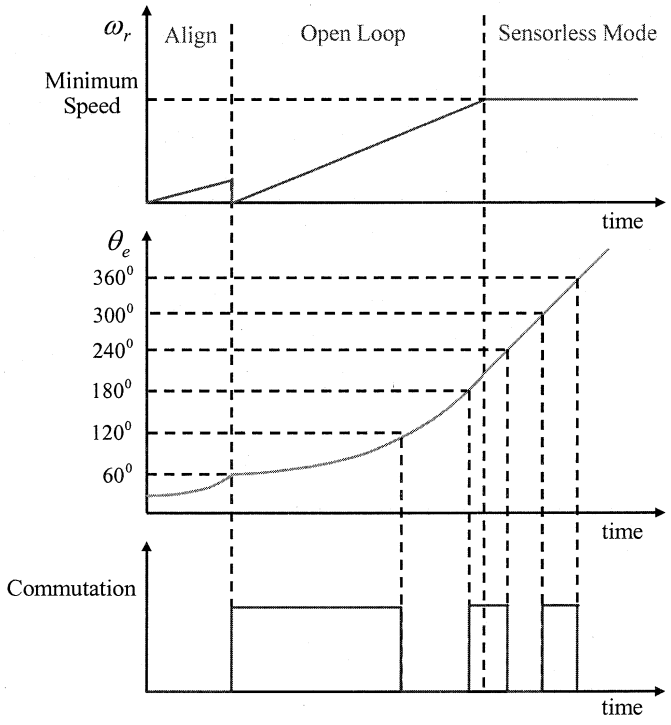



Fig. 7. Operation waveform of open loop starting procedure.

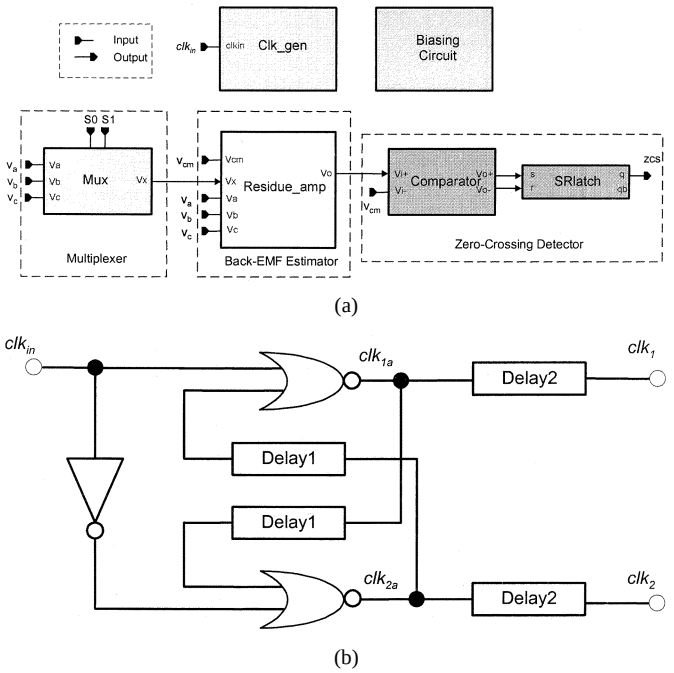



Fig. 8. (a) Circuit-level block diagram of back-EMF sensing and zero-crossing detection circuits. (b) Clock generator circuit.

tation period with only three terminal voltages, a delay circuit is realized in the proposed IC to mask the estimation for avoiding wrong zero-crossing detection during this period. Fig. 4 illustrates the typical waveforms of the estimated nonexcited phase back-EMF and the corresponding zero-crossing signal during two-phase conducting period and commutation period. It should be noted that the duration of the three-phase conducting period would depend on the operating conditions [16]. Therefore, the threshold value $D_{th}$ of the delay circuit as shown in Fig. 4 can be programmed according to required applications.

### *B. Digital Phase Shifter*

After detecting the zero-crossing signal of the estimated nonexcited phase back-EMF, an additional 30° phase shift is required to perform correct commutation. Conventionally, this phase shift is generated using a filter [1]. However, the phase lag resulted by the filter varies with motor speed; hence the accuracy of the sensorless commutation control depends on its rotating speed. In [6], a novel frequency-independent phase shifter (FIPS), which has been proven to be independent of input signal frequencies, has been proposed as shown in Fig. 5(a). Since the count values of $c_p(k)$ and $c_n(k)$ depend on the rotating speed, and the value of scaling factor $\gamma$ is less than one, a long bit-length divider is required at low speed operation to compute $\gamma c_p(k)$ and $\gamma c_n(k)$ precisely. However, designing a long bit-length divider in a single chip may increase the total chip size or decrease the overall performance. In this paper, a digital simplified-type FIPS, which only needs a simple multiplier instead of a long bit-length computation unit, is presented as shown in Fig. 5(b) to reduce the computation effort of FIPS. The counter $c_p(k)$ represents the duration for which the sampled signal $x(k)$ remaining positive. Similarly, the counter $c_n(k)$ represents the duration for which the sampled signal $x(k)$ remaining negative. The variables $\gamma_i$ and $\gamma_d$ denote the increasing and decreasing increments for the counters, respectively. Furthermore, the values of $c_p$ and $c_n$ are limited by a positive constant $L$ to avoid overflow condition at very low speed, therefore the functions of $c_p$ and $c_n$ can be written as

$$c_p(k) = \min\left\{\max\left[0, \sum_{m=k_p}^{k}\left(\frac{1+\mathrm{sgn}\,(x(m))}{2}\gamma_i - \frac{1-\mathrm{sgn}\,(x(m))}{2}\gamma_d\right)\right], L\right\} \quad (7)$$

$$c_n(k) = \min\left\{\max\left[0, \sum_{m=k_n}^{k}\left(\frac{1-\mathrm{sgn}\,(x(m))}{2}\gamma_i - \frac{1+\mathrm{sgn}\,(x(m))}{2}\gamma_d\right)\right], L\right\} \quad (8)$$

with

$$\mathrm{sgn}(x) = \begin{cases} 1, & \text{if } x \geq 0 \\ -1, & \text{if } x < 0 \end{cases} \quad (9)$$

where $\gamma_i$ is a programmable variable as the increasing increment for counters, and $k_p$ is the largest $k$, such that

$$c_p(k) - c_p(k-1) = 0 \quad (10)$$

and $k_n$ is the largest $k$, such that

$$c_n(k) - c_n(k-1) = 0. \quad (11)$$

To describe the basic operation of the proposed digital phase shifter, an ideal case of the periodic input signal is considered. Fig. 5(c) shows the operation waveforms. Assume that the input $x(k)$ in Fig. 5(b) is the zero-crossing signal $z(k)$ of the nonexcited phase back-EMF, and the output $y(k)$ is the corresponding commutation signal $h(k)$. $h^*(k)$ is the desired commutation

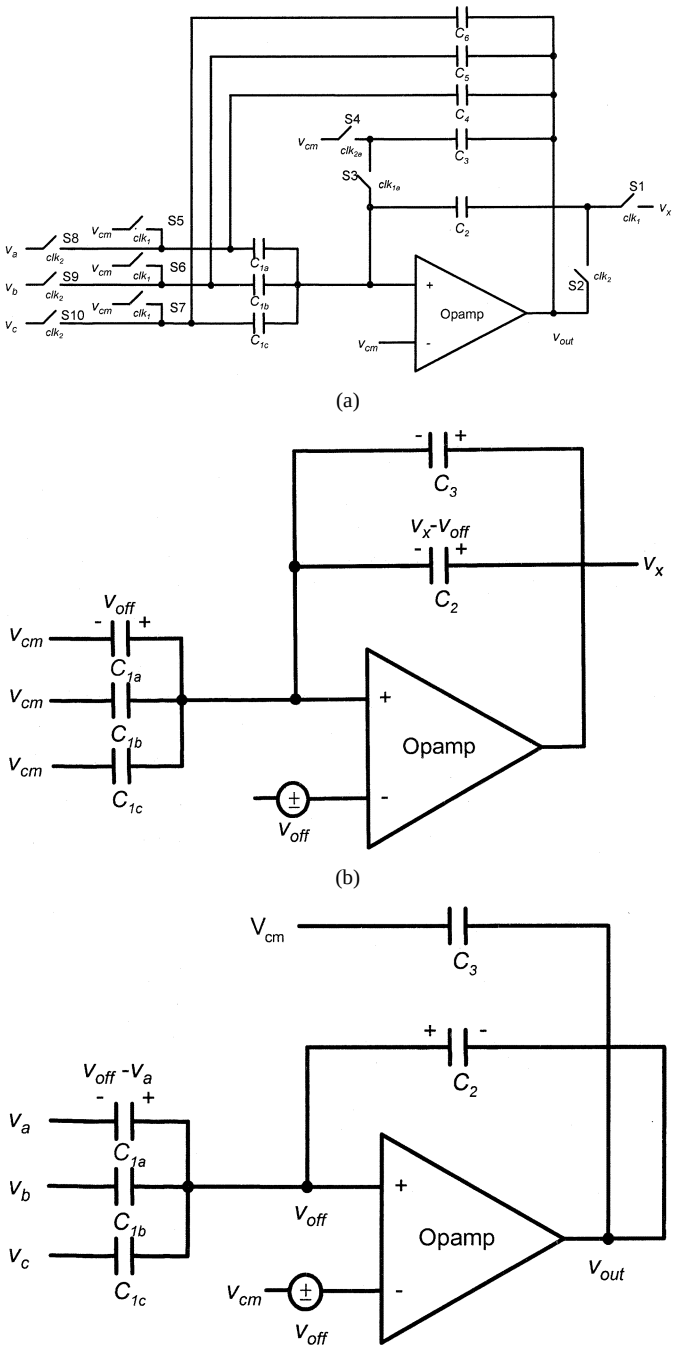



Fig. 9. Designed residue amplifier. (a) Schematic. (b) Reset operation mode. (c) Output operation mode.

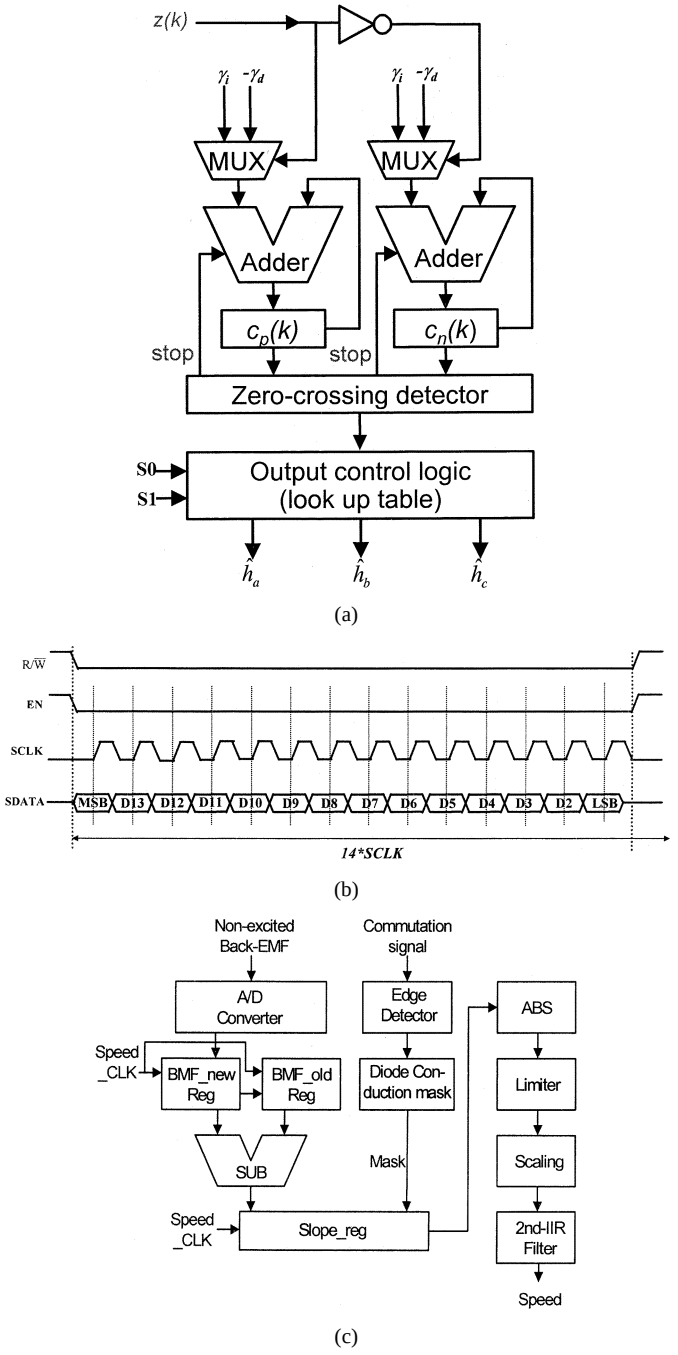



Fig. 10. Digital circuits. (a) Hardware-level diagram of the digital phase shifter. (b) Data transmission waveforms of the serial interface. (c) Hardware-level diagram of the speed estimation circuit.

signal. Also, $\gamma_d$ is set as two-times of the increasing increment $\gamma_i$ to make the phase shift equal to 30° from $z(k)$. $k_{zn}$ denotes the time when the $n$th zero-crossing of input signal $z(k)$ occurs, and $k_{cn}$ denotes the time when the $n$th commutation occurs. A wrong zero-crossing signal is generated at $k_{z1}$ and $k_{z2}$ for examining the robustness of the proposed phase shifter. A phase shift error $\varepsilon_1$ would occur at $k_{c1}$ due to the error signals, but would be vanished at next commutation instant $k_{c2}$. By analyzing the operation waveforms, we can find that the proposed digital phase shifter not only preserves the benefits of FIPS, but also replaces the long bit-length computation unit with a simple multiplier.

### C. Phase Compensation

In order to produce maximum torque at low-speed operation for BLDCMs, the phase currents are required to be aligned in phase with the back-EMF waveforms, i.e. phase shift between zero-crossing of the nonexcited phase back-EMF and real commutation signal is 30° [17]. However, a commutation phase error may exist due to the phase-lag of low-pass filtering, noise, and nonideal effect of the estimated back-EMF. In this paper, the modified digital phase shifter provides a phase compensation capability for adjusting excitation angles for BLDCM com-

TABLE I
PROGRAMMABLE PARAMETERS

| | Description | Address | Format | Range | Unit |
|---|---|---|---|---|---|
| $D_{th}$ | Threshold value for delay circuit | 00 | RW-10 | -2048~2047 | $\mu$s |
| $\gamma_i$ | Counter increasing increment | 01 | RW-10 | 0~4095 | - |
| $\Delta\theta$ | Phase advanced angle for phase compensation | 10 | RW-0 | -300~300 | 0.1 degree |
| $\hat{\omega}_r$ | Estimated speed | 11 | R | -2048~2047 | rad/sec |

(Note: R = read access, W = write access, -0 = value after reset)

mutation control. The phase compensation circuit can be easily implemented by changing the decreasing slew rate $\gamma_d$ with

$$\gamma_d = \frac{60}{30 - \theta_{LP} - \boldsymbol{\Delta\theta}}\gamma_i \tag{12}$$

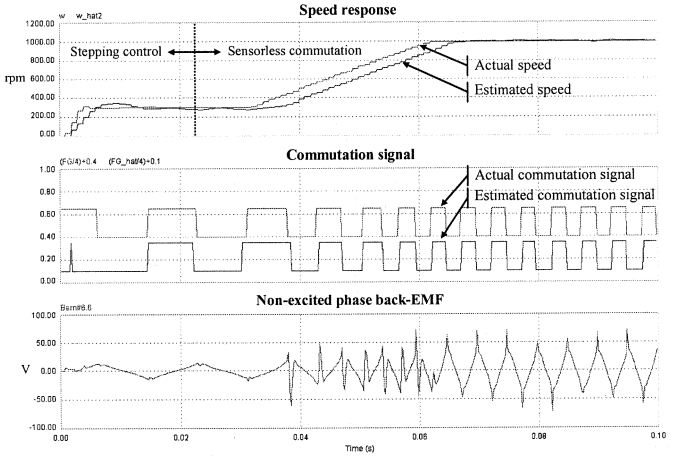
where $\theta_{LP}$ is the phase lag due to the low-pass filtering of the terminal voltages, and $\Delta\theta$ is the desired advanced angle. Since $\theta_{LP}$ would vary with motor speed, the phase-lag effect due to the low-pass filters can be determined by using the estimated speed to compensate the phase error. In order to generate precise phase shift, an accurate speed estimation method is presented in the following section. Besides, the designed phase compensation circuit can be also used for flux-weakening control by advancing the phase angle of excitation points relative to the back-EMF waveforms at high-speed operation [18].

### D. Speed Estimation

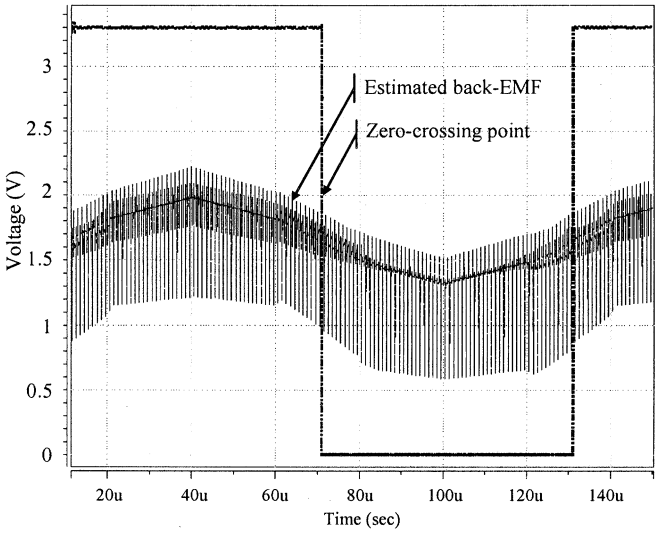
The accuracy of speed estimation is very crucial for closed-loop speed control. Since the commutation signal $h(k)$ can be estimated with the presented algorithm, the time interval $T_c$ between two commutations can be easily calculated as shown in Fig. 6. Hence the rotating speed can be estimated as [14]

$$|\widetilde{\omega}_r| = \frac{120}{P} f_e = \frac{120}{6PT_c} = \frac{20}{PT_c} \tag{13}$$

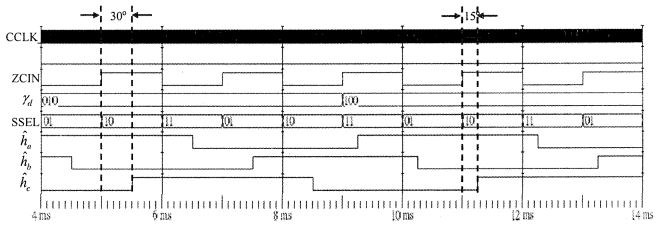
where $\widetilde{\omega}_r$ is the estimated rotating speed from commutation signals, $P$ denotes the number of rotor poles, and $f_e$ is the electrical rotating frequency. However, this method can only update the estimated speed when commutation occurs, and works poorly at low-speed operations because of no information between two commutations. In order to improve the speed estimation at low-speed operation, this paper proposes a novel speed estimation technique, which can estimate the instantaneous speed at each sampling instant of speed control loop.




(a)




(b)




(c)

Fig. 11. Simulation results. (a) System-level simulation result of proposed sensorless commutation algorithm. (b) Back-EMF sensing and zero-crossing detection circuits. (c) Digital phase shifter and phase compensation function.

Fig. 6 also presents a concatenation waveform of the ideal nonexcited phase back-EMF signal $e(k)$. The rotating speed can be also estimated from the peak value $e_p$ of the back-EMF as

$$|\hat{\omega}_r| = \frac{|e_p|}{K_E} \tag{14}$$

where $K_E$ is the back-EMF constant of a BLDCM. The estimation algorithm in (14) suffers from a similar problem as (13), because the peak value $e_p$ can be only actually known at each commutation instant. However, $e_p$ can be predicted from the

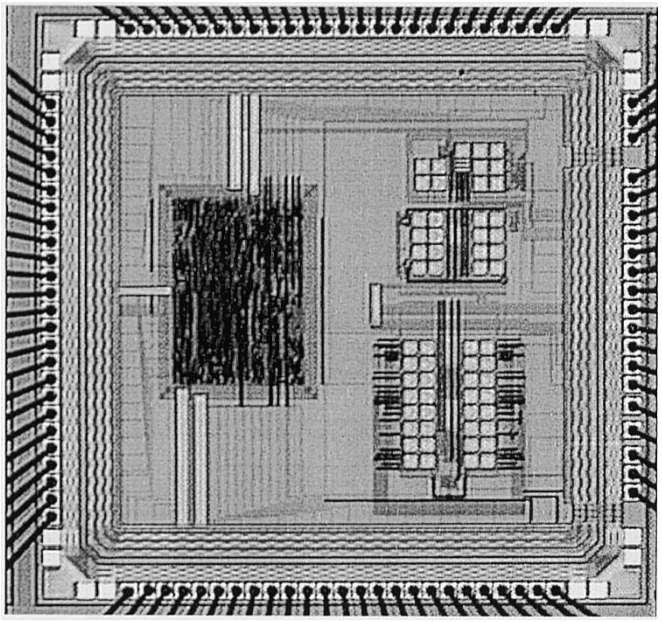


Fig. 12. Die microphotograph of the developed sensorless commutation IC.

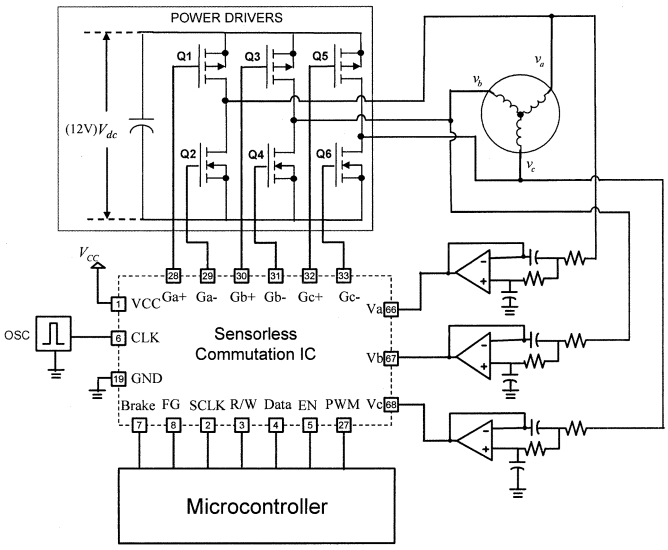



Fig. 13. Detailed evaluation of the drive prototype exploiting the proposed IC.

TABLE II
MOTOR PARAMETERS

| 3-phase brushless dc motor | |
|---|---|
| Type | Y-connection, 12 poles |
| Rated voltage | 12 V |
| Rated speed | 8000 rpm |
| Stator resistance | 0.98 Ω |
| Stator inductance | 0.3 mH |
| Rated stator current | 1.4 A |
| Maximum stator current | 4.4 A |
| Rotor inertia | 0.0121 mN-m$^2$ |
| Torque constant | 0.0074 N-m/A |

sampled back-EMF signal $e(k)$ with sampling period $T_s$ between two commutations. The average slope $\Delta e_{avg}$ of $e$ between two commutations can be derived as

$$\Delta e_{avg} = \frac{e_p(k_{c2}) - e_p(k_{c1})}{T_c(k_{c2})} T_s \tag{15}$$

where $k_{cn}$ denotes the time when the $n$th commutation occurs, and $T_c(k_{cn})$ is the duration between $n$th and $(n-1)$th commutations. From the speed estimation of (13) and (14), (15) can be further derived as

$$\frac{\Delta e_{avg}}{T_s} = \frac{K_E[|\hat{\omega}_r(k_{c2})|\mathrm{sgn}(e_p(k_{c2})) - |\hat{\omega}_r(k_{c1})|\mathrm{sgn}(e_p(k_{c1}))]}{\frac{20}{P|\widetilde{\omega}_r(k_{c2})|}}. \tag{16}$$

As illustrated in Fig. 6, $e_p(k_{c1})$ is negative and $e_p(k_{c2})$ is positive. Therefore (16) can be expressed as

$$\hat{\omega}_r(k_{c2}) = \frac{20}{K_E P T_s \widetilde{\omega}_r(k_{c2})} \Delta e_{avg} - \hat{\omega}_r(k_{c1}). \tag{17}$$

When the sampling instant is between two commutations, i.e. $k_{c1} < k < k_{c2}$, the speed estimation algorithm is derived as

$$\hat{\omega}_r(k) = \frac{20}{K_E P T_s \widetilde{\omega}_r(k)} \Delta e(k) - \hat{\omega}_r(k_{c1}) \tag{18}$$

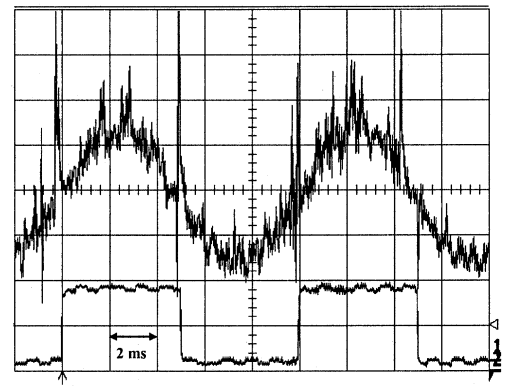
where $\widetilde{\omega}_r(k)$ is equal to $\widetilde{\omega}_r(k_{c1})$, because no commutation occurs during this period. From the observation of (18), the estimated speed $\hat{\omega}_r(k)$ can be updated at each sampling instant of the speed control loop by differentiating the nonexcited phase back-EMF.

In general, the condition for estimating actual rotating speed $\omega_r(k)$ in the proposed IC is described as (19) shown at the bottom of the page, where $d$ is the rotating direction which can be determined from the sequence of the estimated commutation signals. By using (19), the instantaneous speed at each sampling instant $T_s$ can be estimated to improve the dynamic response of the closed-loop speed control.

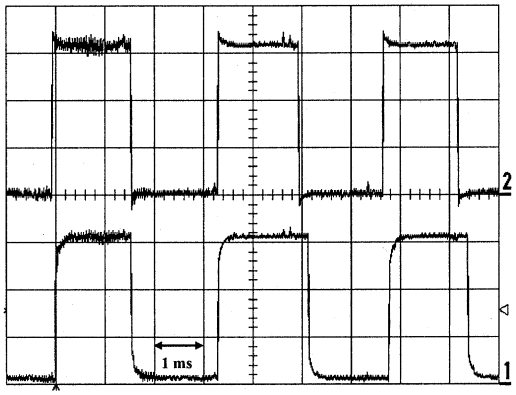
### E. Starting Procedure

Since the back-EMF is proportional to the rotating speed, and is not generated at standstill, a proper starting procedure should be applied for sensorless commutation control. In this paper, an open loop ramping control scheme is adopted to accelerate the motor speed to a certain speed level. As long as the back-EMF is sufficient large for estimating the commutation signal accurately, the control mode may be changed from stepping control to sensorless closed-loop control. Fig. 7 illustrates the motor starting procedure. First, the rotor would be aligned from an unknown position to a certain position by applying a specified

$$\omega_r(k) = \begin{cases} d\widetilde{\omega}_r(k) = \frac{20d}{PT_c(k_{cn})}, if T_s \geq T_c(k_{cn}), k > k_{cn} \\ d\hat{\omega}_r(k) = \frac{20d}{K_E P T_c \widetilde{\omega}_r(k_{cn})} |\Delta e(k)| - \hat{\omega}_r(k_{cn}), if T_s < T_c(k_{cn}), k > k_{cn} \end{cases} \tag{19}$$




(a)




(b)

Fig. 14. Measured waveforms of steady-state speed operation at 1000 rpm. (a) Upper trace: calculated phase voltage of phase A (0.1 V/div). Lower trace: detected zero-crossing signal (2 V/div). (b) Upper trace: detected zero-crossing signal (2 V/div). Lower trace: estimated commutation signal (2 V/div).

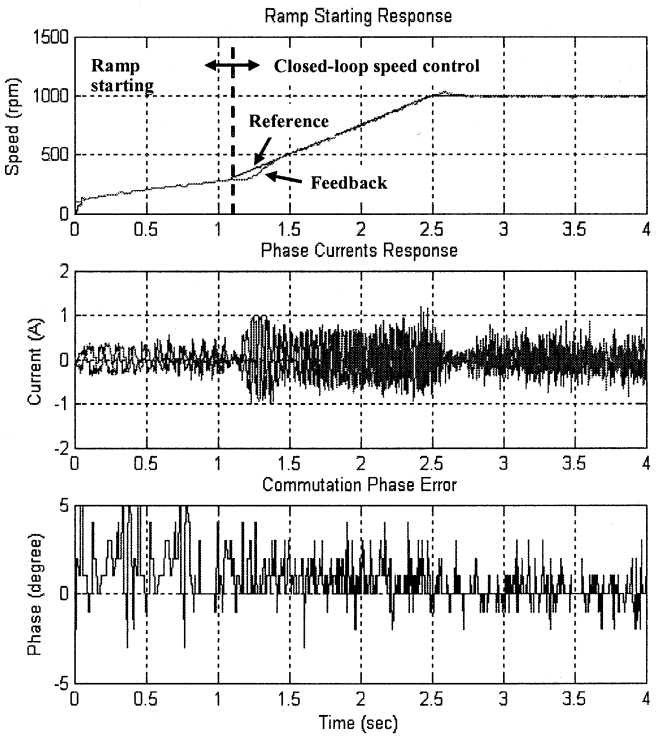



Fig. 15. Ramp starting control response from standstill to 1000 rpm.

voltage vector. Then a current controller is incorporated with the designed stepping control circuit to apply a fixed current $I_{st}$ for the BLDCM. Since the back-EMFs are quite small during the starting period, constant current control can be achieved. Therefore, the BLDCM can be accelerated with a fixed rate as shown as

$$\omega(t) \cong \frac{K_T I_{st} - T_L}{J_M + J_L} t \tag{20}$$

where $K_T$ is the torque constant of the BLDCM, and $T_L$ is the load torque. $J_M$ and $J_L$ represent the rotor inertia and load inertia of the BLDCM, respectively. It should be noted that fixed acceleration can be achieved under different load conditions by applying corresponding $I_{st}$. Hence the electrical angle can be estimated to generate commutation signals during the stepping control mode as

$$\theta_e(t) = \frac{P}{4} \frac{K_T I_{st} - T_L}{J_M + J_L} t. \tag{21}$$

## IV. Realization Issues

### A. Back-EMF Sensing and Zero-Crossing Detection Circuits

Fig. 8(a) shows the circuit-level block diagram of the back-EMF sensing and zero-crossing detection circuits, which are realized by using analog IC design technology. The clock generator is used to generate two nonoverlap clocks $clk_1$ and $clk_2$, and two phase-advanced clocks $clk_{1a}$ and $clk_{2a}$ for the residue amplifier as shown in Fig. 8(b). The bias circuit is used to provide a regulated bias voltage for the analog circuits, and the multiplexer is used to select the nonexcited phase terminal voltage.

Fig. 9(a) shows the schematic of the designed residue amplifier, which is used to estimate the nonexcited phase back-EMF. The design concept of the residue amplifier is from the capacitive reset gain circuit [19], which has some features: the offset compensation ability, input noise insensitivity, and high-speed computational ability. The detailed operation is described below. When the $clk_1$ and $clk_{1a}$ are at high state, only the switches $S_1$, $S_3$, $S_5$, $S_6$, and $S_7$ would be turned on as shown in Fig. 9(b). During this stage, the offset voltage of the operational amplifier $v_{off}$ is stored in the capacitor $C_{1a}$, $C_{1b}$, and $C_{1c}$, and the difference voltage between the input voltage $v_x$ and offset voltage $v_{off}$ is stored in the capacitor $C_2$ as the initial charge in the next stage. It should be noted that the deglitching capacitor $C_4$, $C_5$, and $C_6$ are used to provide negative feedback path to keep the output voltage when all switches are turned off, and can be neglected in analyzing the operation. When the $clk_2$ and $clk_{2a}$ are at high state, only the switches $S_2$, $S_4$, $S_8$, $S_9$, and $S_{10}$ would be turned on as shown in Fig. 9(c). The total charge of $C_2$ can be expressed as

$$Q(C_2) = C_2(v_x - v_{off}) - (C_{1a}v_a + C_{1b}v_b + C_{1c}v_c). \tag{22}$$

Then the output voltage $v_{out}$ can be derived as

$$v_{out} = v_{off} + (v_x - v_{off}) - \left(\frac{C_{1a}}{C_2}v_a + \frac{C_{1b}}{C_2}v_b + \frac{C_{1c}}{C_2}v_c\right). \tag{23}$$

By properly choosing the values of $C_{1a}$, $C_{1b}$, $C_{1c}$, and $C_2$, the output voltage can be simplified as

$$v_{out} = v_x - \frac{1}{3}(v_a + v_b + v_c). \tag{24}$$

By comparison to (4), only a constant scaling factor is required to estimate the nonexcited phase back-EMF during this stage. Besides, from (23), we can find that the offset voltage of the operational amplifier doesn't affect the output voltage of the residue amplifier.

The estimated nonexcited phase back-EMF from the residue amplifier is then converted into a binary signal by using a hysteresis comparator and a SR latch. The threshold level of the comparator is set as 50% of full-scale, and the hysteresis band of the comparator can be properly specified to prevent oscillations due to noise and slow varying edges with slow rotating speed.

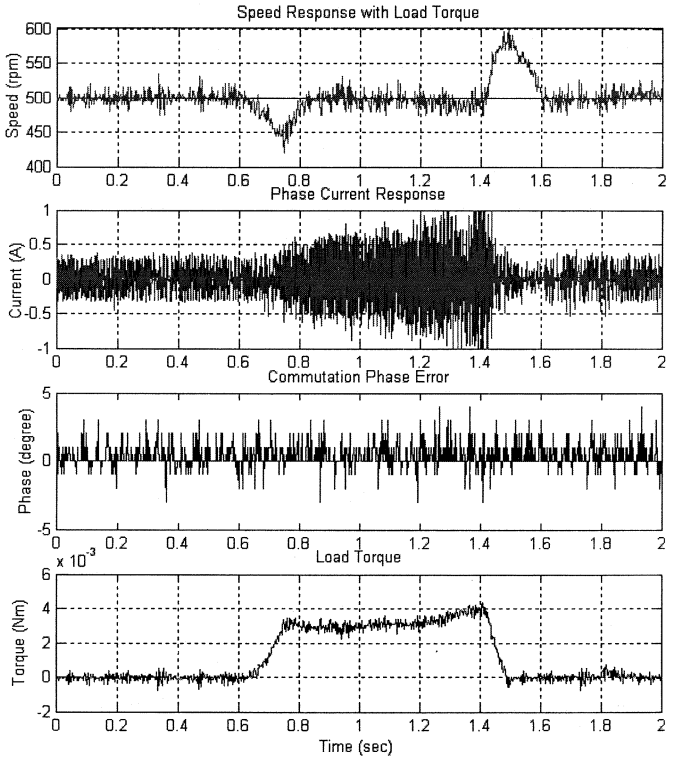
### *B. A/D Converter*

Since the speed estimation algorithm processes in the digital circuits, an analog-to-digital (A/D) converter is needed to convert the analog nonexcited phase back-EMF signal into a digital signal. From the standpoint of total chip size and power dissipation, an algorithmic A/D converter is adopted and realized in the proposed sensorless commutation IC [20]. The specifications of the realized A/D converter are single-channel, 12-b resolution, and 20 kHz sampling frequency. The features of the algorithmic A/D converter are insensitive to capacitor-ratio accuracy, finite gain, and offset voltage of operational amplifiers.

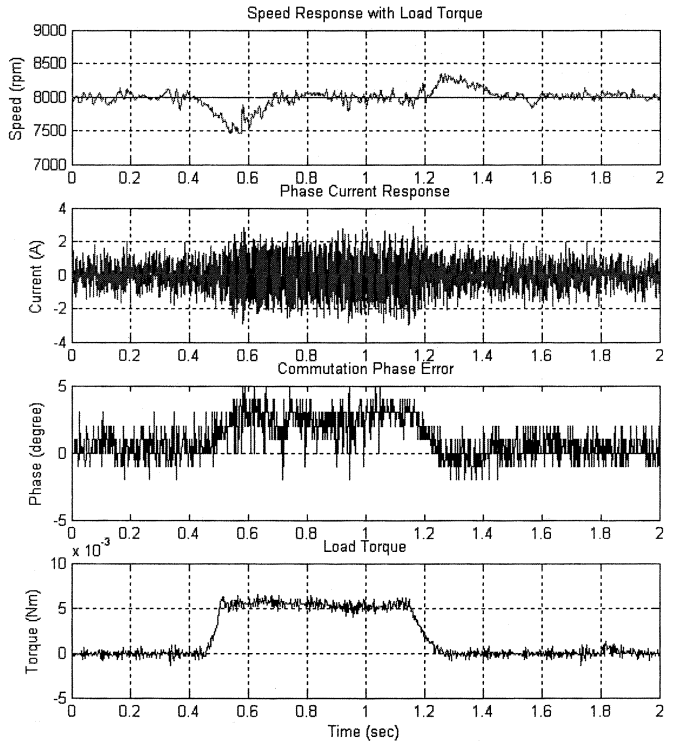
### *C. Digital Phase Shifter and Speed Estimation*

Fig. 10(a) shows the hardware-level diagram of the digital phase shifter. The input signal of the digital phase shifter is the zero-crossing signal, which is generated from the analog zero-crossing detection circuit, and is used to select the counting increments for two 16-b up/down counters. As long as the count value of each counter is less than zero, the counter is reset to zero. In the meantime, the output control logic is triggered to generate a new commutation signals based on the pre-defined table. Since the counting increment $gi$ should be carefully specified for different applications, a serial interface is designed for programmability. In the proposed IC, the default sampling rate of the digital phase shifter is 200 kHz, and the up counting increment is 20. That is, the designed digital phase shifter can work from 100 rpm to 333 krpm for a 12-pole spindle motor, and the resolution for the phase compensation is 0.8°. Fig. 10(b) illustrates data transmission waveforms of the serial interface. The serial interface is set to trigger on the falling edge of the enable signal (EN), and needs 14 clocks for synchronization to complete a 12-b data transmission. The first 2 b of one transmission are used to indicate the address of the parameter as listed in Table I.

Fig. 10(c) shows the hardware-level diagram of the speed estimation circuit. The slope of the nonexcited phase back-EMF, which can be read out from the A/D converter, is calculated with 20 kHz sampling rate. In order to avoid wrong estimation due to the free-wheeling diode clamping effect as described in Section III, a mask function is realized for back-EMF estimation circuits as well as the speed estimation circuit. By scaling and filtering the calculated slope with a 500 Hz second-IIR filter, a smooth speed feedback can be estimated and can be read out from the serial interface with a microcontroller.




(a)




(b)

Fig. 16. External load tests. (a) At low speed operation (500 rpm). (b) At rated speed operation (8000 rpm).

### D. Physical Layout

For mixed-mode IC layout, one important thing should be considered that the large signals from digital circuits might couple to the analog circuits to affect the accuracy of the analog signals and the biasing voltage. Some procedures must be done in preventing signal coupling in a mixed-mode circuit. Add guard rings to separate sensitive analog circuits from noisy circuits. Use independent power supplies for analog and digital circuits. The power supplies for the analog circuits should be well regulated. Analog circuits should be routed away from the high-frequency clock traces of the digital circuits.

## V. Simulation and Experimental Results

Some simulations are carried out to verify the behaviors of the proposed IC. Fig. 11(a) shows the system-level simulation result of the proposed sensorless commutation algorithm from standstill to 1000 rpm. From this figure, the commutation signals can be estimated accurately during both transient and steady state after stepping control mode. Besides, instantaneous speed estimation can be achieved by using the proposed speed estimation algorithm. Fig. 11(b) shows the simulation result of back-EMF sensing and zero-crossing detection circuits. Only one terminal voltage is shown in this simulation. Because of the charge transferring effect of the residue amplifier, the estimated back-EMF signal needs a little settling time to the final value at each clock. Besides, since the common mode voltage for the residue amplifier is half of supplied voltage $V_{DD}$, the threshold voltage for the zero-crossing detection circuit is $V_{DD}/2$ instead of zero. Fig. 11(c) shows the simulation result of digital phase shifter and phase compensation function. By changing the value of $\gamma_d$, the phase shift can be adjusted according to (12).

The experimental chip of the proposed sensorless commutation IC was designed and fabricated by using a standard 0.35 $\mu$m single-poly four-metal CMOS process. The die microphotograph is shown in Fig. 12. The total chip area is about 2.6 mm * 2.6 mm, and the power consumption is about 110 mW with 3.3 V operation. Fig. 13 shows the detailed practical evaluation of the drive prototype exploiting the proposed IC. By incorporating the sensorless commutation IC with a microcontroller, closed-loop speed control can be accomplished with the estimated speed generated from the designed IC. The experimental results are obtained by applying the proposed sensorless commutation IC to control a high-speed spindle motor for DVD players. The motor parameters are listed in Table II.

Fig. 14 shows the experimental results of steady-state speed operation at 1000 rpm. From the results, the nonexcited phase back-EMFs of the spindle motor can be successfully estimated using analog circuits, and the accurate commutation signal can be obtained using digital circuits. Fig. 15 shows the experimental result of a ramp starting control response from standstill to 1000 rpm. Constant acceleration can be achieved during the starting control mode by applying a fixed current for linear ramping control. The minimum controllable speed is set as 300 rpm (4% of the rated speed), and the minimum calculated speed is 100 rpm due to finite bit-length effect in speed estimation. Fig. 16 shows the external load tests at low

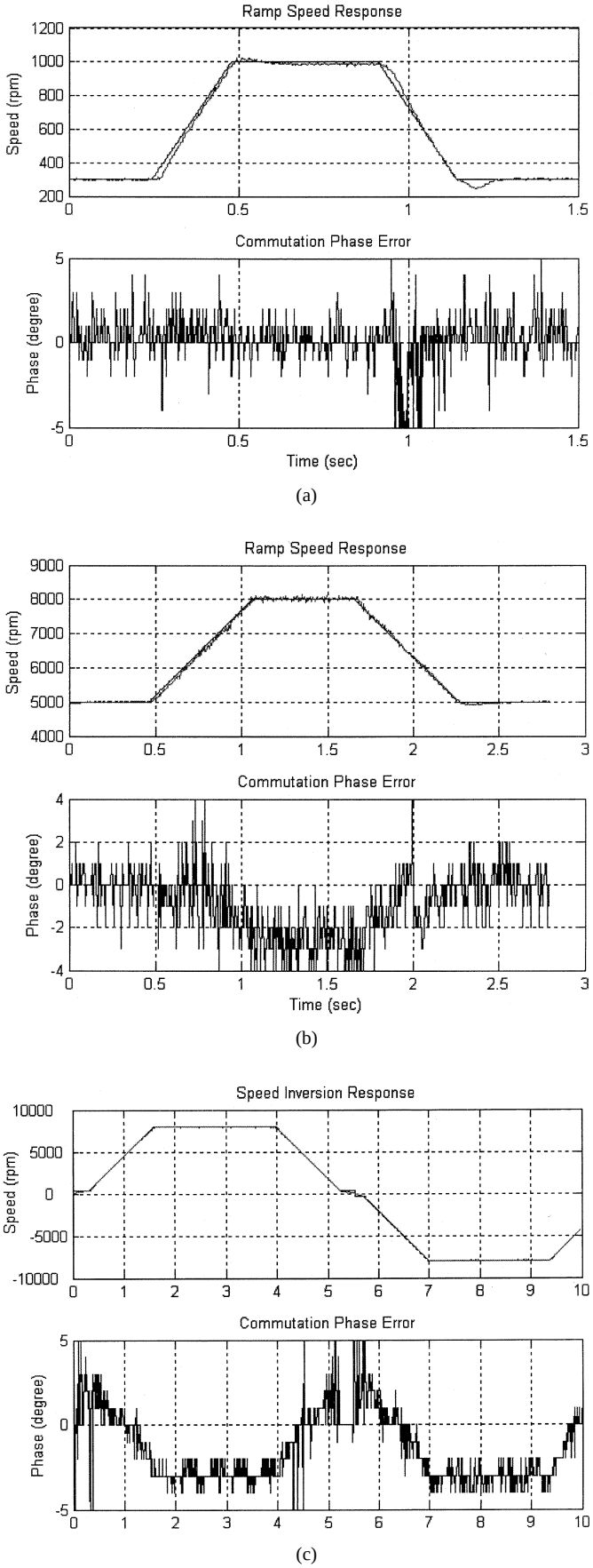



Fig. 17. Ramp speed control performance. (a) Low speed operation from 300 to 1000 rpm. (b) High speed operation from 5000 to 8000 rpm. (c) Ramp speed control from zero to 8000 rpm in both directions.

and rated speed operations. The commutation phase error between the estimated commutation and the real one is less than 5°. Hence accurate commutation control can be achieved under different load conditions.

Fig. 17 shows the ramp speed control and speed inversion performance. Wide speed control range can be obtained from 300 to 8000 rpm, and the commutation phase error is controlled to be less than 5°. It should be noted that the speed inversion response in Fig. 17(c) is obtained by switching the control mode to the open-loop stepping mode while the speed feedback is below to the minimum controllable speed (300 rpm).

## VI. Conclusion

This paper has presented the design and implementation of a programmable sensorless commutation IC for BLDCMs in applications to DVD-RAM. We propose a digital phase compensation scheme to reduce commutation phase error during low speed operation. In order to improve the signal-to-noise ratio when operating in low speed range, analog circuit has been used in detecting the low-level back EMF voltages. This sensorless commutation IC has been implemented by using a standard 0.35-$\mu$m single-poly four-metal CMOS process with mixed-mode IC design methodology. This sensorless commutation IC can be incorporated with a low-cost general-purpose microcontroller to provide a simple, compact, low-cost, and effective solution for BLDCM drives in many applications. Experimental results show a wide speed control range from 300 to 8,000 rpm has been achieved.

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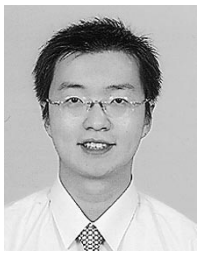
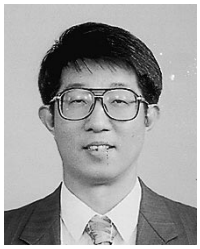


**Kuang-Yao Cheng** (S'01) was born in Taipei, Taiwan, R.O.C., in 1977. He received the B.S. degree in electrical engineering from National Sun Yat-Sen University, Kaohsiung, Taiwan, in 1999 and is currently pursuing the Ph.D. degree in electrical and control engineering at National Chiao Tung University, Hshinchu, Taiwan.

His research interests are in the areas of brushless dc motor control, sensorless algorithm design, digital controller realization, and intelligent optimization techniques.



**Ying-Yu Tzou** (S'81–M'88) was born in Taiwan, R.O.C., on February 13, 1956. He received the B.S. and M.S. degrees in control engineering and the Ph.D. degree in electrical engineering from National Chiao Tung University, Hsinchu, Taiwan, in 1978, 1983, and 1987, respectively.

From 1980 to 1981, he was with the Electronic Research and Service Organization (ERSO), Industry Technology Research Institute (ITRI) as a Design Engineer in the Control System Department. From 1983 to 1986, he was with Microtek Automation, Inc., as a Project Manager for the development of a computer numerical controller (CNC) for machine tools. He is currently a Professor at the Department of Electrical and Control Engineering, National Chiao Tung University, and also serves as an Industrial Consultant for many local power electronics and automation companies. His special interests now are sensorless ac drives, intelligent UPS, PV Inverters, FPGA-based control ICs for motor drives, high-speed digital system design, and DSP applications in power electronics and motion control.