Scanning the Issue

Special Issue on Nanoelectronics and Nanoscale Processing

Nanotechnology has become increasingly mature to produce profound impacts in many aspects of our lives, in industry, medicine, scientific research, aerospace applications, business, and education. As the fabrication technology continues its rapid progress in the nanometer regime, the nanoelectronics era has arrived in the early 21st century. While the feature size of manufactured devices is further scaled down, new nanostructures or nanodevices in the scale of 0.1–50 nm are under aggressive development with the promise to supplement or overtake the real-world impacts of known silicon technologies. With the rapid developments in manufacturing technology and underlying principles of physics/chemistry/biology of nanodevices/nanostructures, advanced research on the integration of millions or even billions of these tiny devices into low-voltage, low-power, and ultrahigh-frequency gigascale nanosystems has been very intense. Meanwhile, design of nanoelectronics and/or nanoscale processing/computing systems as well as biological devices using quantum/novel phenomena is being explored. The research on nanoelectronics and that on gigascale systems are closely linked. Both present exciting new challenges and opportunities to scientists and practicing engineers.

It has been several years since the prior Special Issue of the PROCEEDINGS OF THE IEEE on nanometer-scale science and technology was published in 1997. There have been numerous new developments and achievements in recent years in nanotubes, nanoelectronics, nanoelectromechanical systems (NEMS), and the associated circuits and signal/data processing architecture. Thus, it is timely to organize a Special Issue on nanoelectronics and nanoscale processing to share the vast amount of knowledge accumulated in this fast-growing field.

According to information provided by the IEEE Nanotechnology Council, the IEEE's focus on nanotechnology intensified in 2000 when the IEEE Nanotechnology Committee was established. The Committee was elevated to the Council status in February 2002 under Division 1—Circuits and Devices. The Nanotechnology Council is composed of 19 member societies. The first issue of IEEE TRANSACTIONS ON NANOTECHNOLOGY was published in March 2002, and the annual IEEE Nanotechnology Conference is a major forum for researchers to exchange new ideas and findings.[1]

The research activities in nanotechnology span many specialty areas and generally are highly cross disciplinary. They have attracted growing interest from researchers and scientists, as well as engineers and investors in governmental laboratories, universities, and leading industrial institutions all over the world. This special issue is composed of two highlight papers and 15 focused papers that cover key issues of nanotechnology, from overview/fundamentals on nanotechnology, nanotubes research, through self-assembled quantum dots array to interconnect/circuits/architecture of electronic and electromechanical nanosystems. In addition, the ethics issues in nanotechnology are also addressed with visionary views.

I. TWO HIGHLIGHT PAPERS

In "The Highlights in the Nano World," C.-Y. Chang, President of National Chio Tung University, Hsin-chu, Taiwan and International Member of U.S. National Academy of Engineering, touches on key technologies and also strongly advocates for further investment in education in the nanotechnology era. He first describes spintronics, which combines the electronic charge and spin in operation, then magnetic random access memory (MRAM) and quantum devices are presented. The outreach of nanotechnology into biology will produce fruitful research results in the next several years, and is covered in detail in this paper. Existing investment in nanotechnology education in the U.S. and other regions is discussed. One novel approach taken by National Chiao Tung University is to cooperate with the University of California, Berkeley, in order to participate in the National Nanotechnology Infrastructure Network (NNIN) in the United States. This joint effort can serve as a role model to inspire other academic institutions to be innovative in sharing the resources.

C.-G. Hwang, President of the Memory Division at Samsung Electronics Co., Seoul, Korea, presents a new

Digital Object Identifier 10.1109/JPROC.2003.818331

[1]For additional information on the Nanotechnology Council, please visit http://ewh.ieee.org/tc/nanotech/.

memory growth model based on nanoscale semiconductor technologies in "Nanotechnology Enables a New Memory Growth Model." For personal computers, DRAM and SRAM semiconductor memories are highly demanded. However, for portable electronic devices, the NAND Flash memory will be the driving force due to the multibit-cell capability and easy-to-scale property. Various sub-90-nm memory technologies and a roadmap to the year 2010 are highlighted. The famous Moore's Law predicts that the memory density will be doubled in 1.5 years, while the new growth model pioneered by C.-G. Hwang clearly indicates the doubling of NAND Flash memory density every year.

II. Nanotubes

In the paper "Carbon Nanotube Electronics," by P. Avouris *et al.*. the authors evaluate the potential of carbon nanotubes (CNTs) as the basis for a new nanoelectronic technology. After briefly reviewing the electronic structure and transport properties of CNTs, they then focus on the fabrication and performance characteristics of CNT field-effect transistors (CNTFETs). Comparison of the CNTFET characteristics with those of analogous silicon devices shows that CNTFETs are very competitive with state-of-the-art conventional devices. They also discuss the switching mechanism of CNTFETs and show that it involves the modulation by the gate field of potential energy barriers at the metal–CNT junctions. The potential for integration is demonstrated by fabricating a logic gate alongside a single nanotube molecule.

One of the ultimate limits of nanotechnology is molecular electronics, where devices may consist of individual molecules. Before this can be achieved, experimental methods to probe the electronic characteristics of single molecules must be explored and a theoretical understanding of how electrons traverse and interact with these molecules must be acquired. The paper by B. A. Mantooth and P. S. Weiss, "Fabrication, Assembly, and Characterization of Molecular Electronic Components," is focused on determining the electronic characteristics, mechanisms of action, and possibilities of single-molecule devices. The most recent methods and theories used to probe the electronic characteristics of the leading potential molecular electronics components are discussed. The authors use scanning probe methods to address single molecules and measure their environment. These methods are compared to others that yield less information on the system under study.

The well-defined geometries, exceptional mechanical properties, and extraordinary electric characteristics, among other outstanding physical properties of CNTs, qualify them for many potential applications, especially in nanoelectronics, NEMS, and other nanodevices. Nanorobotic manipulations, which are characterized by multiple degrees of freedom (DOFs) with both position and orientation control, independently actuated multiprobes, and real-time observation systems, are one of the most promising technologies for assembling complex nanodevices in three–dimensional (3-D) space and providing a potential route toward the application of such devices. In "Assembly of Nanodevices with Carbon Nanotubes Through Nanorobotic Manipulations," T. Fukuda *et al.* present a 16-DOF nanorobotic manipulation system, and demonstrate a nano laboratory, a prototype nanomanufacturing system based on the manipulation system, which is designed for the assembly of nanodevices with multiwalled CNTs (MWNTs), with the abilities of *in situ* property characterization and nanofabrication. Key techniques for nanoassembly, including the preparation of nano building blocks and property characterization of them, the positioning of the building blocks with nanometer-scale resolution, and the connection of them, have been shown to be effective with their nano laboratory. Nanotube-based building blocks are prepared by directly picking up, *in situ* property characterization, destructive fabrication, and shape modifications. Kinds of nanotube junctions, the fundamental elements for both nanoelectronics and NEMS, have been constructed by positioning the building blocks together under real-time observation with a field-emission scanning electron microscope (FESEM), connecting them with naturally existing van der Waals forces, electron-beam-induced deposition (EBID), or mechanochemical bonding.

In "Nanotube Electronics: Non-CMOS Routes," J. Xu reviews the recent advances in controlled fabrication of CNTs of uniform diameter, length, and spacing, and discusses their fundamental properties. He also presents some possible applications in the broad content of nanotube electronics. Special attention is paid to the underlying physics and engineering applications in acquisition and execution of the information. The traditional information-processing roles of electronics and CMOS-like routes are excluded. Directions and prospects of nanotube technologies are illustrated with several examples.

III. Novel Circuit Models and Silicon Devices

In "Nonlinear Circuit Foundations for Nano Devices. . .," L. Chua describes the nonlinear circuit foundations for nanodevices. A nanodevice cannot perform computation or information processing unless it is locally active—a deep circuit-theoretic property which can only be determined from the circuit model of the device. Modeling nonlinear high-frequency nanodevices requires the introduction of a high-order family of nonlinear circuit elements which are capable of emulating such exotic quantum-mechanical effects as Coulomb blockade, Kondo resonance, quasiparticle interactions, Aharonov–Bohm nonlocality, etc. These model building blocks are defined axiomatically and represented periodically via a four-element torus.

The paper "Extremely Scaled Silicon Nano-CMOS Devices," by L. Chang, *et al.*, is focused on the extremely scaled silicon nano-CMOS devices. As CMOS technology enters the sub-90-nm regime, the adoption of new tran-

sistor structures, such as the ultrathin-body single-gate and double-gate MOSFETs, is highly desirable. Short-channel effects can be controlled by the thickness of the silicon body, thus relaxing requirements on gate oxide thickness scaling and dopant-profile engineering. In this work, thin-body devices are demonstrated down to 15-nm gate lengths. Practical fabrication of the double-gate device is realized by introduction of the FinFET structure. Key technological challenges, including gate work function engineering and sublithographic patterning, are described. Scaling limits and performance projections are also presented.

IV. Quantum Devices

The paper "Modeling and Prospects for a Solid State Quantum Computer," by H. Ruda and B. Qiao, is focused on the modeling and prospects for building a quantum computer. Moore's law is steadily driving the scaling of current integrated circuit technology to ever smaller characteristic dimensions. Before the next decade is through, it is clear that the classical transport of charge underlying the operation of today's devices and circuits will be severely challenged by quantum effects. These effects may be seen as hurdles or as a catalyst to working with purely quantum or perhaps hybrid devices and architectures. At the same time, such quantum phenomena may be explored as a means to implementing so-called quantum information systems provided practical issues are surmounted—the key issues being to manufacture the appropriate structures and to implement them. Not the least of the problems in the latter case is so-called decoherence. The authors present a vision for this emerging field, discussing limitations and potential approaches to overcoming them with the hope of ushering in a new era for computing based on harnessing the natural quantum processes emergent on the nanometer scale.

In "Variable Optical Buffer Using Slow Light in Semiconductor Nanostructures," C. Chang-Hasnain *et al.* propose and analyze a compact variable all-optical buffer using semiconductor quantum dot structures. Buffering is effectively achieved by varying the group velocity of the optical signal using an external light source to create an electromagnetically induced transparency effect in the quantum dots. This technique would increase the variability (or storage capacity) by five to six orders of magnitude comparing other semiconductor waveguide or resonator techniques.

In "Self-Organized Anisotropic Strain Engineering: A New Concept for Quantum Dot Ordering," R. Nötzel *et al.* introduce a new concept for creating ordered arrays of quantum dots by self-organized epitaxy. Self-organized anisotropic strain engineering of InGaAs/GaAs multilayer templates produces distinct strain patterns for the ordering of quantum dots on top in one- and two-dimensional nanoscale arrays and networks due to local strain recognition. The quantum dot arrays exhibit excellent structural and optical properties to establish the functional building blocks required for the realization of quantum computing and information technology in solid state.

V. NEMS

In "Nanoelectromechanical Quantum Circuits and Systems," H. De Los Santos introduces the novel field of nanoelectromechanical quantum circuits and systems. The field derives from exploiting progress in techniques for fabricating, down to nanometer-length scales, freestanding device structures that incorporate mechanical motion and that may be designed to perform a variety of functions, such as optical, electrical, and, in particular, mechanical and mixed-domain. Since novel quantum mechanical effects, for instance, quantized heat flow, manifestation of charge discreteness, and the quantum electrodynamical (QED) Casimir effect, become operative in this regime, exciting new paradigms for circuit modeling and design must be invoked in order to fully exploit the potential of this technology in sensing, computation, and signal processing applications.

In the paper "Nanorobots, NEMS, and Nanoassembly," A. Requicha discusses the state of the art in nanorobot design and construction. Nanorobots are typical NEMS and raise all the important issues that arise in NEMS, from sensing and actuation to control, communications, power and interfacing. Artificial nanorobots do not exist yet, but nanoscale robot components such as sensors and actuators are beginning to appear. After nanorobots and NEMS, the paper changes its focus to the assembly of nanoscale building blocks with macroscopic robots, which typically are atomic force microscopes (AFMs). Here the state of the art is more advanced. Nanomanipulation with AFMs is now done routinely in several labs, and nanostructures are being built by positioning components and then connecting them by various chemical and physical processes. Nanoassembly is a promising process for building and investigating device prototypes, and may become a practical fabrication technique if current work on multitip arrays comes to fruition.

VI. Interconnects/Circuits/Architectures

Is terascale integration possible? In "Limits to Binary Logic Switch Scaling—A Gedanken Model," V. Zhirnov and colleagues consider device scaling and speed limitations on von Neumann computing that are derived from the requirement of "least energy computation" at maximum device densities and speed. They consider computational systems whose material realizations utilize electrons and energy barriers to represent and manipulate their binary representations of state. The analysis is based on the concept of distinguishability of binary state(s). It is shown that for nanometer-scale devices, where tunneling plays a significant role, the fundamental limit on the energy of a single binary

switching transition is larger than $k_B ln2$. The article suggests that even if entirely different electron transport devices are invented for digital logic, their potential for density and performance may not go much beyond the ultimate limits obtainable with CMOS technology, due primarily to limits on heat removal capacity.

In their paper, "Molecular Electronics: From Devices and Interconnect to Circuits and Architecture," M. Stan *et al.* address molecular electronics from devices and interconnects to circuits and architecture. Most existing studies were focused on the devices and interconnections. The authors extend the efforts to discuss issues at the circuit and architectural levels. Based on the proposed nanoscale interconnect and device structures, the authors explore the design space available to the nanoelectronic circuit designers and system architects.

In "An *Ab Initio* Approach to the Calculation of Current-Voltage Characteristics of Programmable Molecular Devices," J. Seminario *et al.* present a scenario for molecular electronics (moletronics) whereby microelectronics can further be scaled down below its minimum feature size making use of the programmability feature of molecular devices. Since the minimum feature size also determines the smallest addressable distances in the fabrication of electronic circuits, any potential molecular device in the nanometer size would be discarded, except if this device could be programmed remotely to perform a specific function. The authors demonstrate with examples based on *ab initio* quantum calculations how molecules with high nonlinear behavior able to be assembled on an array by chemical (as opposed to lithographic) means can have multivalued responses and, thus, are able to be programmed. Molecular programmability compensates for the inability to address feature sizes in the range of one nanometer and, therefore, complements and expands the capabilities of present microelectronics to the nanometer domain. They analyze and propose the solution to the critical point for the development of molecular electronics, i.e., the programmability of the electronic devices to compensate for the inability to perfectly address chemically assembled molecules. The paper also includes a description and usage of the methods and techniques that compose the molecular electronics design automation (MEDA) tools.

VII. Ethics

In her paper, "Zeroing in on Ethical Issues in the Nano Area," V. Weil discusses ethical issues in the nano era. Setting aside exaggerated notions of both the benefits and harm to be expected from nanotechnologies, we need to focus ethical investigation on specific initiatives at the nanoscale that are already underway or planned. The aims are to anticipate ethical issues likely to arise in specific cases, to foster sensitivity to ethical issues and responsibility among nano specialists and policy makers, and to stimulate interchange between members of the public and nano specialists so that the public can become involved. After clarifying what the term "nanotechnology" embraces and looking at cautionary lessons from experience with the information technologies and biotechnology, the discussion turns to the importance of anticipating consequences, intended and unintended. Although there is a lack of specific nano options to consider, a brief survey indicates the issues to watch out for: preventable harms, conflicts about justice and fairness, respect for persons, and more specifically, safeguards for workers in new production processes, intellectual property concerns, preservation of university values in university/industry relationships, and conflicts of interest. Three main fronts of activity are needed to address ethical issues: 1) incorporating ethics research into nano research and development enterprises; 2) devising mechanisms to involve the public so that their perspectives and concerns feed back into research and development; and 3) initiating educational efforts at every level addressing both technical aspects and ethics and social implications aspects.

VIII. Special Thanks

Successful publication of this Special Issue would not be possible without the enthusiastic support of many volunteers and IEEE professionals. Great thanks go to J. Calder and M. Scanlon at the office of Proceedings of the IEEE. The Guest Editors would like to express deep appreciation to L. Terman, R. Trew, C. Lau, T. Theis, H. T. Kung, H. C. Lin, W. Porod, A. Csurgay, E. Friedman, C. Toumazou, A. Andreou, G. Cauwenburghs, and many tireless reviewers and supporters.

Continuous advances in nanotechnology enable human beings with the ability to manipulate at the atomic level in mass quantity. It is important that we live in good harmony with the earth, the sun, and the universe for many more generations to enjoy. Advocation and inspiration on such from S. A. Sheu, J. C. Sheu, and R. J. Sheu of the Pasadena, CA, area; from C.-L. T. Wu, C. C.-Y. Wu, and A. Y.-H. Wu of the Hsin-Chu, Taiwan, R.O.C., area; and T. Sze of the Silicon Valley, CA, area are highly appreciated.

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Dr. Wu has received numerous awards in Taiwan, R.O.C. He is a Recipient of the IEEE Third Millennium Medal. He is also a Member of Eta Kappa Nu and Phi Tau Phi. He served as VLSI Track Chair of the 1999 ISCAS in Orlando, FL, and gave tutorial talks at ISCAS in the 1990s. He was General Chair of 1994 APCCAS Conference for researchers from the United States, Japan, and all over the world. He is the Founding Chair of the Technical Committee on Nanoelectronics and Giga-scale Systems. He served as Chair of the Neural Technical Committee and as Chair of the Multimedia Technical Committee. He is a Board of Governors Member of the IEEE Circuits and Systems (CAS) Society. He was Guest Editor of the August 1997 Multimedia Special Issue for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, and was Associate Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II, IEEE TRANSACTIONS ON VLSI SYSTEMS, and IEEE TRANSACTIONS ON MULTIMEDIA. He is currently CAS Editor for IEEE *Circuits and Devices Magazine*. He is CAS Representative to the IEEE Neural Networks Society. He has served as CAS Taipei Chapter Chair and IEEE Taipei Section Chair. In 2000 and 2001, he served as a Distinguished Lecturer in the IEEE CAS Society.

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Dr. Sze has received the IEEE Ebers Award. In Taiwan, he has received the Sun Yet-Sen Award, the National Science and Technology Award, and the National Chair Professor Award. He is a Member of the Academia Sinica in Taiwan; the Chinese Academy of Engineering, Beijing, China; and the U.S. National Academy of Engineering.