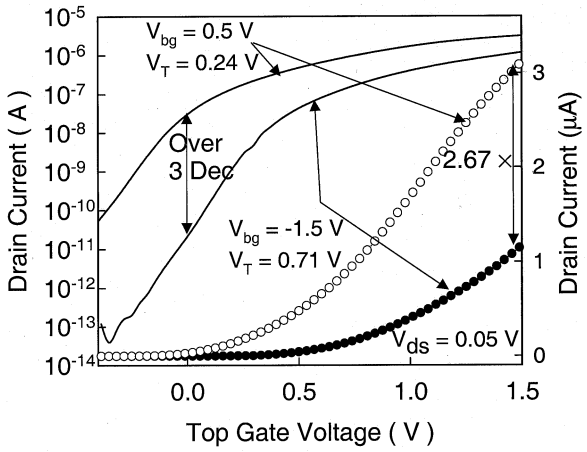

Fig. 4. On-current and off-current changes in the SA ESDG device under different BG biases.

IV. Summary

An SA ESDG transistor fabrication process has been demonstrated. The successful implementation of the SA ESDG structure in the fabricated device has been verified by the SEM photograph. The fabricated devices have shown the reasonably good performances. Moreover, the measured dynamic threshold voltage effects have been found to be consistent with that calculated by theoretical formula.

Acknowledgment

The authors would like to thank the fabrication staffs at the HKUST for helping with the processing.

References

[1] D. Frank, S. Laux, and M. Fischetti, "Monte Carlo simulation of a 30-nm dual-gate MOSFET: How far can silicon go?," in *IEDM Tech. Dig.*, 1992, p. 553.

[2] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, and T. Elewa, "Double-gate silicon-on-insulator transistor with volume inversion: a new device with greatly enhanced performance," *IEEE Electron Device Lett.*, vol. EDL-8, pp. 410–412, 1987.

[3] Y. Taur, "Analytic solutions of charge and capacitance in symmetric and asymmetric double-gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 48, pp. 2861–2869, Dec. 2001.

[4] I. Yang, C. Vieri, A. Chandraksan, and D. A.Dimitri A. Antoniadis, "Bottom-gate CMOS on SOIAS for dynamic threshold voltage control," *IEEE. Trans. Electron Devices*, vol. 44, pp. 822–831, 1997.

[5] H.-S. Wong, K. Chan, and Y. Taur, "Self-aligned (top and bottom) double-gate MOSFET with a 25 nm thick silicon channel," in *IEDM Tech. Dig.*, 1997, pp. 427–430.

[6] D. Hisamoto, W.-C. Lee, J. Kedzierski, E. Anderson, H. Takeuchi, K. Asano, T.-J. King, J. Bokor, and C. Hu, "A folded-channel MOSFET for deep-sub-tenth micron era," in *IEDM Tech. Dig.*, 1998, pp. 1032–1034.

[7] X. Huang, W.-C. Lee, C. Ku, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y.-K. Choi, K. Asano, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, "Sub 50-nm FinFET: PMOS," in *IEDM Tech. Dig.*, 1999, pp. 67–70.

[8] J. H. Lee, G. Tarashi, A. Wei, T. A. Langdo, E. A. Fitzgerald, and D. A. Antoniadis, "Super self-aligned double-gate (SSDG) MOSFET's utilizing oxidation rate difference and selective epitaxy," in *IEDM Tech. Dig.*, 1999, pp. 71–74.

[9] H. Wang, M. Chan, S. Jagar, V. M. C. Poon, M. Qin, Y. Wang, and P. K. Ko, "Super thin-film transistor with SOI CMOS performance formed by a novel grain enhancement method," *IEEE Trans. Electron Devices*, vol. 47, pp. 1580–1586, Aug. 2000.

[10] J. P. Colinge, *ULSI Devices*. New York: Wiley, 2000, pp. 234–235.

Simultaneous Quality Improvement of Tunneling- and Interpoly-Oxides of Nonvolatile Memory Devices by NH_3 and N_2O Nitridation

Tien Sheng Chao and Tsung Hsien Chang

***Abstract*—This brief presents a new nitridation process on floating poly-Si gate to improve the quality of both tunneling oxide and interpoly-oxide of nonvolatile memories. Three types of poly-Si for a floating gate have been investigated. We found *in-situ* doped poly-Si shows the best performance in terms of breakdown field, charge-to-breakdown ($Q_{\rm BD}$) and trapping rate. The $Q_{\rm BD}$ of interpoly-oxide can be reached as high as 35 C/cm^2. This scheme is very promising for nonvolatile memory devices.**

***Index Terms*—Interpoly-oxide, N_2O, NH_3, nitridation, nonvolatile memory, tunneling oxide.**

I. Introduction

With the scaling down of thickness of the tunneling oxide and interpoly-dielectrics, the quality of dielectric becomes very critical for EEPROM and Flash nonvolatile memories. Low leakage of the dielectric means long data retention time. Recently, N_2O-grown polyoxide film has been shown excellent electrical properties due to its incorporation of nitrogen at the interface of polyoxide/floating poly-Si gate [1]. However, rough interface, resulting from the thermal oxidation of rough poly-Si surface, degrades the integrity of interpoly-oxide. It has been reported that chemical vapor deposition (CVD) oxide instead of using thermal oxidation exhibits smooth interface due to no consumption of poly-Si [2], [3]. In addition, *in-situ* doped poly-Si and with an additional N_2O rapid thermal annealing (RTA) treatment can significantly improve the quality of interpoly-oxide. High quality stack nitride/oxide gate dielectrics prepared by *in-situ* rapid thermal N_2O oxidation of NH_3-nitrided Si has been proposed by Song *et al.*, [4]. Previously, we have extended this NH_3 nitridation process on poly-Si in elsewhere [5]. With an additional N_2O treatment, this scheme improves the quality of interpoly-oxide further. A very high $Q_{\rm BD}$ (20 C/cm^2) can be obtained for interpoly-oxide under constant current stressing. Among these reports, there is no detailed study focusing on the impact of the quality of the bottom tunneling oxide which undergoes a nitridation process on the floating poly-Si gate during growth of the interpoly-oxide. Therefore, in this brief, the effect of nitridation of floating poly-Si on the tunneling oxide is investigated. Based on the optimized nitridation scheme reported in [5], three-type of floating poly-Si gates are investigated and the impact of this nitridation on the bottom tunneling oxide integrity is investigated at the same time. Using N_2O oxidation on NH_3-nitrided poly-Si, we found *in-situ* doped poly-Si shows the best performance in terms of breakdown filed, charge-to-breakdown($Q_{\rm BD}$) and trapping rate. The $Q_{\rm BD}$ of interpoly-oxide can be reached as high as 35 C/cm^2. Besides, the integrity of tunneling oxide has also been significantly improved for this nitridation scheme. This optimized scheme is very promising for nonvolatile memory devices.

Manuscript received June 16, 2003; revised July 29, 2003. This work was supported by the National Science Council of Taiwan, Taiwan, R.O.C. under Grant NSC89-2215-E-317-009. The review of this brief was arranged by Editor S. Kimura.

T. S. Chao is with the Department of Electrophysics, National Chiao Tung University, Hsinchu 30050, Taiwan, R.O.C. He is also with the National Nano Device Laboratories, Hsinchu 300, Taiwan, R.O.C.

T. H. Chang is with the Department of Engineering and System Science, National Tsing Hua University, Hsinchu 300, Taiwan, R.O.C.

Digital Object Identifier 10.1109/TED.2003.818819

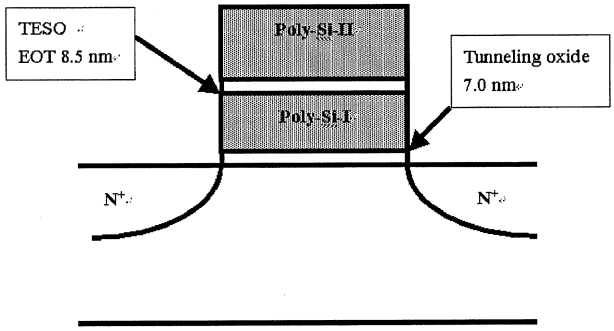

Fig. 1. Cross section of the device.

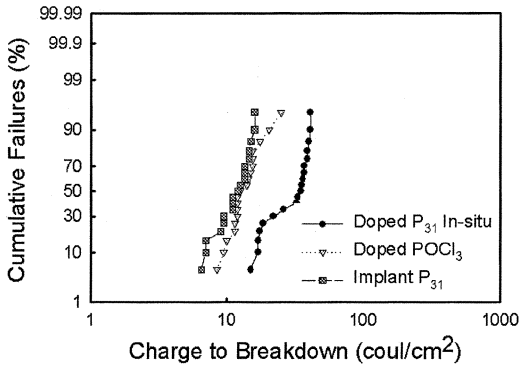

Fig. 2. Cumulative failures plot of charge-to-breakdown.

II. Device Fabrication

Fig. 1 shows the cross section of devices. After local oxidation of silicon (LOCOS) isolation, tunneling oxide of 7 nm was thermally grown in dry O_2 at 900 °C. The floating poly-Si gate (poly-Si-I) with a thickness of 300 nm was deposited and doped by three different methods, including *in-situ* N^+-doped (namely *in-situ*), $POCl_3$-doped (namely $POCl_3$, 900 °C, 30 min), and N^+-implanted (namely Implant, P_{31}, 50 keV, 5×10^{15} ion/cm^2). An ultrathin nitride film was grown on this poly-Si-I by NH_3 nitridation in a LPCVD system at 800 °C for 2-h. The flow rate was set at 105 sccm and the pressure was 500 m torr. All samples were immediately RTA-annealed in N_2O at 800 °C for 20 s to reduce the hydrogen incorporation. The interpoly-oxide was deposited using TEOS in an LPCVD system and then annealed again in an RTA N_2O ambient at 800 °C for 20 s to condense this CVD dielectric to thickness about 8.5 nm. After that, poly-Si-II of 300 nm was deposited and doped by $POCl_3$ to a resistivity of 30–40 $\Omega/\square$. After gate definition and etching, N^+-doped source and drain were formed by As implantation, at 20 keV to a dose of 5×10^{15} ions/cm^2. Then, a passivation oxide of 550 nm was deposited. Contact holes were then open and standard four-layer metal (Ti/TiN/Al/TiN) was sputtered and defined, followed by a sintering process at 400 °C for 30 min.

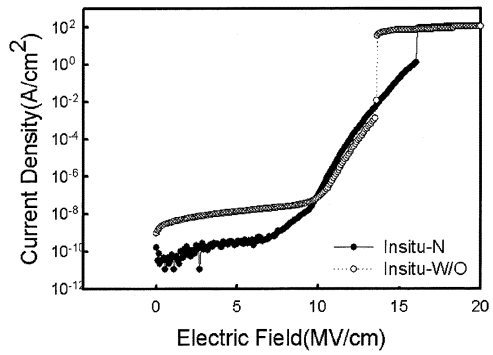

Fig. 3. Current density versus electric field of poly-oxide for *in-situ* sample.

III. Results and Discussion

A. Interpoly-Oxide Integrity

It is well known that the quality of the interpoly-oxide depends on the roughness of the poly-Si gate. Rough interface degrades the integrity of interpoly-oxide. Surfaces of the three floating poly-Si gates were first measured by atomic force microscopic (AFM). Resultant roughness was 1.2, 3.8, and 4.8 nm, respectively, for *in-situ*, $POCl_3$, and Implant samples, respectively. The *in-situ* sample shows the smoothest surface among these samples. The gate voltage shifts (ΔV_g) under constant current stressing at 10 mA/cm^2 (not shown). Electron trapping rate is the largest for the Implant sample, the second is the $POCl_3$ sample, and the smallest one is the *in-situ* sample. Resultant charge-to-breakdown, $Q_{\rm BD}$, for these samples are shown in Fig. 2. It is found that the Implant sample exhibits the lowest $Q_{\rm BD}$ (12 C/cm^2 at a 50% failure rate) due to the rougher surface, the $POCl_3$ sample is the second (12.5 C/cm^2) and the *in-situ* sample is the largest one among these three samples. The $Q_{\rm BD}$ for *in-situ* can be increased as high as 35 C/cm^2. Based on the result, we found that *in-situ* doped poly-Si is the best choice to obtain a high integrity of interpoly-oxide. The nitridation scheme can also improve the integrity further. By using this combination, $Q_{\rm BD}$ increases from 20 C/cm^2 in [5] to a record a high 35 C/cm^2 in this brief.

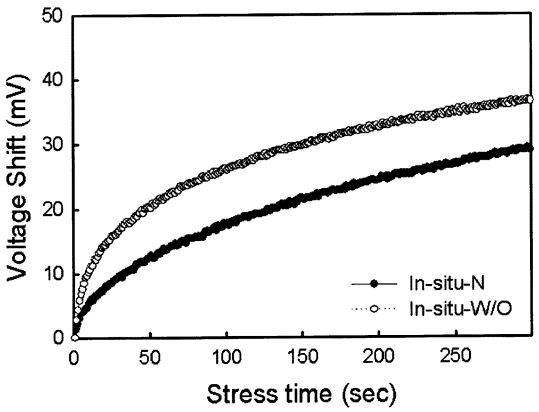

Fig. 4. Shift of gate voltage under constant current stressing at 100 mA/cm^2 of *in-situ* sample.

B. Tunneling Oxide Integrity

1) B-1 MOS Capacitors: As we mentioned in part A, using nitridation step on poly-Si-I shows improved performance. In this section, the tunneling oxide integrity with or without (control sample) nitridation of poly-Si-I will be investigated. Since the trend of improvement is similar to Implant and $POCl_3$ samples, the following only shows the result of the *in-situ* sample. Fig. 3 show the *J–E* curves with (N)/without (W/O) nitridation for *in-situ* samples. We found all samples underwent nitridation on the poly-Si-I show an improved breakdown field, and lower leakage in the low field. Improvement of the gate voltage shift under constant current stressing (100 mA/cm^2) of the *in-situ* sample is shown in Fig. 4. It is found that the electron trapping rate decreases significantly after the nitridation. $Q_{\rm BD}$ at 100 mA/cm^2 stressing for the three samples are also exhibited the same trend, but only the *in-situ* sample is shown in Fig. 5. It is seen that the $Q_{\rm BD}$ is significantly improved with nitridation. Leakage current of the gated diode for these samples were measured and shown in Fig. 6. We found the nitrogen from nitridation of poly-Si-I decreases the interface density states.

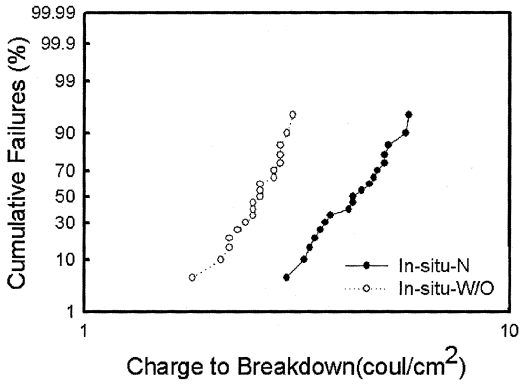

Fig. 5. Cumulative plot of charge-to-breakdown of *in-situ* sample.

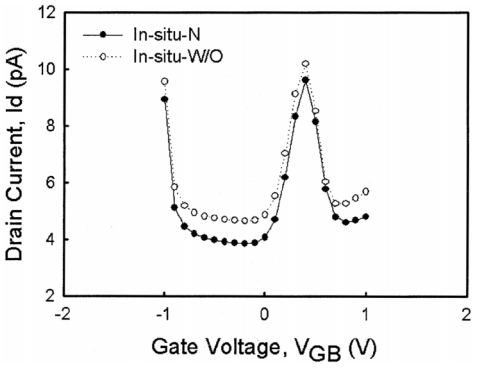

Fig. 6. Measured leakage current of gated diode as a function of V_g for *in-situ* sample.

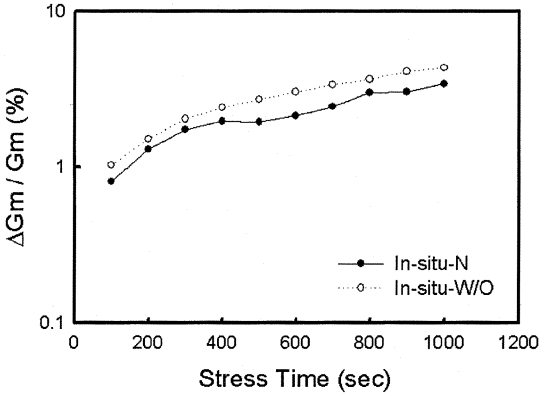

Fig. 7. Degradation of $G_{M(\max)}$ under stress at $I_{\mathrm{SUB}(\max)}$ for *in-situ* sample for 1000 s.

C. B-2 MOSFETs

Hot carrier stressing on MOSFETs with the tunneling oxide with or without nitridation from poly-Si-I are investigated under $V_D = 4$ V, $V_g = 2.2$ V for 1000 sec. Fig. 7 shows the degradation of G_M of the *in-situ* sample. We found that G_M degradation can be improved with nitridation. Degradations of driving current is shown in Fig. 8. Devices with nitridation also show improved performance. It is consistent that all the electrical properties of MOSFET with the tunneling oxide can be improved with the nitridation on the floating poly-Si gate.

It is well known that nitridation of dielectrics improves the electrical properties significantly due to creation of Si-N bonds at the interface that have a higher bond energy than Si-H bonds. The other reason is

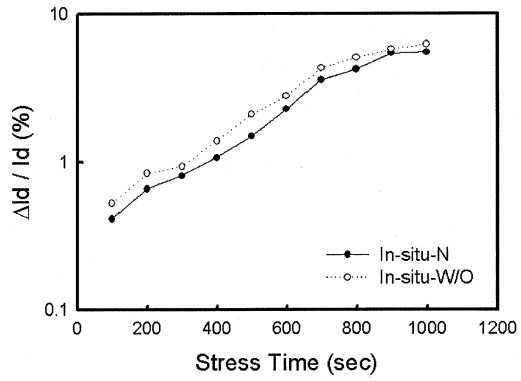

Fig. 8. Degradation of driving current of MOSFETs with *in-situ* doped poly-Si under stressing.

the stress relaxation when nitrogen is introduced at the interface [6]. In addition, reliability of MOSFETs can be improved by N_2O reoxidation on poly-Si gate [2]. It was found that nitrogen diffuses quickly through the poly-Si gate and piles up at both oxide interfaces, resulting in superior reliability properties [7]. Consequently, to fabricate nonvolatile memory with stacked structure, we can use nitridation on the poly-Si-I, resulting in the diffusion of nitrogen through the poly-Si-I and piles up at the interface at the tunneling oxide during the nitridation process. Hence, integrity of both interpoly-oxide and tunneling oxide can be improved simultaneously. By using this scheme, the Q_{BD} of interpoly-oxide can be reached to a record high of 35 C/cm^2. And the reliability of MOSFETs of the tunnel oxide is also significantly improved.

IV. Conclusion

In this brief, we proposed a new nitridation scheme on the dielectrics for nonvolatile memories. Nitridation on the floating gate results in diffusion of nitrogen through the poly-Si to bottom tunneling oxide that improves the integrity of the tunneling oxide and hot-carrier resistance of MOSFETs at the same time. Hence, this process appears a very promising scheme to fabricate nonvolatile memory.

References

[1] C. S. Lai, T. F. Lei, and C. L. Lee, "The characteristics of polysilicon oxide grown in pure N_2O," *IEEE Trans. Electron Devices*, vol. 43, pp. 326–331, Feb. 1996.

[2] C. H. Kao, C. S. Lai, and C. L. Lee, "The TEOS oxide deposited on P *in-situ*/$POCl_3$ doped poly-Si with rapid thermal annealing N_2O," *IEEE Trans. Electron Devices*, vol. 45, pp. 1927–1933, Sept. 1998.

[3] R. I. Hedge, W. M. Paulson, and P. J. Tobin, "Surface topography of phosphorus doped polysilicon," *J. Vac. Sci. Technol. B*, vol. 13, no. 4, pp. 1434–1441, 1995.

[4] S. C. Song, H. F. Luan, C. H. Lee, A. Y. Mao, S. J. Lee, J. Gelpey, S. Marcus, and D. L. Kwong, "Ultra thin high quality stacked nitride/oxide gate dielectrics prepared by *in-situ* rapid thermal N_2O oxidation of NH_3-nitrided Si," in *Proc. VLSI Tech. Symp.*, Kyoto, Japan, 1999, pp. 137–138.

[5] W. L. Yang, T. S. Chao, C. M. Cheng, T. M. Pan, and T. F. Lei, "High quality interpoly dielectrics deposited on the nitrided-polysilicon for nonvolatile memory devices," *IEEE Trans. Electron Devices*, vol. 48, pp. 1304–1309, July 2001.

[6] Y. Harada, K. Eriguchi, M. Niwa, T. Watanabe, and I. Ohdomari, "Impacts of strained SiO_2 on TDDB lifetime projection," in *Proc. VLSI Tech. Symp.*, 2000, pp. 216–217.

[7] C. S. Lai, T. F. Lei, and C. L. Lee, "The electrical characteristics of polysilicon oxide grown in pure N_2O," *IEEE Electron Device Lett.*, vol. 16, pp. 385–386, Aug. 1995.