PERGAMON

Available online at www.sciencedirect.com

SCIENCE DIRECT®

Solid-State Electronics 47 (2003) 1693–1698

SOLID-STATE ELECTRONICS

www.elsevier.com/locate/sse

Modeling and design of the high performance step SOI-LIGBT power devices by partition mid-point method

Fang-Long Chang [a,*], Ming-Jang Lin [a], Gwo-Yann Lee [a], Young-Shying Chen [b], C.W. Liaw [c], Huang-Chung Cheng [a]

[a] Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan, ROC
[b] Industrial Technology Research Institute, Hsinchu, Taiwan, ROC
[c] Department of Electronics Engineering, National Tsing Hua University, Hsinchu, Taiwan, ROC

Received 11 September 2001; received in revised form 12 February 2002; accepted 16 April 2003

Abstract

In this paper, a partition method is proposed to study the high voltage devices with the step doping profile for the first time. It has been proposed that its breakdown voltage can be approached to that of the linearly graded devices with similar forward voltage drop (V_{ce}). In addition, by this method, the breakdown voltage can be deduced and its corresponding issue location is also fingered out in the step drift region. Furthermore, in order to reduce the undesirable additional masks, the degraded factor (D) is developed to obtain better performance with the least number of frames. Eventually, a 660 V step analytical results are compared with a 606.6 V MEDICI simulation and this shows that the partition method is very effective.
© 2003 Elsevier Ltd. All rights reserved.

Keywords: Step drift doping profile; Linearly graded doping; SOI-LIGBT

1. Introduction

In recent years, Silicon-on-Chip (SOC) has been devoted to develop. In respect of the high power applications, Silicon-on-Insulation (SOI) is the promising candidate in this field, because of its superior isolation characteristic to the Junction Isolation (JI) devices, reducing the LIGBT turn-off time with thin SOI layer, and increasing the blocking voltage under well-RESURF design. For low power SOI applications, it provides immunizing from the ionization via radiations, reducing parasitic capacitances, short-channel effects, hot-carrier effects, and static power consumption.

The SOI devices have two main problems, which must be addressed significantly, such as self-heating effect and lower breakdown than JI devices. The latter problem is even greater concern. This is due to the native ineffective RESURF effect in SOI layer. To achieve high breakdown voltage, a linear doping profile in the drift region is necessary to provide a more uniform electrical field distribution along the drift region and so to optimize the RESURF condition [1].

Using a Variation in Lateral Doping (VLD) technology in a sequence of small opening oxide slits, which can achieve the linearly graded doping profile to relax the two-dimension electrical-field effect and bring lower on-resistance with high breakdown voltage in the drift region. Unfortunately, there are two drawbacks of this structure: Firstly, the linearly graded doping profile needs complicated mask layout to be fabricated. Furthermore, it is difficult to know whether the doping profile is certainly satisfied [2]; Secondly, the local self-heating is arose near the lightly doping side and it

* Corresponding author. Address: Department of Electronics Engineering, National Tsing Hua University, Hsinchu, Taiwan, ROC. Tel.: +886-3-5712121-54218; fax: +886-3-5738343.
E-mail address: u8811515@cc.nctu.edu.tw (F.-L. Chang).

0038-1101/$ - see front matter © 2003 Elsevier Ltd. All rights reserved.
doi:10.1016/S0038-1101(03)00143-6

influences the reliability of surrounding low power cells on the same chip [3]. At present, when replacing the linear profile by the distinct doping region along lateral direction [4], the separated uniform doping can effectively avoid the former descriptions and can be easily realized by different implant dosages. Nevertheless, the additional mask of the step doping case is a serious problem in the cost aspect. Hence, this paper is to offer a choice of either increasing the masks with step doping or longer thermal process with linearly graded doping for designs.

2. Modeling descriptions and verifications

While deriving an n-separate frames in drift region, as shown in Fig. 1, the neighborhood frame with a previous frame is conjugated to find its individual boundary parameters. Assuming that the SOI layer is completely depleted and the buried oxide is charge-free, the frame 2-D Poisson equation is given with a parabolic approximation approach [5]

$$\frac{\partial^2\psi}{\partial^2 x}+\frac{\partial^2\psi}{\partial^2 y}=-\frac{qN}{\varepsilon_{\mathrm{si}}}, \tag{1}$$

and

$$\psi(x,y)=u(x)+u_1(x)y+u_2(x)y^2, \tag{2}$$

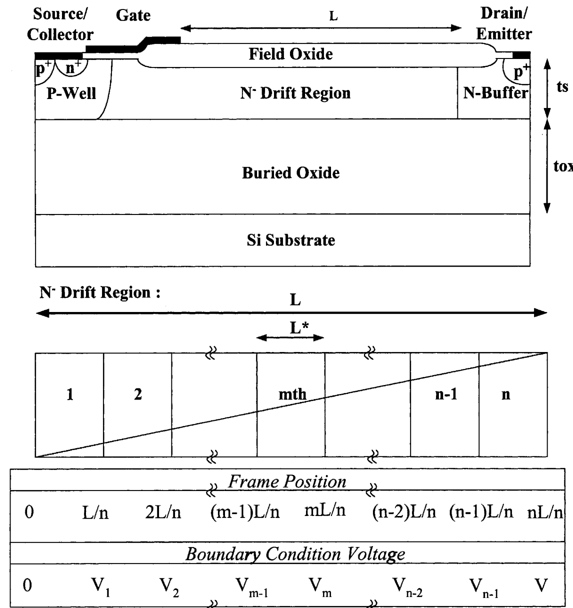


Fig. 1. Corresponding structure and frame architecture of step SOI-LIGBT device. The concentration of the first frame is equal to the background doping which is also replicated from p-well to gate edge.

$$E_y(x,0)=\left(\frac{\partial\psi(x,y)}{\partial y}\right)\bigg|_{y=0}=0, \tag{3}$$

$$E_y(x,\mathrm{ts})=\left(\frac{\partial\psi(x,y)}{\partial y}\right)\bigg|_{y=\mathrm{ts}}, \tag{4}$$

where $u(x)$ is the surface potential at $y=0$ and "N" is the concentration of each frame. From Eqs. (1)–(4) and the continuity of the displacement vector at the Si/SiO_2 surface, the potential can be simplified to be

$$\psi(x,y)=\left(1-\frac{y^2}{2\mathrm{ts}\left(\frac{\mathrm{ts}}{2}+\frac{\varepsilon_{\mathrm{si}}}{\varepsilon_{\mathrm{ox}}}\mathrm{tox}\right)}\right)u(x), \tag{5}$$

where the differential of Eq. (5) is its electrical field. Substituting Eq. (5) into Eq. (1), the surface potential equation can be expressed as

$$\left(1-\frac{y^2}{2\mathrm{ts}\left(\frac{\mathrm{ts}}{2}+\frac{\varepsilon_{\mathrm{si}}}{\varepsilon_{\mathrm{ox}}}\mathrm{tox}\right)}\right)\frac{\partial^2 u(x)}{\partial x^2}-\frac{u(x)}{\mathrm{ts}\left(\frac{\mathrm{ts}}{2}+\frac{\varepsilon_{\mathrm{si}}}{\varepsilon_{\mathrm{ox}}}\mathrm{tox}\right)}=-\frac{qN}{\varepsilon_{\mathrm{si}}}, \tag{6}$$

where the top of SOI layer is set at $y=0$. Assuming that mth frame (m) has existed at n-separate (n) frames. Each frame concentration (N) is the mean value of the linearly graded slope (a), which is spread into the individual frame. The relationship of its position and concentration (N) are mL/n, $a(2m-1)L/2n$, respectively. According to the quasi-neutral drift region under low-level injection condition, the surface potential of the mth frame in reach and non-reach boundary condition is given

$$u_m\left(\frac{(m-1)L}{n}\right)=V_{m-1},\quad u_m\left(\frac{mL}{n}\right)=V_m, \tag{7}$$

$$u_{mw}\left(\frac{(m-1)L}{n}\right)=V_{m-1},\quad u'_{mw}(w_m)=0, \tag{8}$$

where "w" is presented as the non-reach through length. The corresponding voltage is called the non-reach through voltage u_{mw}. Hence, combining Eqs. (7) and (8) with Eq. (6), the surface potential $u(x)$ will be solved while the value of $y=0$ is substituted. As the applied voltage increases, the impact ionization rate will determine whether the non-reach through of the mth frame can eventually deplete to the end. With deducing its ionization integral over the horizontal and vertical surface path, the mth frame's breakdown testing equation defined as [6]

$$\mathrm{IHori}_{m(w)}=\int_{[(m-1)L]/n}^{mL/n}[A(|E_{x(w)}(x,0)|)^7]\,\mathrm{d}x, \tag{9}$$

$$\mathrm{IVert}_{m(w)} = \int_0^{\mathrm{ts}} [A(|E_{y(w)}(K,y)|)^7]\,\mathrm{d}y + \int_{[(m-1)L]/n}^{mL/n} [A(|E_{x(w)}(x,\mathrm{ts})|)^7]\,\mathrm{d}x, \quad (10)$$

where

$$K = \frac{mL}{n} \text{ or } w, \quad (11)$$

$A = 1.8 \times 10^{-35}$ when $E(x,y)$ is expressed in V/cm [7]. "IHori" and "IVert" is the lateral and vertical impact ionization rates. To simplify the analysis, only consider the two high-field locations are considered: (1) the first frames along $y = 0$, where "IHori" is high and (2) the last frame at point ($x = K$, $y = \mathrm{ts}$), where "IVert" is high. Moreover, the critical electrical field and potential of the mth frame are obtained as one of the value "I" approaches to the value 1. To make a summary, the mth frame-testing flowchart described above is illustrated in Fig. 2.

In order to achieve higher breakdown voltage, the difference between maximum and minimum electrical fields must be eliminated in each frame. For this reason, a degraded factor "D" is provided to ensure near ideal-breakdown voltage as expected. It can be written as

$$D = \mathrm{Exp}[-x/t] + \mathrm{Exp}[(x - L^*)/t], \quad (12)$$

where

$$t = \sqrt{\mathrm{ts}\left(\frac{\mathrm{ts}}{2} + \frac{\varepsilon_{\mathrm{si}}}{\varepsilon_{\mathrm{ox}}}\mathrm{tox}\right)}, \quad (13)$$

$$L^* = \frac{L}{n}, \quad (14)$$

this factor "D" include SOI layer thickness (ts), buried oxide thickness (tox), frame length (L^*), and the number of frames (n). Among these the optimum structure parameters will be found at approaching $D = 1$. To simplify the mathematics in solving Eq. (10), it is convenient to assume the minimum electrical field is located in the coordinate of $x = L^*/2$. In place of the x-coordinate, the general solution is

$$D = 2 * \mathrm{Exp}\left[-\frac{L}{2nt}\right] \leqslant 1, \quad (15)$$

$$n \geqslant \frac{L}{2 * t * \ln 2}, \quad (16)$$

where the number of frames (n) is proportional to drift length (L) and inversely proportional to the term "t"—associated with the buried oxide and SOI layer thickness. It is apparent that the thicker buried oxide and shorter drift length will promote smaller number of frames, especially if the SOI layer thickness is large enough. This makes it possible to reduce production cost. A relationship of breakdown voltage and degraded factor is demonstrated in Fig. 3. The value 0.6 is corresponding to the

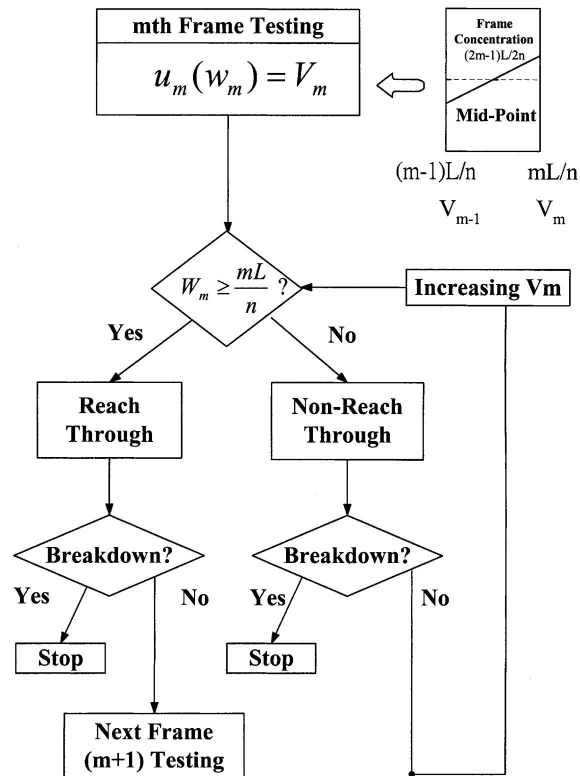


Fig. 2. Illustration of the partition method with a testing flowchart and single frame diagram. The key point is to determine whether the applied voltage will attain reach-through-out for each frame.

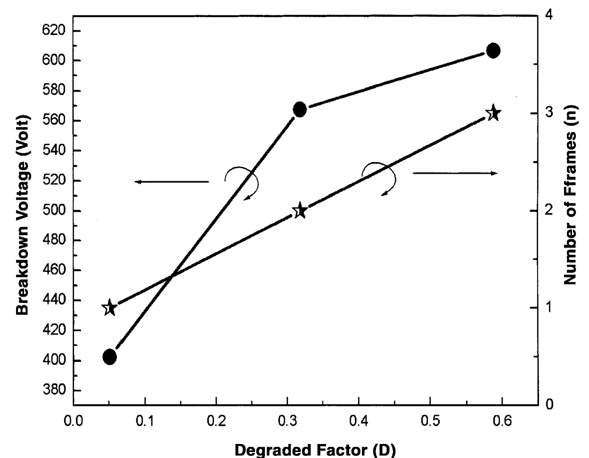


Fig. 3. Dependence of the breakdown voltage and frame number with degraded factor. The improvement of breakdown voltage is enough to use three frames in the drift region.

"three frames", which is chosen under economical consideration.

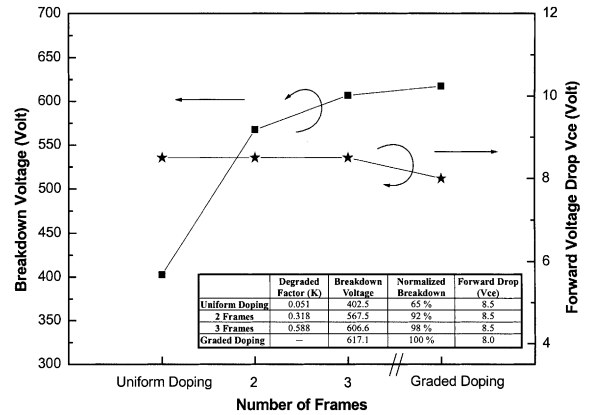
In this methodology, an algorithm is developed to obtain systematic n-separate frames cogitation. In the first part, the user is demanded to offer some fundamental parameters that comprise the drift length (L) with respond to linearly graded slope definition (a) [8]. Then, the algorithm works are listed as follows:

(1) Set up the structure parameter from the degraded factor (D).
(2) By dint of the flowchart in Fig. 2. Each frame electrical and potential function can be obtained step by step. The n-separate frames will donate $2n$ states that include reach and non-reach through case. If some frame breaks down during examination, the program will be claimed to stop.
(3) Be sure that each frame's electrical and potential function comprises not only device dimension parameters but also its neighbor boundary value.
(4) Start from the left side zero point and equalize its individual functional equation with its neighbor frame equation. Substitute all derivational boundary value into the next unknown frame equation to evaluate its unknown electrical and potential value in turn. Then these frames boundary values are functions of V_1 eventually ($x_m = x_{m+1}, x_{m+1} = x_{m+2}, \ldots$).
(5) Substitute the desired breakdown voltage into the final value "V". Then the value "V_1" will be gained, so every boundary condition value can be discovered from the right-side to left-side.

In the following, the breakdown voltage, weak-point, optimum design parameters, and low-cost way are taken systematically.

3. Results and discussion

In this section, a numerical example of this analysis is demonstrated. The data of the example is 600 V linearly graded SOI devices, whose specification is as follows: ts = 1.5 μm, tox = 5 μm, $L = 36$ μm, slope (a) = 5.05×10^{18} cm^{-4}. As the result of statistics, the required degraded factor (D), ranging from 0.5 to 0.7, is enough to achieve high breakdown voltage. So the value 0.6 is chosen such that three frames can be obtained under this economical mode. Fig. 4 shows the electricity of various partition frames, linearly graded, and uniform type for comparison. In this figure, the breakdown voltage of three-frame (607 V) is indeed nearly close to the linearly graded device (617 V) at similar V_{ce} of 12 V-gate bias at 100 A/cm^2. However, the deviation of the graded doping V_{ce} is caused by the different concentration between the p-well and the gate edge.



	Degraded Factor (K)	Breakdown Voltage	Normalized Breakdown	Forward Drop (Vce)
Uniform Doping	0.051	402.5	65 %	8.5
2 Frames	0.318	567.5	92 %	8.5
3 Frames	0.588	606.6	98 %	8.5
Graded Doping	–	617.1	100 %	8.0

Fig. 4. Investigation of the optimum device characteristics in respect of breakdown voltage and forward voltage drop with various number of frames. Its SOI layer thickness, buried oxide thickness, and the drift length are 1.5 μm, 5 μm and 36 μm respectively.

Moreover, for further comprehension, the three frame's electrical and potential-matching curves are illustrated in Fig. 5(a) and (b) with the fully reach through case. Its general equations for the electrical field are given below:

$$\mathrm{ExI} = \alpha\left[(\beta - 6V_1\varepsilon_{si}) * \cosh\left(\frac{x}{t}\right) - \beta * \cosh\left(\frac{L/3 - x}{t}\right)\right], \quad (17)$$

$$\mathrm{ExII} = 3\alpha\left[(\beta - 2V_2\varepsilon_{si}) * \cosh\left(\frac{L/3 - x}{t}\right) + (2V_1\varepsilon_{si} - \beta) * \cosh\left(\frac{2L/3 - x}{t}\right)\right], \quad (18)$$

$$\mathrm{ExIII} = \alpha\left[(5\beta - 6V\varepsilon_{si}) * \cosh\left(\frac{2L/3 - x}{t}\right) + (6V_2\varepsilon_{si} - 5\beta) * \cosh\left(\frac{L - x}{t}\right)\right], \quad (19)$$

where

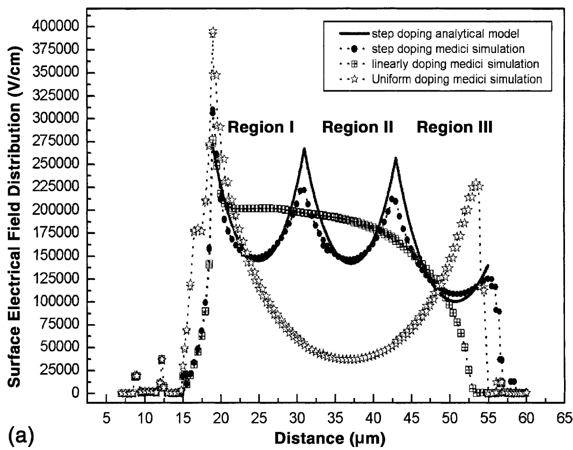
$$0 \leqslant \mathrm{I} \leqslant \frac{L}{3}, \quad \frac{L}{3} \leqslant \mathrm{II} \leqslant \frac{2L}{3}, \quad \frac{2L}{3} \leqslant \mathrm{III} \leqslant L, \quad (20)$$

and

$$\alpha = \frac{(2f^2 - y^2)}{12t^3\varepsilon_{si}} \cosh\left(\frac{L}{3t}\right), \quad (21)$$

$$\beta = aqt^2L, \quad (22)$$

where the relationship between V_1 and V_2 can be found from the algorithm in the fourth item. As pictured in



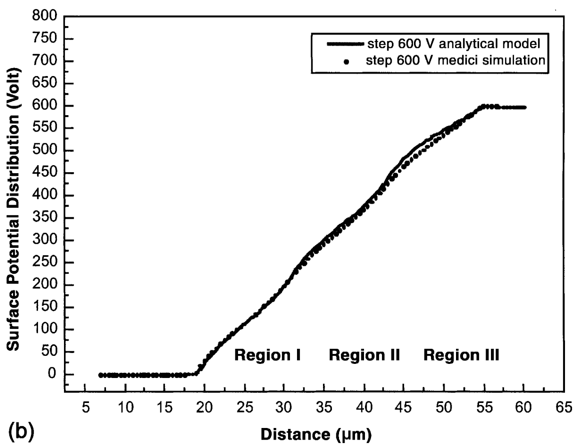
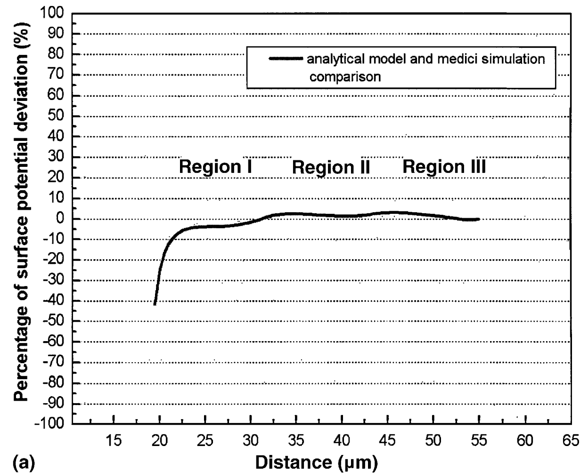


Fig. 5. (a) The different kinds of surface electrical field distribution are shown in each drift region before the breakdown voltage happens. The step doping type exhibits a significant electrical improvement compared to the uniformly doping type. (b) Comparison of the surface potential distribution with analytical model and MEDICI simulation. The analytical result is most in agreement with the data generated by MEDICI simulation.



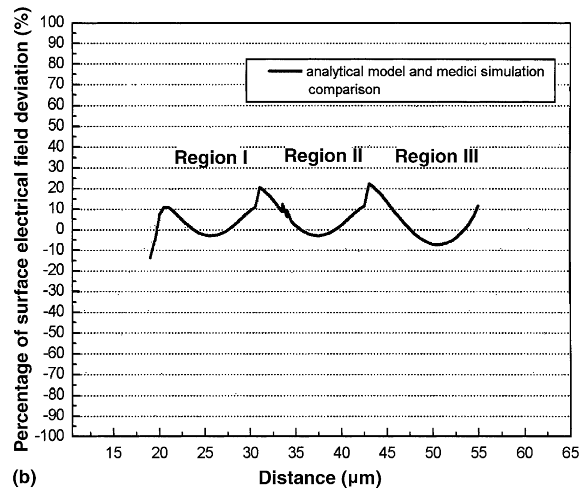


Fig. 6. (a) Percentage of the surface electrical field deviation as a function of the distance in three frames. Each neighbor frame at their boundary exist a higher error value. (b) Percentage of the surface potential deviation as a function of the distance in three frames. It is worth to mention that the maximum error value is occurred on the outset.

Fig. 5(a), the step doping devices exhibit 3 times improvement of the middle electrical field with the uniform doping type and 0.75 times less than that of the linearly graded doping devices. These simulated results are compared to analytic data, that showing good qualitative and quantitative agreement in Fig. 5(a) and (b). In these verification regulations, the highest impact ionization rate is found at the third (last) frame, where the value "IVert" is about 0.9 while substituting the voltage 660 into the value of "V". The breakdown voltage is over the prediction with only about 8.9% of the MEDICI simulation value.

In respect of step doping device reliability, the deviation percentages would be provided between analytical model and MEDICI simulation, illustrated in Fig. 6(a) and (b). As presented in these figures, the ranges of data variation are available from −5% to 5% in surface potential part and −20% to 20% in surface electrical field part. The deviation of surface electrical field become more severe than that of potential exhibition due to the differential at the corner of each frame, where exists the transitional tangent lines relative to high peak electrical value. Moreover, the positions of frame boundary are located accurately in each frame with this method.

It should be emphasized that the point of 20 μm distance indicates a large surface potential deviation in Fig. 6(b). The reason is that initial solution of the analytical model is set up the zero voltage value at the poly

gate edge (20 μm). But in the MEDICI simulation, the zero value of the origin point is situated at the p-well edge (15 μm). It is allowed to modify the initial solution if you prefer to obtain less deviation at the origin point, but the modified initial solution (0 V ⇒ 6 V) would not affect the previous consequence of this paper more seriously.

4. Conclusion

In this paper, the use of partition method is successful to explain the underlying reverse-bias performance, attain 50.7% improvement of the breakdown voltage compared with the uniform doping, and decrease the undesirable additional masks in the step doping SOI devices. It can also be implemented in the vertical devices by multi-epitaxy or multi-implanted technology without any additional masks, and superior device characteristics can be achieved as well. In summary, this method offer the designers with a choice between the step doping required more mask and the linearly graded doping required longer thermal process flexibly.

Acknowledgements

This research has been supported by the National Science Council of Taiwan under Contract NSC 90-2215-E-009-074. The authors thank National Center for High Performance Computing (NCHC) for providing MEDICI software and the Industrial Technology Research Institute (ITRI) for helpful discussions.

References

[1] Udrea F, Garner D, Sheng K, Popescu A, Lim HT, Milne WI. SOI power devices. Electron Commun Eng J 2000;(February).

[2] Zhang S, Sin JK, Lai TM, Ko PK. Numerical modeling of linear doping profiles for high-voltage thin-film SOI devices. IEEE Trans Electron Devices 1999;46(5):1036–41.

[3] Leung Y-K, Kuehne SC, Huang VS, Nguyen CT, Paul AK, Plummer JD, et al. Spatial temperature profiles due to nonuniform self-heating in LDMOS's in thin SOI. IEEE Electron Device Lett 1997;18(1):13–5.

[4] Sunkavalli R, Tamba A, Baliga BJ. Step drift doping profile for high voltage DI lateral power devices. SOI Conference, 1995 Proceedings, 1995 IEEE International. 1995. p. 139–40.

[5] Young KK. Short-channel effect in fully depleted SOI MOSFETs. IEEE Trans Electron Devices 1989;36:399–402.

[6] Merchant S, Arnold E, Baumgart H, Mukherjee S, Pein H, Pinker R. Realization of high breakdown voltage (<700 V) in thin SOI devices. In: ISPSD '91. Proceedings of the 3rd International Symposium on Power Semiconductor Devices and ICs, 1991. p. 31–5.

[7] Fulop W. Calculations of available breakdown voltage of silicon p–n junctions. Solid-State Electron 1967;10:39–43.

[8] Leung Y-K, Paul AK, Plummer JD, Wong SS. Lateral IGBT in thin SOI for high voltage, high speed power IC. IEEE Trans Electron Devices 1998;45(10):2251–4.