PAPER Special Section on Recent Progress in Microwave and Millimeter-Wave Technologies and Their Applications

A Flexible Microwave De-Embedding Method for On-Wafer Noise Parameter Characterization of MOSFETs

Yueh-Hua WANG[†a)], *Member*, **Ming-Hsiang CHO**[†], *and* **Lin-Kun WU**[†], *Nonmembers*

SUMMARY A flexible noise de-embedding method for on-wafer microwave measurements of silicon MOSFETs is presented in this study. We use the open, short, and thru dummy structures to subtract the parasitic effects from the probe pads and interconnects of a fixtured MOS transistor. The thru standard are used to extract the interconnect parameters for subtracting the interconnect parasitics in gate, drain, and source terminals of the MOSFET. The parasitics of the dangling leg in the source terminal are also modeled and taken into account in the noise de-embedding procedure. The MOS transistors and de-embedding dummy structures were fabricated in a standard CMOS process and characterized up to 20 GHz. Compared with the conventional de-embedding methods, the proposed technique is accurate and area-efficient.

key words: *de-embedding, microwave, MOSFETs, noise, RF, silicon*

1. Introduction

Wafer-level device characterization is extremely important for the design of high-performance RF/microwave integrated circuits. Since reliable device models require accurate on-wafer measurements, modeling test keys should be carefully designed to reproduce and remove the external parasitics surrounding the fixtured devices. To extract the intrinsic device characteristics from microwave measurements, much research effort has been devoted to this subject and several methods for parasitic de-embedding have been reported over the past years. The open-short de-embedding method [1] was developed to subtract the shunt admittance and series impedance of the probe pads and interconnects by employing an open and a short structure. Although there are many other methods for eliminating the unwanted parasitics [2]–[4], the open-short de-embedding procedure is still the current industry standard. The physics-based de-embedding methods mentioned above utilize lumped-circuit assumptions to model the parasitic networks. However, as the device is operated at microwave frequencies and/or its interconnect length is considerable, these lumped-circuit models may be invalid due to the distributed nature of silicon-based test fixtures. Recently, a noise de-embedding method based on cascade configuration [5] was presented. It uses open and thru dummies to subtract the pad admittance and interconnect parasitics and does not require any lumped-circuit representation. A cascade-based scalable noise de-embedding method [6] was also developed to reduce the chip area consumption for test structures. Although the cascade de-embedding schemes are more suitable for application in the microwave/millimeter-wave regime, the parasitic effects of the dangling leg between the MOSFET and ground plane are neglected in these cascade methods [7]. In this study, we propose a scalable noise de-embedding method by further taking into account the series impedance of the probe pads and the parasitic effects of dangling leg. To validate the proposed method, the MOS transistors and de-embedding standards were fabricated using a standard 0.25 μm CMOS technology, and the noise and S-parameter measurements were taken up to 18 GHz and 20 GHz, respectively.

2. Proposed Noise De-Embedding Procedure

As illustrated in Fig. 1(a), an open, short, and thru are employed in this proposed method. Here we also apply the

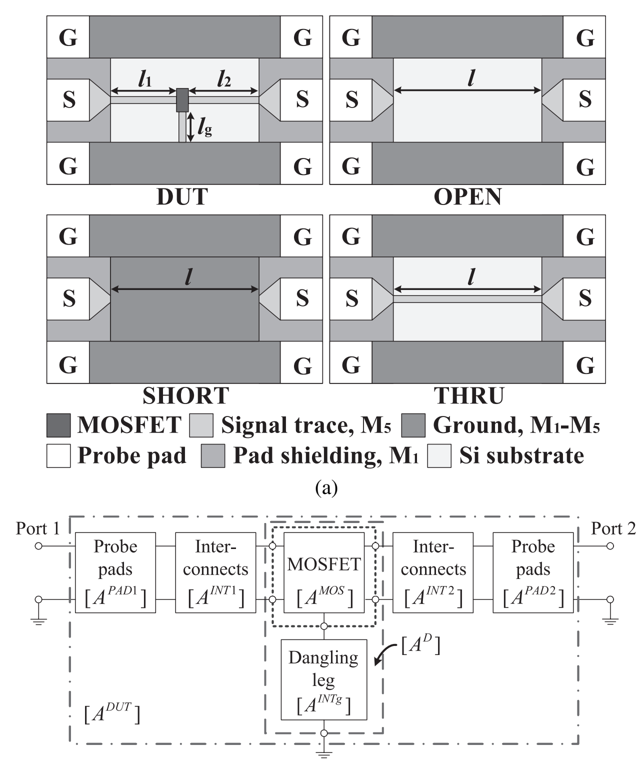

Fig. 1 Proposed noise de-embedding method. (a) Device under test (DUT) and de-embedding structures. (b) Suggested systematic model for the DUT.

Manuscript received December 25, 2008.
Manuscript revised April 10, 2009.

[†]The authors are with the Department of Communication Engineering, National Chiao-Tung University, Hsinchu, 300, Taiwan.
a) E-mail: richywan@ieee.org

DOI: 10.1587/transele.E92.C.1157

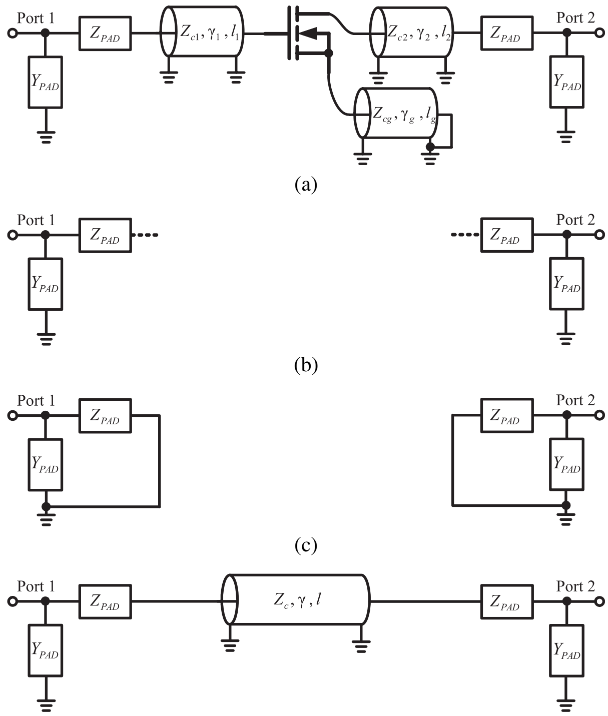

Fig. 2 Suggested parasitic models for the on-wafer test structures. (a) DUT. (b) Open standard. (c) Short standard. (d) Thru standard.

shielding technique [8] to improve the port-to-port isolation. The bulk-shielded open and short structures can be used to eliminate the shunt admittance and series impedance of the probe pads, respectively. The scalable interconnect parameters extracted from the thru structure can be used to efficiently subtract the parasitic effects of interconnects and dangling legs of the DUTs with different device geometries and interconnect lengths. Therefore, the proposed method is area-efficient and suitable for the automatic testing process in a mass-production line. Figure 1(b) is the systematic parasitic model for the fixtured MOSFET.

Figure 2 exhibits the semi-distributed model for the DUT and de-embedding structures. The *ABCD* matrices of the probe pads are

$$\left[A^{PAD1}\right] = \begin{bmatrix} 1 & Z^{PAD} \\ Y^{PAD} & 1 + Y^{PAD}Z^{PAD} \end{bmatrix}, \quad (1)$$

and

$$\left[A^{PAD2}\right] = \begin{bmatrix} 1 + Y^{PAD}Z^{PAD} & Z^{PAD} \\ Y^{PAD} & 1 \end{bmatrix}. \quad (2)$$

It should be noted that $Y^{PAD} = Y_{11}^{OPEN}$ and $Z^{PAD} = Z^{SHORTD}$, where $Z^{SHORTD} = (Y_{11}^{SHORT} - Y_{11}^{OPEN})^{-1}$, and $[Y^{OPEN}]$ and $[Y^{SHORT}]$ are the Y-parameters of the open and short converted from the S-parameter measurements. The thru dummy can be modeled as the probe pads and interconnect in cascade connection and its pad parasitics can be de-embedded using $[A^{INT}] = [A^{PAD1}]^{-1}[A^{THRU}][A^{PAD2}]^{-1}$, where the superscript "−1" denotes the inverse of the matrix, and $[A^{INT}]$ and $[A^{THRU}]$ are the *ABCD* matrices of the intrinsic interconnect and thru dummy, respectively. Consequently, the scalable interconnect parameters, such as characteristic impedance Z_c and propagation constant γ, can be evaluated as in [9]. Based on the above results, the parasitic effects of the input/output interconnects and dangling leg with arbitrary line length (l_1, l_2, and l_g) of a fixtured MOSFET can be efficiently reproduced from the *ABCD* matrices of a lossy transmission line

$$\left[A^{INTi}\right] = \begin{bmatrix} \cosh \gamma l_i & Z_c \sinh \gamma l_i \\ \frac{1}{Z_c} \sinh \gamma l_i & \cosh \gamma l_i \end{bmatrix}, i = 1, 2, g. \quad (3)$$

As referred to Fig. 1(b), the proposed noise de-embedding procedure is detailed as follows.

1) Measure the S-parameters $[S^{DUT}]$, $[S^{OPEN}]$, $[S^{SHORT}]$, and $[S^{THRU}]$ of the DUT, open, short, and thru, respectively.
2) Measure the noise parameters NF_{min}^{DUT}, R_n^{DUT}, and Y_{opt}^{DUT} of the DUT and calculate the correlation matrix $[C_A^{DUT}]$ as in [10].
3) Convert $[S^{OPEN}]$ and $[S^{SHORT}]$ to their Y-matrices $[Y^{OPEN}]$ and $[Y^{SHORT}]$, respectively, and calculate the *ABCD* matrices $[A^{PAD1}]$ and $[A^{PAD2}]$ of RF pads from (1) and (2).
4) Extract the intrinsic interconnect parameters using $[A^{INT}] = [A^{PAD1}]^{-1}[A^{THRU}][A^{PAD2}]^{-1}$ and calculate the interconnect characteristic impedance Z_c and propagation constant γ as in [9].
5) Calculate the *ABCD* matrices $[A^{INT1}]$, $[A^{INT2}]$, and $[A^{INTg}]$ of the interconnects and dangling leg as in (3).
6) Calculate the *ABCD* matrices $[A^{IN}]$ and $[A^{OUT}]$, which are respectively the parasitic networks at input and output ports, from $[A^{IN}] = [A^{PAD1}][A^{INT1}]$ and $[A^{OUT}] = [A^{INT2}][A^{PAD2}]$.
7) Convert $[S^{DUT}]$ to its *ABCD* matrix $[A^{DUT}]$ and calculate the *ABCD* matrix $[A^D]$ of the MOSFET with dangling leg using $[A^D] = [A^{IN}]^{-1}[A^{DUT}][A^{OUT}]^{-1}$.
8) Convert $[A^D]$ and $[A^{INTg}]$ to Z-matrix $[Z^D]$ and Y-matrix $[Y^{INTg}]$, respectively.
9) Calculate the Z-matrix $[Z^{MOS}]$ of the MOSFET without dangling leg from $[Z^{MOS}] = [Z^D] - [Z^{LEG}]$, where $[Z^{LEG}]$ is

$$\left[Z^{LEG}\right] = \begin{bmatrix} 1/Y_{11}^{INTg} & 1/Y_{11}^{INTg} \\ 1/Y_{11}^{INTg} & 1/Y_{11}^{INTg} \end{bmatrix}. \quad (4)$$

10) Convert $[Z^{MOS}]$ to $[A^{MOS}]$, where $[A^{MOS}]$ is the *ABCD* matrix of the intrinsic MOSFET.
11) Convert $[A^{IN}]$ and $[A^{OUT}]$ to their impedance matrices $[Z^{IN}]$ and $[Z^{OUT}]$, respectively.
12) Calculate the noise correlation matrices $[C_Z^{IN}]$, $[C_Z^{OUT}]$, and $[C_Z^{LEG}]$ from $[C_Z^{IN}] = 2kT\mathrm{Re}([Z^{IN}])$, $[C_Z^{OUT}] = 2kT\mathrm{Re}([Z^{OUT}])$, and $[C_Z^{LEG}] = 2kT\mathrm{Re}([Z^{LEG}])$.
13) Convert $[C_Z^{IN}]$ and $[C_Z^{OUT}]$ to their chain matrices $[C_A^{IN}]$ and $[C_A^{OUT}]$ using $[C_A^{IN}] = [T^{IN}][C_Z^{IN}][T^{IN}]^H$ and $[C_A^{OUT}] = [T^{OUT}][C_Z^{OUT}][T^{OUT}]^H$, where the superscript "H" denotes the Hermitian conjugate of the matrix, and $[T^{IN}]$

and $[T^{OUT}]$ are the transformation matrices [10].

14) Calculate the correlation matrix $[C_A^D]$ of the MOSFET with dangling leg as $[C_A^D] = [A^{IN}]^{-1}([C_A^{DUT}] - [C_A^{IN}])([A^{IN}]^H)^{-1} - [A^D][C_A^{OUT}][A^D]^H$ [5].
15) Convert $[C_A^D]$ to its impedance representation $[C_Z^D]$ using $[C_Z^D] = [T^D][C_A^D][T^D]^H$, where $[T^D]$ is the transformation matrix [10].
16) Calculate the correlation matrix $[C_Z^{MOS}]$ of the MOSFET without dangling leg as $[C_Z^{MOS}] = [C_Z^D] - [C_Z^{LEG}]$.
17) Convert $[C_Z^{MOS}]$ to its chain matrix $[C_A^{MOS}]$ using $[C_A^{MOS}] = [T^{MOS}][C_Z^{MOS}][T^{MOS}]^H$, where $[T^{MOS}]$ is the transformation matrix [10].
18) Calculate the intrinsic noise parameters NF_{min}, R_n, and Y_{opt} from the noise correlation matrix $[C_A^{MOS}]$ using

$$NF_{\min} = 1 + \frac{1}{kT}(\mathrm{Re}(C_{A12}^{MOS}) + \sqrt{C_{A11}^{MOS}C_{A22}^{MOS} - (\mathrm{Im}(C_{A12}^{MOS}))^2}) \quad (5)$$

$$R_n = \frac{C_{A11}^{MOS}}{2kT} \quad (6)$$

and

$$Y_{opt} = \frac{\sqrt{C_{A11}^{MOS}C_{A22}^{MOS} - (\mathrm{Im}(C_{A12}^{MOS}))^2} + j\mathrm{Im}(C_{A12}^{MOS})}{C_{A11}^{MOS}} \quad (7)$$

3. Results and Discussion

To verify the proposed de-embedding theory, the DUT and

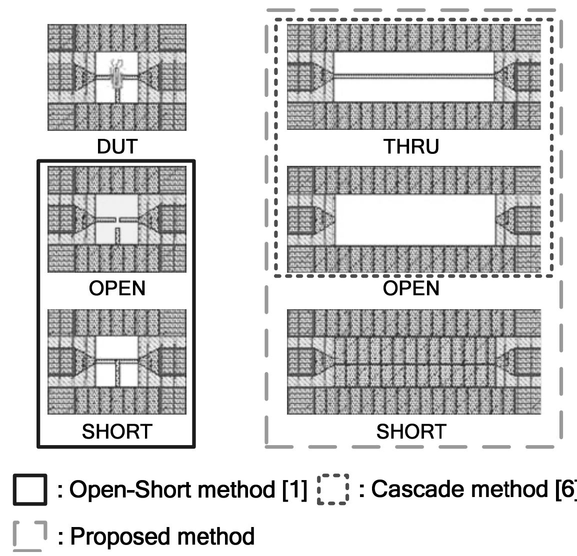

Fig. 3 Layout of the on-wafer MOSFET test key and de-embedding structures for the open-short method [1], cascade method [6], and proposed method.

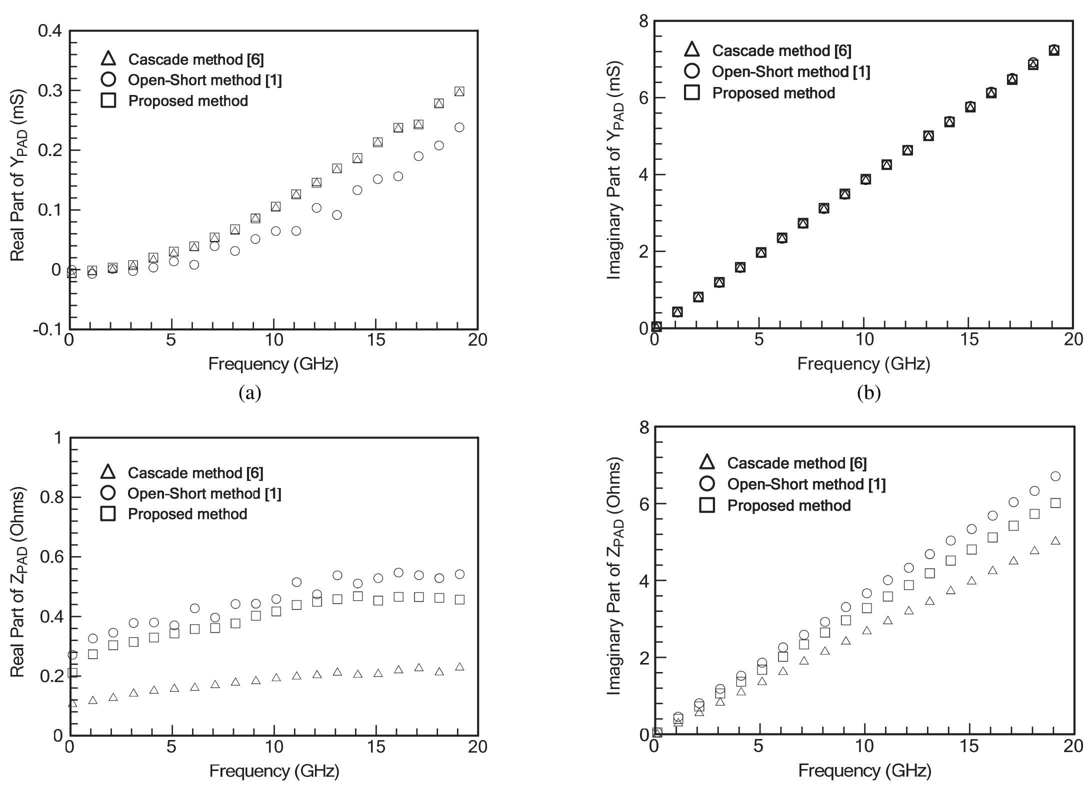

Fig. 4 Shunt admittance (Y_{PAD}) and series impedance (Z_{PAD}) of the feeding network, which comprises probe pads and interconnects except the dangling leg, estimated by conventional de-embedding methods, and proposed method. (a) Real part of Y_{PAD}. (b) Imaginary part of Y_{PAD}. (c) Real part of Z_{PAD}. (d) Imaginary part of Z_{PAD}.

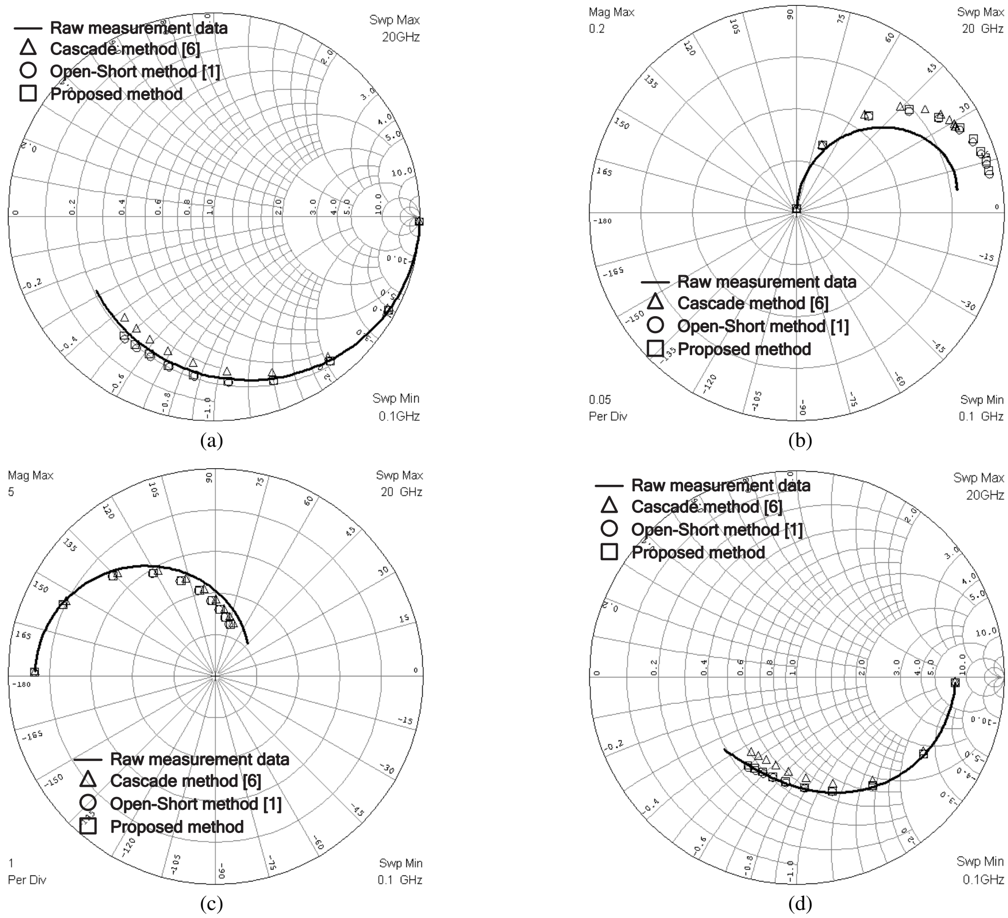

Fig. 5 Measured and de-embedded S-parameters of the fixtured NMOS transistor biased at V_{GS} = 1.065 V and V_{DS} =2.000 V (I_{DS} = 19.940 mA). (a) S_{11} (b) S_{12} (c) S_{21} (d) S_{22}.

de-embedding structures were fabricated using a 0.25-μm five-metal-layer CMOS process. The NMOS transistor with the dimensions of channel length (L_g) = 0.24 μm and channel width (W_g) = 160 μm was connected in a common-source configuration. The lengths of the 10-μm wide interconnects and dangling leg are $l_1 = l_2 = 50\,\mu$m and l_g = 42 μm. The on-wafer noise and S-parameter measurements were accomplished with the ATN NP5B Noise Parameter Measurement System. Before measuring S-parameters, the measurement system was calibrated using the short-open-load-thru (SOLT) calibration procedure and the reference planes were shifted to the probing planes, i.e. the probe tips. In this work, the pad parasitics were removed by using an open and short dummy, and the interconnect parasitics were removed by using a thru dummy. Since here we adopt the *ABCD* matrices of a lossy transmission line to model the interconnect parasitics, both the interconnect parasitics of signal trace and ground return would be properly estimated and removed. In addition, the short dummy in the proposed method has been carefully designed to minimize the de-embedding error [11]. For example, the probe pads are shielded and the pad-to-interconnect junctions are tapered to reduce the parasitic effects. Low impedance ground return of the short dummy is also achieved by a wide, smooth ground connection. Figure 3 illustrates the layout of the fabricated test keys and dummy structures for the open-short method [1], cascade method [6], and proposed method. Figure 4 shows the parasitic effects of the feeding network, which comprises probe pads and interconnects except the dangling leg, estimated by conventional de-embedding methods, and proposed method. As we can see, the proposed method can predict the pad and interconnect parasitics more accurately than the cascade method [6] do. The cascade method [6] employs only an open and thru dummy, and thus does not take the series impedance of probe pads into account. A slight difference between the open-short method [1] and proposed method is observed, and it might be caused by the additional metal connection of a short dummy used in [1]. Figure 5 displays the measured and de-embedded reflection coefficients (S_{11} and S_{22}) and transmission coefficients (S_{12} and S_{21}) of the fixtured RF MOSFET. It is shown that there are considerable differences between the proposed method and cascade method [6]. This is mainly because the parasitic effects of the dangling leg are ignored in the cascade de-embedding procedures [5], [6]. The proposed method further consider the series impedance of probe pads and dangling-leg parasitics, and therefore the results obtained from the proposed method

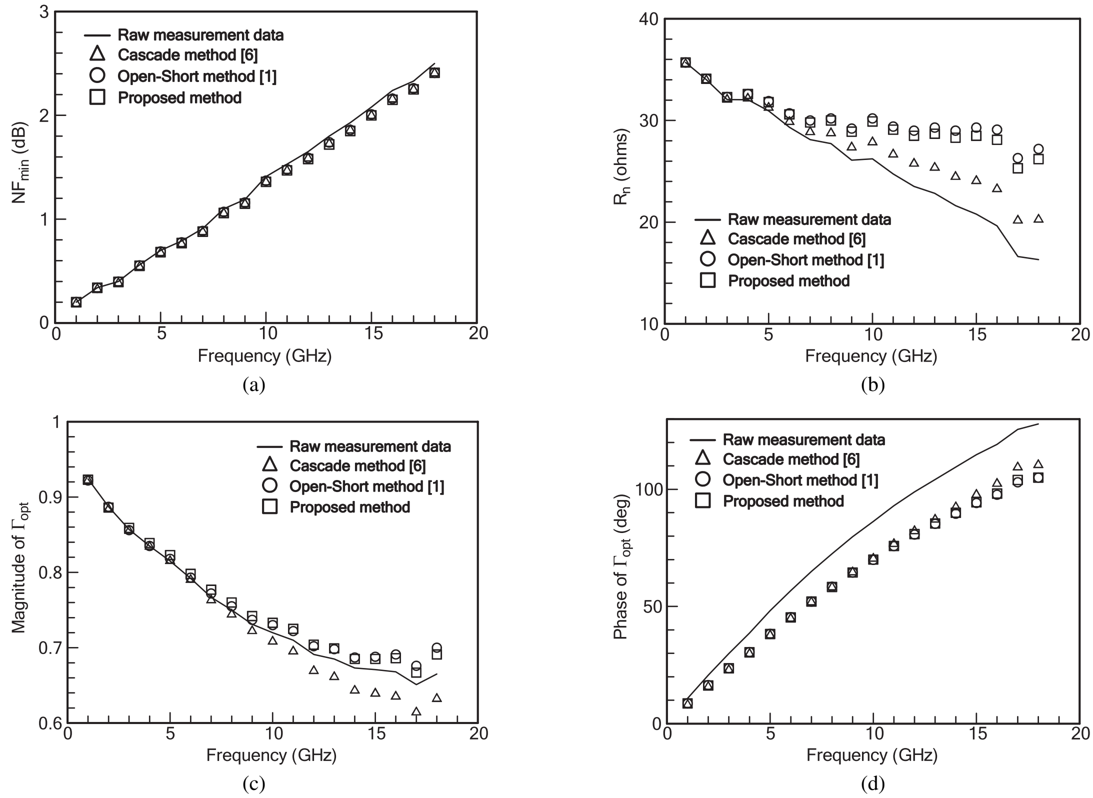

Fig. 6 Measured and de-embedded noise parameters of the fixtured NMOSFET biased at V_{GS} = 1.065 V and V_{DS} =2.000 V (I_{DS} = 19.940 mA). (a) NF_{min} (b) R_n (c) $|\Gamma_{opt}|$ (d) $\angle\Gamma_{opt}$ obtained from raw data, conventional de-embedding methods, and proposed method.

and the open-short method [1] are in excellent agreement over the entire frequency range. Figure 6 shows the measured and de-embedded noise parameters as a function of frequency. These results indicate that the intrinsic noise parameters obtained from the proposed method also agree well with those from the open-short method. They also demonstrate the parasitics of the dangling leg can affect the noise characteristics of a MOS transistor, especially for equivalent noise resistance (R_n) and optimized input reflection coefficient (Γ_{opt}) at higher frequencies. Based on the above results, we can substantiate our argument that the proposed method is accurate (as compared to the industry-standard open-short method [1]) and efficient. Since typically the conventional de-embedding methods need more than two dummy structures for each DUT, and thus, the chip area for modeling test keys would be considerable. The proposed method can reduce the chip area and characterization time in a mass-production line to about one-third of the conventional ones since only three dummy structures are needed for all DUTs on a wafer. In addition, the proposed method also can be applied to characterize various devices, such as varactor, resistor, BJT, MIM capacitor, etc.

4. Conclusions

In this study, a flexible noise de-embedding method suitable for on-wafer MOSFET characterization has been presented and verified. The bulk-shielded open and short structures are used to subtract the pad parasitics and the thru standard is used to remove the interconnect parasitics in gate, drain, and source terminals of the MOSFET. The de-embedding accuracy is validated up to 20 GHz and results show that the proposed method is accurate and efficient for characterizing the silicon-based active devices.

Acknowledgments

The authors would like to thank C.-H. Hsieh and C.-S. Chiu for their fabrication support, and X.F. Shao, and Y. Cho for useful discussions. This research was supported by the ROC (Taiwan) National Science Council under Grant No. 96-2221-E-009-001.

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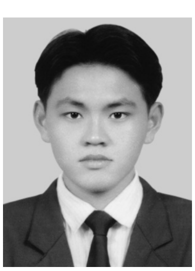
Yueh-Hua Wang was born in I-Lan, Taiwan, R.O.C., in 1971. He received the Electrical Engineering Diploma degree from the National Taipei Institute of Technology in 1991, and M.S. degree in communication engineering from the National Chiao Tung University in 1995, and is currently working toward the Ph.D. degree at NCTU. He is currently a Country Manager in Wavesat Inc, Taiwan. His current research focuses on wafer level device characterization.



Ming-Hsiang Cho was born in Kaohsiung, Taiwan, ROC, in 1976. He received the M.S. and Ph.D. degrees in communication engineering from the National Chiao Tung University, Hsinchu, Taiwan, ROC, in 2001 and 2008, respectively. From 2002 to 2006, he was with National Nano Device Laboratories, Hsinchu, Taiwan, ROC, working on wafer-level device characterization and RFIC testing. From 2006 to 2008, he was a Staff Engineer with the United Microelectronics Corporation, Hsinchu, Taiwan, ROC, working on RFCMOS technology development and characterization. He has authored or coauthored over 40 journal and conference papers. His present research interests include design of passive and active microwave components, antenna theory and applications, microwave measurement techniques, and device characterization. Mr. Cho is a member of Phi Tau Phi.

Lin-Kun Wu was born in Hsinchu, Taiwan, R.O.C., in 1958. He received the M.S. and Ph.D. degrees in electrical and computer engineering from the University of Kansas, Lawrence, in 1982 and 1985, respectively. From November 1985 to December 1987, he was a Post-Doctoral Research Associate at the Center for Research Inc., University of Kansas, where he was involved with microwave remote sensing and computational electromagnetics. In 1988, he joined the Department of Communication Engineering, National Chiao Tung University, Hsinchu, Taiwan, R.O.C., where he is currently a Professor. His current research interests include computational electromagnetics, biological effects and medial applications of electromagnetic energy, and electromagnetic compatibility.