A Highly Linear 125-MHz CMOS Switched-Resistor Programmable-Gain Amplifier

Cheng-Chung Hsu, *Student Member, IEEE,* and Jieh-Tsorng Wu, *Member, IEEE*

***Abstract*—A highly linear programmable-gain amplifier (PGA) is fabricated using a 0.35-μm CMOS technology. High linearity and constant wide bandwidth are achieved by using a high-gain amplifier with low input impedance and resistor-network feedback. The voltage gain is varied by digitally controlling the input switched resistors. The distortion of a switched resistor has been analyzed using the Volterra series. The PGA has a voltage gain varying from 0 to 19 dB, while maintaining a constant bandwidth of 125 MHz. The third-order intermodulation distortion is −86 dB at 10 MHz. The circuit dissipates 21 mW from a 3.3-V supply.**

***Index Terms*—Distortion, programmable-gain amplifier (PGA), switched resistor, variable-gain amplifier (VGA).**

I. Introduction

IN A MODERN communication receiver, the received signal is quantized by an analog-to-digital converter (ADC) so that complex signal processing can be performed in the digital domain. As shown in Fig. 1, a programmable-gain amplifier (PGA) is usually placed in front of the ADC, adapting the loss variation of the transmission channel in order to ease the dynamic range requirement for the ADC. The gain of the PGA is digitally controlled by an automatic gain control (AGC) loop. The linear-in-dB gain control for the PGA is usually required to achieve constant settling time of the AGC loop [1]. In the broad-band wireline receiver such as very high-speed digital subscriber lines (VDSL), the ADC usually requires 12-bit resolution with 0.2–11 MHz signal spectrum. It indicates that the PGA needs to have smaller than −74-dB total harmonic distortion (THD) over the signal spectrum, and amplifies the received signal by 0 to 20-dB gain control range [2], [3]. Signal attenuation may be required to accommodate large input signal swing [4]. The PGA needs to maintain its high linearity and low noise over the entire signal bandwidth as well as gain range.

High-speed PGAs have been realized using variable MOS transconductors in the disk drive applications [5], [6]. The linearity is limited by nonlinear characteristics of the transconductors. Although the resistor-network feedback closed-loop architectures can achieve high linearity [7], previous designs involved tradeoff among gain range, bandwidth, linearity, and power dissipation.

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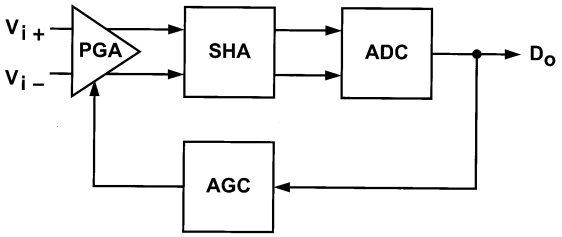

Fig. 1. Block diagram of an analog front-end.

This paper describes a PGA using an amplifier with low input impedance and resistor-network feedback to achieve high linearity and wide bandwidth simultaneously. The PGA meets the stringent requirements of the VDSL system. The paper is organized as follows. Section II analyzes various PGA architectures. Section III contains the distortion analysis of switched resistors. The proposed PGA is described in Section IV. Section V shows the experimental results, and finally, conclusions are given in Section VI.

II. PGA Architectures

The four basic gain variation techniques are shown in Fig. 2. Fig. 2(a) is a current divider. The dividing ratio is determined by the control voltage V_c. The quadratic characteristic of the current divider makes it difficult to realize a linear-in-dB gain setting. A predistorting stage for V_c may be required [8]. The overall linearity is limited by the input transconductor which generates I_i.

The transconductance of the source-coupled pair shown in Fig. 2(b) is varied by changing the bias current of the transistors [9]. The circuit's gain and the input-referred noise are proportional to g_m and $\sqrt{1/g_m}$ of the input transistors, respectively. When the input signal is weak, the large bias current is needed to obtain high-gain and low-noise performance. On the other hand, when the input signal is large, the low bias current can degrade the linearity.

In Fig. 2(c), the transconductance of the source-coupled pair is varied by changing the resistance of the degeneration resistor R_s. When the input signal is weak, small R_s is used to obtain high gain and low noise. When the input signal is large, large R_s is used to obtain low gain and high linearity. Thus, this topology can achieve constant signal-to-noise-and-distortion ratio for the fixed output level regardless of the gain settings.

Fig. 2(d) shows a high-gain amplifier with resistor-network feedback. Its voltage gain can be varied by changing the ratios of R_{f1}/R_1 and R_{f2}/R_2. High linearity can be achieved if the loop gain is large and the resistor network is linear. However, if the conventional operational amplifier is used [7], the variation of

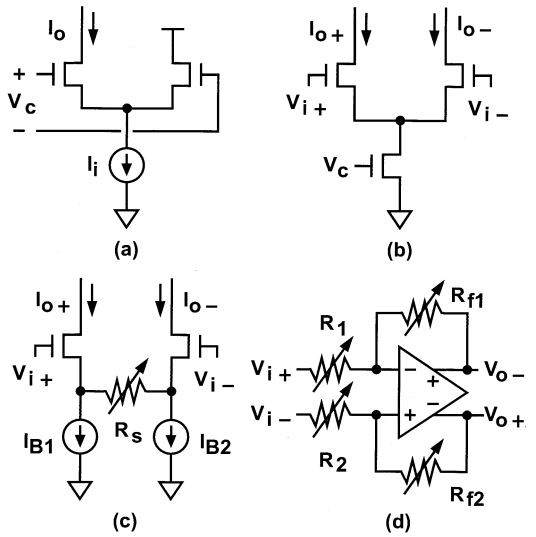

Fig. 2. Basic topologies for gain variation.

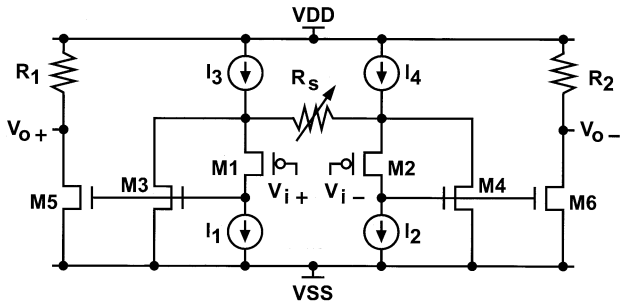

Fig. 3. Degenerated differential pair with the super-source follower.

the feedback factor results in variations of the bandwidth and the total harmonic distortion. When the circuit is designed to cover the worst-case scenario over the entire gain range, its power consumption is not optimized.

Fig. 3 shows a variation of the Fig. 2(c) topology [10]. The source-coupled transistors are replaced by two super-source followers [11], [12], consisting of M1-M3-I_1 and M2-M4-I_2. The improved output resistance of the super-source followers can reduce distortion when driving the resistive loads. However, the open-loop nature of the M3-M5 and M4-M6 current mirrors can limit the overall linearity of the circuit.

The circuit shown in Fig. 4 was derived from Fig. 3 [13]. It can also be shown as a variation of the Fig. 2(d) topology. As depicted in Fig. 4(a), it is a noninverting feedback configuration, with voltage gain approximately equal to $1+R_{f1}/R_1$. The input impedance of the amplifier is designed to be low. Thus, the PGA's feedback factor is a constant, if R_{f1} is not changed. The overall voltage gain is varied by changing R_1. One drawback of this configuration is that the voltage gain can only be larger than one. Signal attenuation is not possible.

A PGA with differential inverting configuration is shown in Fig. 5(a) [14]. The overall voltage gain is equal to the ratios of R_{f1}/R_1 and R_{f2}/R_2. Thus, the signal amplification and attenuation can be obtained easily through this configuration. Two voltage buffers, B1 and B2, are placed before the variable resistors R_1 and R_2 to provide high input impedance for the inputs.

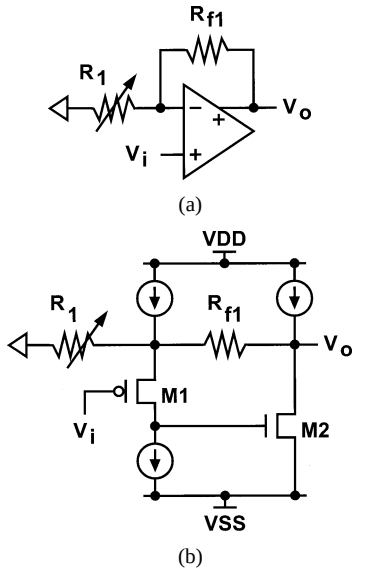

Fig. 4. (a) Noninverting resistor-network feedback configuration. (b) Single-ended circuit schematic.

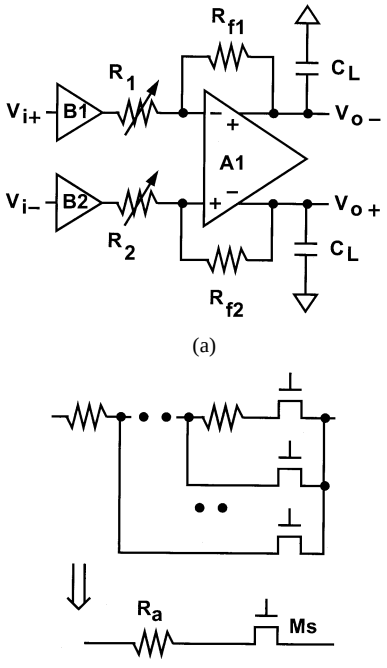

Fig. 5. Programmable-gain amplifier (PGA) simplified schematic.

With low input impedance of the input stage for the A1 amplifier and fixed resistances for R_{f1} and R_{f2}, the PGA can maintain a constant feedback factor, regardless of the values of R_1 and R_2. Thus, the amplifier can be optimized for minimal power dissipation at a specific bandwidth. The PGA's voltage gain can be varied by changing the resistances of R_1 and R_2. When the PGA is placed in an AGC loop, R_1 and R_2 resistors will be adjusted so that the average current signals flowing through the resistors remain constant, leading to little change of linearity at the PGA's outputs.

To facilitate digital gain control, the variable resistors, R_1 and R_2, are realized using the linear resistors in series with the MOSFET switches biased in the triode region, as shown

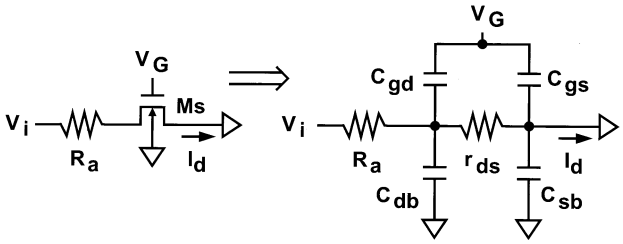

Fig. 6. Switched resistor circuit model.

in Fig. 5(b). Switched resistors can be used to implement low-distortion variable analog blocks [15]. Accurate prediction of the nonlinear effects of the MOSFET switch on the switched resistor is essential to obtain optimal tradeoff between the overall linearity and available bandwidth. Detailed analysis of the switched resistors is given in the following section.

III. Switched Resistor Analysis

The circuit model for a switched resistor is shown in Fig. 6. To minimize the distortion, the MOSFET switch is usually connected to the virtual ground, such as the summing node of the feedback network. We can describe the drain current of the MOS transistor using Taylor series expansion at $V_{ds} = 0$. Neglecting terms whose order is higher than three, the drain current is given by

$$I_d = g_{ds}V_{ds} + \alpha_2 V_{ds}^2 + \alpha_3 V_{ds}^3 \tag{1}$$

where g_{ds} is the drain–source conductance, α_2 and α_3 are the second- and third-order nonlinear coefficients, respectively. The body effect, mobility reduction, and carrier velocity saturation must be considered in order to understand their influence in the deep-submicron technology. Calculated from the simple level-two model of the device, the drain current can be expressed by [16]

$$\begin{aligned} I_D = {} & \frac{\mu_{\text{eff}} C_{\text{ox}} W}{L}(V_{gs} - V_{\text{FB}} - \phi_0 - \gamma\sqrt{\phi_0 + V_{sb}})V_{ds} \\ & - \frac{\mu_{\text{eff}} C_{\text{ox}} W}{2L}\left(1 + \frac{\gamma}{2\sqrt{\phi_0 + V_{sb}}}\right)V_{ds}^2 \\ & + \frac{\mu_{\text{eff}} C_{\text{ox}} W}{24L}\frac{\gamma}{(\phi_0 + V_{sb})^{\frac{3}{2}}}V_{ds}^3 \end{aligned} \tag{2}$$

where μ_{eff} is the effective surface mobility, C_{ox} is the gate-oxide capacitance per unit area, V_{FB} is the flat-band voltage, γ is the body-effect factor, and ϕ_0 is the surface potential. Considering the short-channel effects, the mobility term in the current–voltage characteristic shows a dependence on the voltage V_{ds} or channel electric field [17]. Therefore, it causes the distortion in the switched resistor. Neglecting terms whose order is higher than three, the mobility reduction caused by voltage V_{ds} can be also expressed as

$$\mu_{\text{eff}} = \mu_v \left[1 - \frac{1}{2(LE_c)^2}V_{ds}^2\right] \tag{3}$$

where μ_v is the carrier mobility when $V_{ds} \approx 0$ and E_c is the critical electric field which is approximately 6.09 MV/m for the 0.35-μm CMOS technology used in this paper.

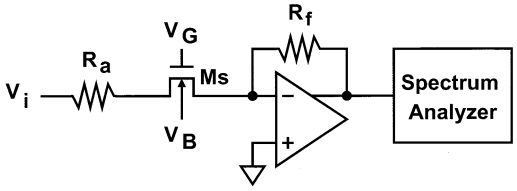

Fig. 7. Switched resistor distortion measurement setup.

For the weakly nonlinear network in Fig. 6, the second- and third-order harmonic distortions, HD_2 and HD_3, of I_d can be obtained by using the Volterra series (shown in the Appendix):

$$\text{HD}_2 = \frac{-V_i\alpha_2}{2R_t^2 g_{ds}^3} \tag{4}$$

$$\text{HD}_3 = \frac{-V_i^2\alpha_3}{4R_t^3 g_{ds}^4} + \frac{V_i^2\alpha_2^2}{2R_t^4 G_a g_{ds}^5} \tag{5}$$

where V_i is the input's peak amplitude, $G_a = 1/R_a$ is the linear conductance, and $R_t = R_a + r_{ds}$ is the equivalent resistance of the switched resistor. The HD_2 is proportional to the second-order nonlinear coefficient α_2. The HD_3 consists of two major contributors. One is the third-order coefficient α_3 of the drain current, and the other is due to the mixing of the second-order coefficient α_2 and the linear conductor G_a.

By using these expressions in (1), (2), and (3), (4) and (5) can be rearranged as

$$\text{HD}_2 = \frac{V_i}{2R_t^2\beta^2 V_{\text{ov}}^3}\left[\frac{1}{2} + \frac{\gamma}{4\sqrt{\phi_0 + V_{sb}}}\right] \tag{6}$$

$$\begin{aligned} \text{HD}_3 = {} & \frac{V_i^2}{4R_t^3\beta^3 V_{\text{ov}}^4}\left[\frac{V_{\text{ov}}}{2(L\cdot E_c)^2} - \frac{\gamma}{24(\phi_0 + V_{sb})^{\frac{3}{2}}}\right] \\ & + \frac{V_i^2 R_a}{2R_t^4\beta^3 V_{\text{ov}}^5}\left[\frac{1}{2} + \frac{\gamma}{4\sqrt{\phi_0 + V_{sb}}}\right]^2 \end{aligned} \tag{7}$$

where $\beta = \mu_v C_{\text{ox}} W/L$ is the device transconductance parameter, and $V_{\text{ov}} = g_{ds}/\beta$ is the gate overdrive voltage. For a given R_t, the distortions can be reduced by increasing g_{ds} which is equal to $\beta \times V_{\text{ov}}$. The mobility reduction on HD_3 shows up in the first term of (7); but it has the opposite effect against the body effect.

The setup shown in Fig. 7 has been used to measure the HD_2 and HD_3 of the switched resistors [16]. N-channel MOSFETs from a standard 0.35-μm CMOS technology are measured. The dc gain of the voltage-mode operational amplifier (opamp) is 94 dB, which is enough to suppress the distortions caused by the opamp itself. The input V_i is a sinusoidal signal with 0.5-V amplitude and 1-kHz frequency. The MOSFET's body effect parameter γ is found to be 0.52 $\text{V}^{1/2}$, and its substrate bias V_{sb} is set to 1.83 V.

Both measured and calculated distortions versus the MOSFET's r_{ds} are shown in Fig. 8. The MOSFETs with different size are all biased with a gate overdrive V_{ov} of 0.43 V. The resistance of R_a is adjusted so that the equivalent total resistance of R_t is 1 kΩ. The calculated values from (6) and (7) are in good agreement with the measured data.

The measured and calculated distortions versus the MOSFET's V_{ov} are shown in Fig. 9. The resistance of R_a is adjusted so that the equivalent total resistance of R_t is 1 kΩ.

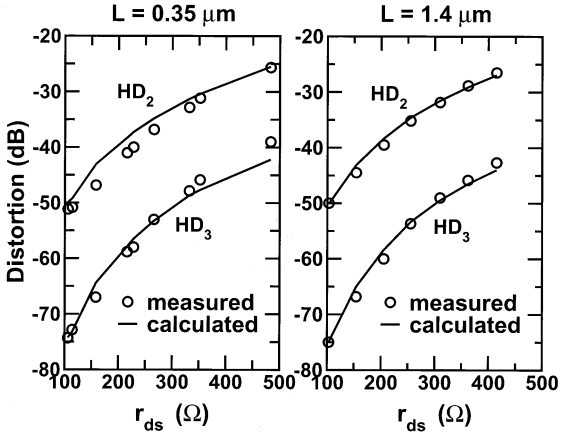

Fig. 8. Measured and calculated HD_2 and HD_3 versus r_{ds}.

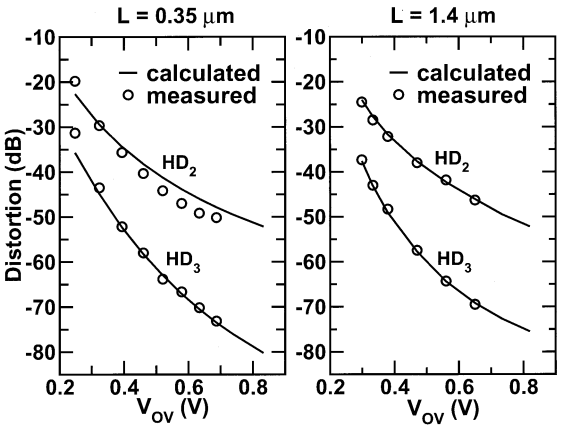

Fig. 9. Measured and calculated HD_2 and HD_3 versus V_{ov}.

Under the condition of a fixed R_t, the switched resistor exhibits an HD_2 inversely proportional to the third order of the gate overdrive, and an HD_3 inversely proportional to higher than fourth order of the gate overdrive. Thus, the most effective way to improve the linearity of a switched resistor is to increase the gate overdrive.

The measurement shows that the MOSFETs with different channel length have almost identical distortions if their channel resistances r_{ds} are adjusted to have the same value. Under the conditions of Fig. 8, the calculated first terms of (7) are approximately 34 and 60 dB less than the second terms of (7) for 0.35- and 1.4-μm channel length, respectively. Although the influence of the mobility reduction increases when the channel length decreases, it is still not significant for the 0.35-μm channel length. Thus, it can be concluded that the effect of mobility variation shown as the first term in (7) can be ignored for the 0.35-μm technology.

In most switched resistor applications, the MOSFET's gate overdrive is limited by the supply voltage. Distortions are reduced by using the transistors with larger channel width. But increasing the device's size also increases the gate-to-source capacitor and the source-to-substrate capacitor, shown as C_{gs} and C_{sb} in Fig. 6. If the capacitors are at the summing node of the feedback loop, such as the one shown in Fig. 5, they can degrade the stability and settling time of the circuit. Let $C_s = C_{gs} + C_{sb}$ is proportional to the transistor's channel width W, then we have

$$\mathrm{HD}_2 \propto \frac{1}{R_t^2 W^2} \propto \frac{1}{(R_t C_s)^2} \tag{8}$$

The HD_2 is inversely proportional to the square of time constant $R_t C_s$.

For the switched resistor, there is a tradeoff between linearity and bandwidth. The distortions versus $R_t C_s$ time constant are shown in Fig. 10 for the MOSFET switches with different channel length. The switches with shorter channel length should be used when the short-channel effects on the distortions are still not significant. For a fully differential circuit configuration, the HD_2 distortion can be suppressed effectively so that the HD_3 is dominant. When the total resistance of R_t and the design target of the HD_3 are given, it is possible to calculate the minimum device size. The capacitor C_s and HD_3 versus the channel width are shown in Fig. 11. The capacitor C_s increases with the channel width while the HD_3 decreases with the channel width. If the targeted HD_3 is -74 dB, the crossing point of the dash line and the line of HD_3 versus channel width determines the minimum device size. It corresponds to the minimum capacitance of C_s. Therefore, the switched resistors

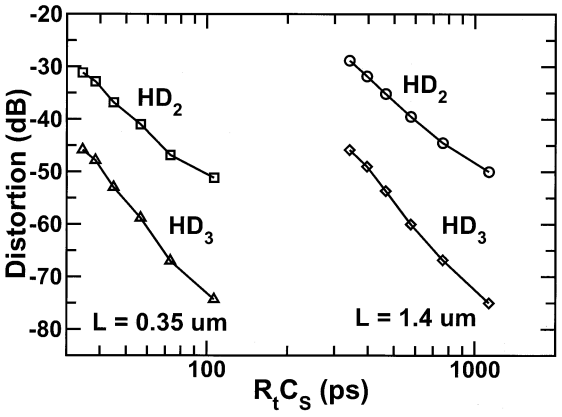

Fig. 10. Measured HD_2 and HD_3 versus the time constant $R_t C_s$.

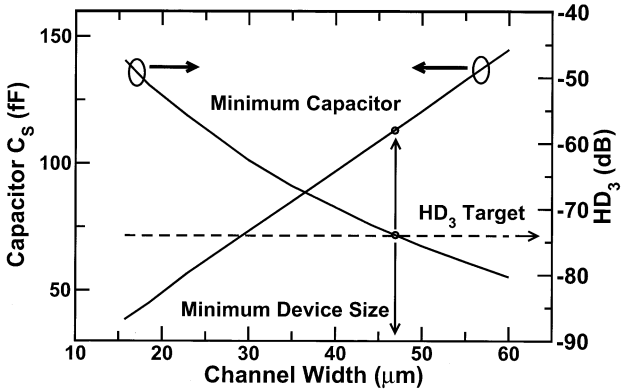

Fig. 11. For given R_t and targeted HD_3, the minimum device size can be determined. The channel length is 0.35 μm, $R_t = 1$ kΩ, $V_I = 0.5$ V, and $V_{\mathrm{ov}} = 0.43$ V.

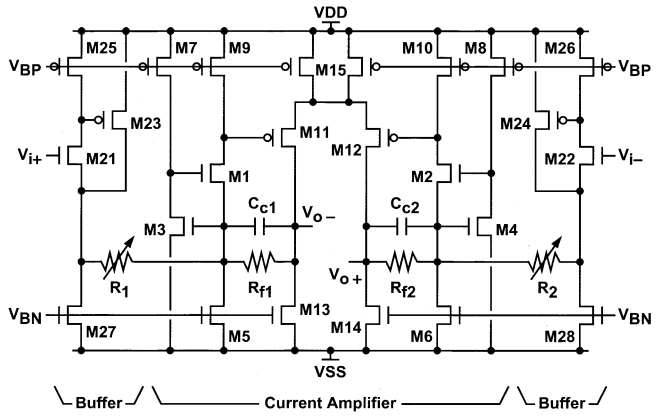

Fig. 12. Proposed PGA circuit schematic.

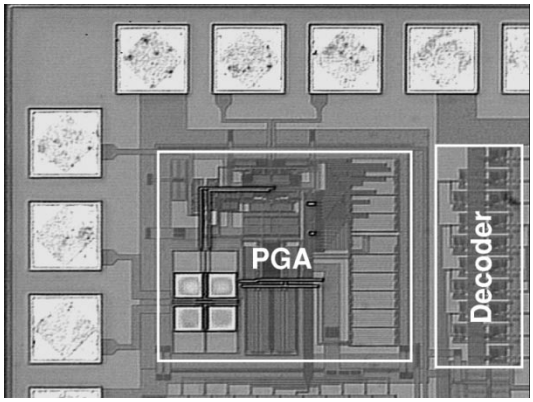

Fig. 13. Chip micrograph of the PGA.

can be effectively designed by calculating the minimum device size of the switches from (7), as follows:

$$\frac{W}{L} \approx \frac{1}{\mu_v C_{\rm ox}} \left(\frac{V_i^2 R_a}{8 {\rm HD}_3 R_t^4 V_{\rm ov}^5} \right)^{\frac{1}{3}} \tag{9}$$

The body effect is neglected in the above equation.

As shown in Fig. 6, the frequency dependence of the distortion is due to the nonlinear junction capacitors, C_{db} and C_{sb}. In most cases, the transistor's source node is connected to the virtual ground, and the nonlinear effects of C_{sb} can be ignored. Increasing the channel width of the MOSFET switch results in larger C_{db}, and potentially degrades the linearity. For given R_t and input voltage amplitude, the effect of the larger C_{db} on distortions is compensated by a smaller V_{ds} across the transistor, so that the contribution of C_{db} on distortion does not change significantly. With the following conditions, $R_t = 1$ kΩ, $V_i = 0.5$ V, $R_a = 0.905$ kΩ, $W/L = 47$ μm/0.35 μm, $C_{db} = 68$ fF, and $V_{\rm ov} = 0.43$ V, the estimated ${\rm HD}_3$ is -74 dB and the simulations show the distortions are unchanged versus the frequency sweep up to several hundred megahertz.

IV. PGA Circuit Description

Fig. 12 shows the circuit schematic of the proposed PGA based on the architecture in Fig. 5. The two super-source followers [11], [12], M21–M28, are voltage buffers to provide high input impedance. The variable resistors, R_1 and R_2, are two separate digitally controlled switched resistor networks. The high-gain current amplifier, consisting of M1–M15, has low input impedance and high output impedance. Transistors M1 and M2 form the input common-gate stages. The local feedbacks provided by the M3 and M4 transistors further reduce the input impedance of the M1 and M2 input stages. To enable the capability of common-mode rejection, the second gain stage is realized using the M11–M12 source-coupled pair. Not shown in the schematic is a continuous-time common-mode feedback (CMFB) which is applied to stabilize the common-mode voltage at the gates of the M11–M12 pair. The CMFB monitors the common-mode voltage and adjusts the currents of the M9 and M10 current sources. The transfer characteristic of the current amplifier is linearized by the two fixed resistors, R_{f1} and R_{f2}. The frequency compensation capacitors, C_{c1} and C_{c2}, create no right half-plane feedforward zero usually associated with the Miller compensation technique [18].

In addition to the nonlinear characteristics of the R_1 and R_2 switched resistors, other distortion sources in the PGA are suppressed by the negative feedbacks. The distortions caused by the two input super-source followers driving the resistive loads are suppressed by the internal feedback loops [16], which have the loop gain expressed as

$$T_1 = \frac{g_{m23} r_{o25} \times g_{m21} R_1}{2 + g_{m21} R_1} \tag{10}$$

where g_{m21} and g_{m23} are the transconductances of M21 and M23, respectively, and r_{o25} is the output resistance of M25. If $g_{m21} R_1 \gg 2$, the loop gain is insensitive to R_1 variation when changing the PGA's voltage gain. Then, the loop gain can be approximated by $g_{m23} r_{o25}$.

The distortions caused by the current amplifier are suppressed by the negative feedbacks using the R_{f1} and R_{f2} linear resistors. The loop gain can be expressed as

$$T_2 = \frac{g_{m11} r_{o9} (1 + s C_{c1} R_{f1})}{(1 + s C_p r_{o9}) \left[1 + s (C_{c1} + C_L) R_{f1} \right]} \tag{11}$$

where g_{m11} is the transconductance of M11, r_{o9} is the output resistance of M9, C_L is the output capacitive load, and C_p is the parasitic capacitance at the gate node of M11. By freezing the values of R_{f1} and R_{f2}, this loop gain and the distortion of the current amplifier remain unchanged, regardless of the PGA's voltage gain setting. At high frequencies, the zero caused by the compensation capacitors, C_{c1} and C_{c2}, can boost the loop gain, thus improving the amplifier's linearity. Simulation shows that, with $C_{c1} = C_{c2} = 0.3$ pF and $C_L = 2$ pF, the compensation capacitors can improve the linearity by 3 dB, comparing with the traditional Miller compensation.

V. Experimental Results

A PGA test chip was fabricated in a standard 0.35-μm CMOS technology. A micrograph of the chip is shown in Fig. 13. The active area occupies 0.18 $\rm mm^2$. Power dissipation is 21 mW from a 3.3-V supply, of which 6.6 mW is consumed by the two input voltage buffers. The resistance of $R_{f1,f2}$ is 5 kΩ, while the minimum and maximum resistances of $R_{1,2}$ are 0.42 and 4.2 kΩ, respectively. At the maximum gain setting,

TABLE I
PGA PERFORMANCE COMPARISON

Design	[6]	[10]	[13]	This Work
Bandwidth	85 MHz	15 MHz	100 MHz	125MHz
Gain Range	0∼30 dB	-2∼12 dB	5.6∼17 dB	0∼19 dB
Input Referred Noise	x	12 nV/$\sqrt{\text{Hz}}$	16.75 nV/$\sqrt{\text{Hz}}$	8.63 nV/$\sqrt{\text{Hz}}$
Distortion at 10 MHz	x	−60 dB (1 Vpp)	−67 dB (1.4 Vpp)	−74 dB (2 Vpp)
Distortion at 50 MHz	−43.1 dB (1.2 Vpp)	x	x	−55 dB (2 Vpp)
Technology	0.6 μm CMOS	0.5 μm CMOS	0.25 μm CMOS	0.35 μm CMOS
Total Current	2 mA	5 mA	2.7 mA	6.4 mA
Supply Voltage	5 V	5 V	2.5 V	3.3 V

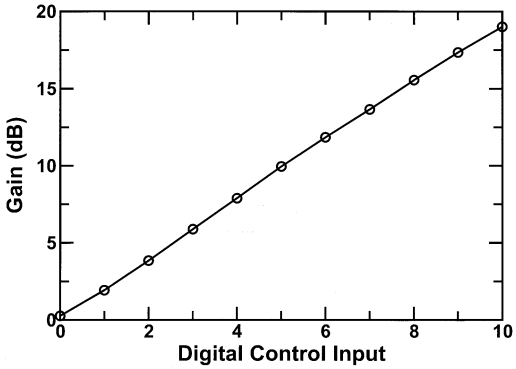

Fig. 14. Measured PGA's gain versus digital control input.

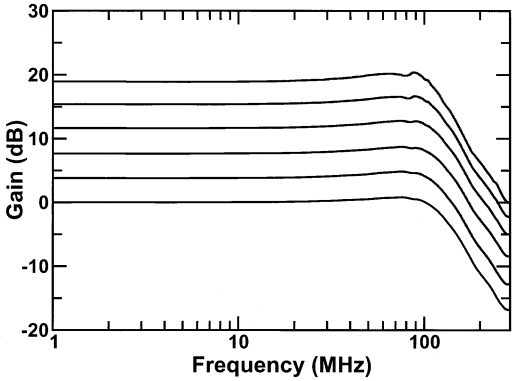

Fig. 15. Measured PGA's frequency response.

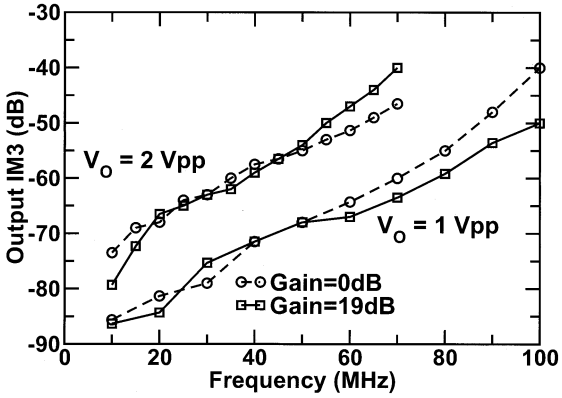

Fig. 16. Measured PGA's IM3 versus frequencies at 1 V_{pp} and 2 V_{pp} output.

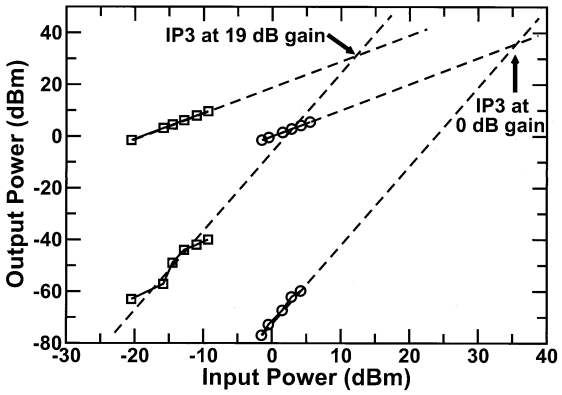

Fig. 17. Measured IIP3 at 10 MHz.

in the switched resistor of either R_1 or R_2, the linear resistor is 0.31 kΩ, and the MOSFET switch has a size of 20 μm/0.35 μm and an equivalent resistance of 0.11 kΩ. The HD_3 of this switched resistor is calculated to be −105 dB with 0.96-V gate overdrive voltage when the PGA's output is 2 V_{pp}. Since the targeted HD_3 is −74 dB, the design margin is 31 dB. Thus, the switched resistor does not dominate the linearity of the PGA. The switched resistors are weighted to obtain a dB-linear gain step with a step size of 2 dB. Fig. 14 shows the measured PGA's voltage gain versus the digital gain control input. The voltage gain can be varied from 0 to 19 dB. The maximum gain error is 1 dB at 20-dB gain setting. The measured PGA's frequency response is shown in Fig. 15. The PGA maintains a constant bandwidth of 125 MHz over the entire gain range, while driving 2-pF capacitive loads.

Fig. 16 shows the measured third-order intermodulation distortion (IM3) of the PGA at different frequencies when the outputs are 2 V_{pp} and 1 V_{pp}. As frequency increases, the IM3 worsens due to the attenuation of the amplifier's loop gain and the nonlinear junction capacitors at the output nodes. With 2-V_{pp} and 1-V_{pp} output, the IM3 are −74 and −86 dB at 10 MHz, respectively. The variation of the IM3 for different gain settings is less than 5 dB over the 0–80-MHz frequency range for 1-V_{pp} output. Fig. 17 shows the measured input-referred third-order intercept point (IIP3) at 10 MHz. The IIP3 are 35 and 12 dBm for 0 and 19 dB gain settings, respectively. The input-referred noise is 8.63 nV/$\sqrt{\text{Hz}}$ for 19-dB gain.

The PGA's performance is summarized in Table I and compared with several previously published designs. Note that the input-referred noise is calculated at the maximum gain setting. In [6], the PGA is based on the architecture in Fig. 2(b). Thus, the differential pair generates quadratic nonlinearities. In [10], the linearity is limited by the open-loop current mirroring from

the first stage to the second stage. In [13], good linearity can be achieved, but the noninverting configuration makes it difficult to realize low gain. This work has the best linearity performance among the PGAs with the similar bandwidth.

VI. Conclusion

PGAs using amplifiers with low input impedance and resistor-network feedback can achieve constant bandwidth and high linearity. The voltage gain is varied by digitally controlling the input switched resistors.

The distortion of a switched resistor can be analyzed using the Volterra series. It is caused by the nonlinear characteristic of the MOSFET switch, and depends on the transistor's device size and gate overdrive voltage, as well as the associated linear resistor. Closed-form formulas for HD_2 and HD_3 have been derived, and verified with the experimental data.

A PGA has been designed and fabricated using a standard 0.35-μm CMOS technology. The PGA has a voltage gain varying from 0 to 19 dB, while maintaining a constant bandwidth of 125 MHz. With 2-$\mathrm{V_{pp}}$ and 1-$\mathrm{V_{pp}}$ output, the IM3 are -74 and -86 dB at 10 MHz, respectively.

Appendix

A weakly nonlinear network can be represented by the sum of a linear term, a second-order term, and a third-order term, etc. [19]. This series is called the Volterra series. In Fig. 6, the Volterra series of the voltage V_{ds} can be described by

$$V_{ds} = H_1 V_i + H_2 V_i^2 + H_3 V_i^3 + \cdots \tag{12}$$

where V_i is the input's peak amplitude, and H_1, H_2, and H_3 represent the Volterra coefficients. The drain current can be calculated as

$$I_d = \frac{1}{R_a}\left[(1-H_1)V_i - H_2 V_i^2 - H_3 V_i^3 - \cdots\right] \tag{13}$$

where R_a is the linear resistor. Following the definition for harmonic distortions, the expressions for HD_2 and HD_3 in terms of the Volterra coefficients are given by

$$\mathrm{HD}_2 = \frac{V_i}{2}\frac{|H_2|}{|1-H_1|} \tag{14}$$

$$\mathrm{HD}_3 = \frac{V_i^2}{4}\frac{|H_3|}{|1-H_1|} \tag{15}$$

Calculating the Volterra coefficients [16], H_1, H_2, H_3 can be obtained as

$$1 - H_1 = \frac{1}{R_t G_a} \tag{16}$$

$$H_2 = \frac{-\alpha_2}{R_t^3 G_a g_{ds}^3} \tag{17}$$

$$H_3 = \frac{-\alpha_3}{R_t^4 G_a g_{ds}^4} + \frac{2\alpha_2^2}{R_t^5 G_a^2 g_{ds}^5} \tag{18}$$

where $R_t = R_a + r_{ds}$ is the equivalent resistance of the switched resistor and $G_a = 1/R_a$ is the linear conductance. From (14)–(18), the distortions are

$$\mathrm{HD}_2 = \frac{-V_i \alpha_2}{2R_t^2 g_{ds}^3} \tag{19}$$

$$\mathrm{HD}_3 = \frac{-V_i^2 \alpha_3}{4R_t^3 g_{ds}^4} + \frac{V_i^2 \alpha_2^2}{2R_t^4 G_a g_{ds}^5}. \tag{20}$$

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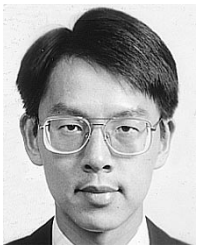

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