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2008 J. Phys.: Conf. Ser. 100 042045

(http://iopscience.iop.org/1742-6596/100/4/042045)

Impact of Charge Trapping Effect on Negative Bias Temperature Instability in P-MOSFETs with HfO_2/SiON Gate Stack

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Abstract. In our study, we systematically investigated the behavior of charge trapping in P-MOSFETs with HfO_2/SiON gate stack. We found that typical linear extrapolation does not work well for the lifetime extraction at normal operation condition since the polarity of dominant trapped charge in high-κ dielectric is not the same at lower and higher stress voltage regimes. This phenomenon is considered the competition of hole trapping and electron trapping with respect to applied gate voltages. Besides, the results of AC stress reveal the distinct responses to electrons and holes. It indicates that electrons can easily follow the AC signal while holes seem to need more time for the response at AC stress.

1. Introduction

High-permittivity (high-κ) materials are introduced as the alternative gate dielectrics since they can significantly suppress the intolerable leakage current presented in the ultra-thin conventional SiO_2.[1-3] To date, although a lot of investigations have been done with respect to high-κ dielectrics, many of challenges still remain [4-6]. One of the most critical problems in high-κ dielectric are the charge trapping effect in the bulk of high-k materials since the phenomena will have significant impacts on device performances and reliabilities [7-9]. In this work, we systematically investigated the behaviors of charge trapping effect in P-MOSFETs with HfO_2/SiON gate stack. Many methodologies were employed to evaluate its impact on the electrical properties and reliability of the P-MOSFETs with HfO_2/SiON gate stack, such as negative bias stress instability (NBTI), measurements with DC and AC stresses. We found that the polarity of net trapped charge in high-κ dielectric is not the same in the regimes of applied gate voltages for DC case; while the trapping of high-κ dielectric is strongly dependent on the frequency and duration of AC stress.

2. Experimental

In this study, P-MOSFETs were fabricated on (100) n-type wafers. After a standard RCA cleaning with a final HF-dip. The N_2O surface treatment performed a 0.7nm thin interfacial oxyntride layer

(SiON) using rapid thermal processing at 700°C. A 3nm HfO_2 layer was deposited by MOCVD system at 500°C, followed a high temperature post deposition annealing in an N_2 ambient at 700°C for 20s to improve the film quality. A polycrystalline silicon layer was utilized to be the gate electrode, and the dopant activation was conducted at 950°C by rapid thermal annealing for 20s in an N_2 atmosphere. After passivation, contact holes formation, Al metallization and patterning, the forming gas annealing at 400°C was finally performed for 30 minutes to complete the device fabrication. In NBTI investigations, interface trap density (N_{it}) was extracted by charge pumping method. The increase of total trap density was calculated from $\Delta N_{tot} = C\Delta V_{th} / qA_G$, where C is gate capacitance and A_G is the gate area.

3. Results and Discussion

3.1. Characteristics at DC Stress

Figure 1(a) and (b) showed the variations of ΔV_{th} and ΔN_{it} as a function of stress voltage V_g over time.

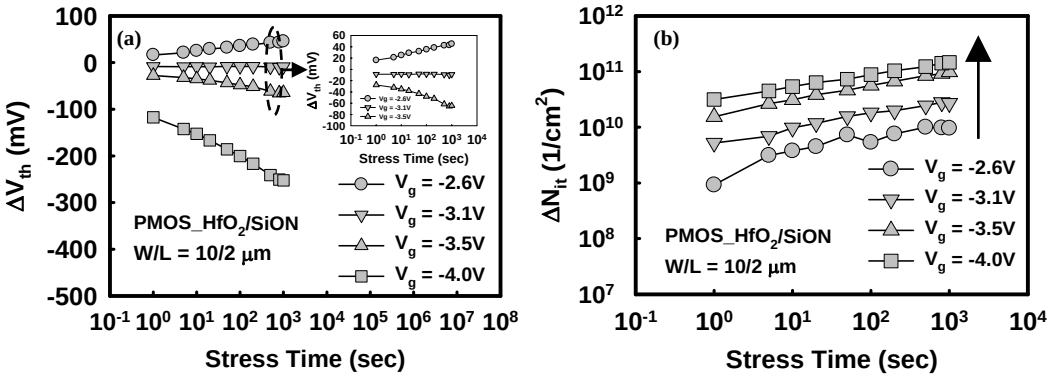

Figure 1. (a) ΔV_{th} versus stress time under various stress conditions at 25℃. (b) ΔN_{it} versus stress time is as a function of stress voltages.

In figure 1(a), the resultant ΔV_{th} was negative and it became more significant with larger stress voltage when $|V_g| > 3.1V$. This experimental result has been well known as a result of the hole trapping in the bulk of high-k dielectrics [10-11]. Nevertheless, the tendency of NBTI results was not monotonic as we expected when we kept going on lowering the stress voltage. When $|V_g| < 3.1V$, an apparent turnaround phenomenon was observed that the ΔV_{th} turned negative trend into positive trend since the type of the dominant trapped charge in the dielectrics has changed from hole to electron. Furthermore, the degradation became more significant with further deceasing stress voltage indicating that electron trapping dominates at lower applied gate voltages. This result strongly implies that the mechanism of ΔV_{th} in the high-κ dielectrics is not unique since the charge trapping effect in the bulk of HfO_2 is distinct in different stress voltage regimes. On the other hand, figure 1(b) illustrated the variation of ΔN_{it} that increased monotonically with increasing stress voltage and represented only relatively small influence on ΔV_{th}. Therefore, it is considered that the phenomenon is closely related to the bulk traps rather than the interface states.

This charge trapping effects can be also verified by the results of I_{cp} measurements shown in figure 2. As expected, the interface degraded much seriously with increasing stress voltage. However, the different charge trapping effects were found in I_{cp} measurements. As stress voltage = -3.0V, an obvious positive shift of I_{cp} indicated the apparent electron trapping. On the contrary, as stress voltage = -3.3V and -3.5V, the negative shift of I_{cp} referred to the hole trapping. A turn around point with net trapping free except the generation of interface sites was observed between these two different charge

trapping mechanisms at stress voltage = -3.1V. The experimental result here is fully consistent with that presented in Figure 1.

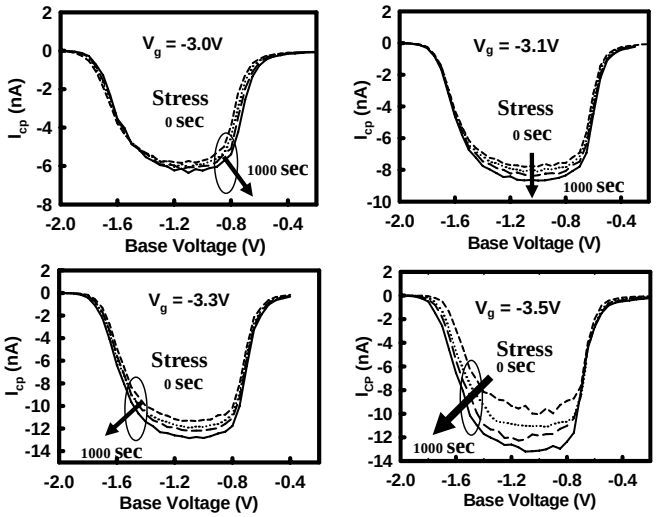

Figure 2. Charge pumping current under various stress conditions (-3.0V, -3.1V, -3.3V, -3.5V, stress 1000 sec).

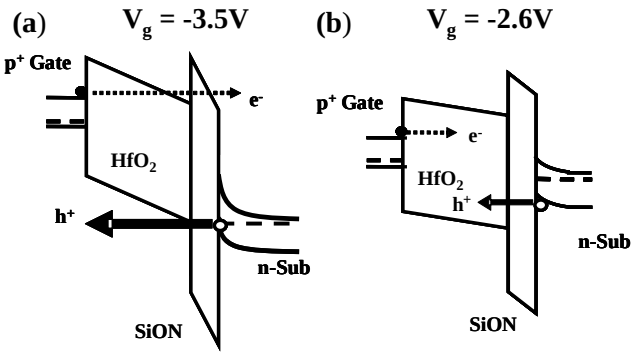

Figure 3. Band diagrams of HfO_2/SiON gate stack under (a) Stress Voltage = -3.5V (b) Stress Voltage = -2.6V.

Figure 3(a) and (b) showed the band diagrams under bias conditions of -3.5 and -2.6V, respectively. As stress voltage = -3.5V, large probability of hole injection from Si substrate induced significant negative ΔV_{th} according to the obvious band bending under large voltage. On the contrary, when stress voltage = -2.6V, the hole injection was suppressed by interfacial layer while the dominant mechanism changed from hole trapping to electron trapping. Therefore, the NBTI behaviors reveal a strong dependence on applied gate voltage.

3.2. Characteristics at AC Stress

Figure 4 and Figure 5 represented the ΔV_{th} and ΔN_{it} as a function of frequency and duty cycle, respectively.

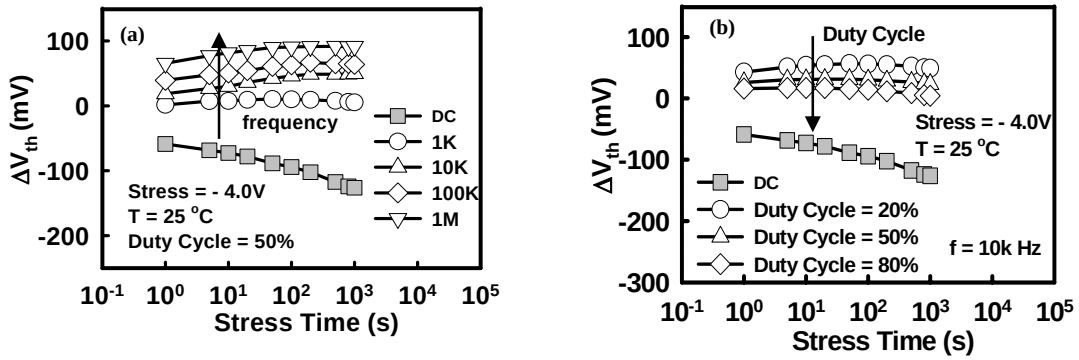

Figure 4. ΔV_{th} versus stress time under various (a) frequency and (b) duty cycle at 25℃

We clearly observed that ΔV_{th} appears to be strongly dependent on frequency and duty cycle while ΔN_{it} depicts almost no frequency and duty cycle dependence. As a result, we again conclude that the strong dependences of ΔV_{th} during AC stress on frequency and duty cycle are intimately related to the

characteristics of bulk traps instead of interface states as what we have observed at DC stress. In the AC stress conditions, it is considered that holes do not have enough time for tunneling and getting trapped while, in strong contrast, electrons can easily follow the varying AC signal and get trapped during the on-period.

From all above experimental data, we conclude that electron and hole trappings are both likely to emerge in the high-κ dielectrics. The dominant trapped species will be determined by the magnitude of stress voltage, the testing temperature and stress signal shape. Figure 6 demonstrated that the modified lifetime prediction in P-MOSFETs with HfO_2/SiON gate stack will no longer be linear since the polarity of dominant trapped charge in high-κ dielectric is not the same different voltage regimes.

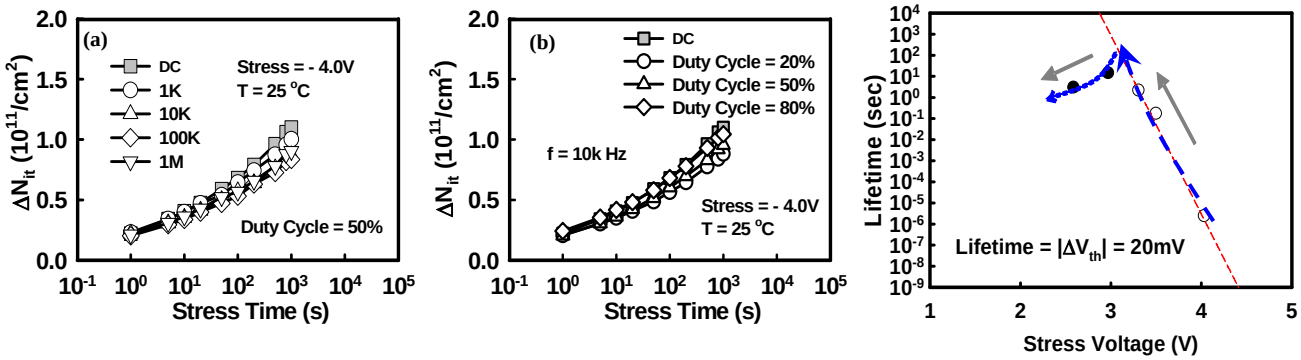

Figure 5. ΔN_{it} versus stress time under various (a) frequency and (b) duty cycle at 25℃.

Figure 6. Modified lifetime prediction of NBTI degradation.

4. Conclusions

In our study, we systematically investigated the behaviors of negative bias temperature instability of P-MOSFETs with HfO_2/SiON gate stack. We demonstrated that an anomalous NBTI behavior was observed since the type of dominant trapped charge in the bulk of HfO_2 is not the same in whole regimes of stress voltages. The linear lifetime extraction is not able to accurately predict the lifetime at normal operation. Finally, the trapping of high-κ dielectric is strongly dependent on the frequency and duration of AC stress.

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