Light-Induced Sidegating Effect in GaAs MESFET's

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Abstract—**Light sensitivity of sidegating effect in GaAs MESFET's is investigated by performing two-dimensional numerical simulations on realistic sidegate structures. Mechanism of the light-induced sidegating is identified and compared with alternative mechanisms of sidegating including trap-fill-limited conduction and conduction through the Schottky-i-n(sidegate) structure. Ionization of hole traps in the substrate by capturing the photo-generated holes is found to be the major cause of light-induced sidegating effect which occurs even at very low sidegate voltages. In the presence of the hole traps occupied by holes, the potential distribution in the electron-trap-rich substrate becomes similar to that in the hole-trap-rich substrate, i.e., the negative voltage applied to the sidegate is carried over to the channel-substrate interface.**

I. Introduction

SIDEGATING effect is the modulation of FET's drain current by applying a negative voltage to an adjacent electrode called the sidegate. Since this is the key problem that limits the integration scale of GaAs IC, much effort has been made to understand and overcome the effect.

Several models have been proposed to explain the typical features measured in the sidegating characteristics. For example, correlation between the reduction in drain current and abrupt increase in substrate leakage current was attributed to the electron injection and trap-fill-limited (TFL) conduction [1]. The hysteresis or *S*-type negative differential conductivity associated with the sidegating threshold was explained with trap-impact-ionization model [2]. Recently, it is recognized that the presence of Schottky contacts directly on the semi-insulating (SI) substrate play an important role in sidegating effect [3]–[6]. Two-dimensional numerical simulations with well controlled test structure arrangement, device and substrate parameters have shown that the temperature dependence [7], hysteresis associated with the sidegating threshold [8] as well as the suppression of sidegating effect by using a Schottky shielding bar [4] or ion bombardment [9] can be explained consistently with the conduction through the Schottky-i-n(sidegate) structure which injects holes into the SI substrate and causes the sidegating [4].

So far, light-sensitivity of the sidegating effect has been recognized and simply attributed to the increase of substrate current due to optically generated carriers [10]–[12]. In this work, the detailed mechanism of light-induced sidegating effect in GaAs MESFET's is analyzed and compared with other common mechanisms of sidegating, including the Schottky-i-n(sidegate) and TFL conduction in the n(sidegate)-i-n(FET).

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II. Models and Device Structures for Simulation

A two-dimensional, two-carrier device simulation program based on the drift-diffusion formulation is used for the numerical simulations. In this program, transport of free carriers is calculated by solving current continuity equations and Poisson's equation. The emission and capture of free carriers through deep levels follow the Shockley–Read–Hall model. Constant electron mobility at low fields and velocity saturation beyond a critical field was used for the velocity-field relationship. The Schottky barrier height was assumed to be 0.8 V. Current transport across the Schottky-barrier junctions is described by the thermionic emission-diffusion theory.

The semi-insulating substrate was assumed to contain deep donors that compensate for shallow acceptors, similar to the case of undoped LEC GaAs substrates. The shallow acceptor concentration was taken to be 10^{15} cm^{-3}. The midgap donors included electron traps and hole traps, whose concentrations were 10^{16} cm^{-3} and 10^{15} cm^{-3}, respectively. Capture cross-sections and energy levels of these traps are listed in Table I. These values, similar to those used in [13], were chosen to emphasize the relationship between the trap properties and the sidegating effect so that the respective roles of the deep traps can be more easily identified. We have confirmed that the results presented in this paper are not significantly affected as long as the trap types are preserved and the hole traps lies below the electron traps. The existence of hole traps has been found essential to the sidegating effect [4], although similar results can be obtained if the hole traps are deep acceptors instead of deep donors.

The device structure shown in Fig. 1 was used in the simulation, with and without the Schottky contact on the SI substrate [3], [4]. This Schottky contact may represent a small portion of the Schottky gate that extends onto the semi-insulating substrate or a section of an interconnection line. The FET had a 1 μm gate with a 3 μm source to drain spacing. The FET's channel was 0.12 μm thick and uniformly doped to 10^{17} cm^{-3}. In the simulation, the Schottky contact, the source and gate contacts of the FET were all grounded.

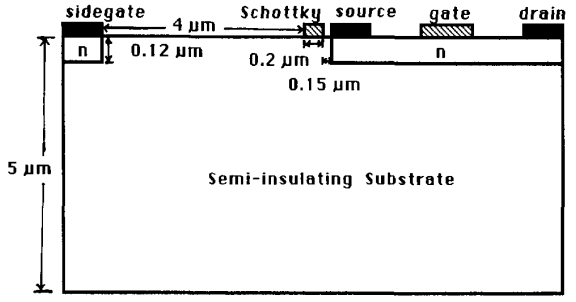


Fig. 1. Device structure used in the simulations.

TABLE I
PARAMETERS RELATED TO TRAPS

Category	Electron Capture Cross-Section (cm^2)	Hole Capture Cross-Section (cm^2)	Energy Level $Ec - Et$ (eV)
Electron Trap	1×10^{-13}	3×10^{-16}	0.715
Hole Trap	3×10^{-16}	1×10^{-13}	0.745

The effects of illumination on substrate conduction and sidegating have been treated by having a photon flux incident on the top surface of the surface. Because the metal contacts are not transparent to light, it is assumed that no light can penetrate to the regions below these contacts. The photogeneration rate of electron-hole pairs, G, is an exponentially decaying function of the depth, y, from the top surface as follows:

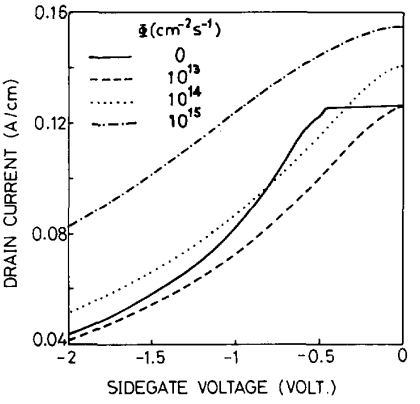
$$G = \Phi\alpha \exp(-\alpha y).$$

The constant absorption coefficient, α, was set to 10^4 cm^{-1} and the incident photon flux density, Φ, was varied from 10^{13} to 10^{15} $cm^{-2}\,s^{-1}$. This is approximately equivalent to the condition of illumination from a microscope light.

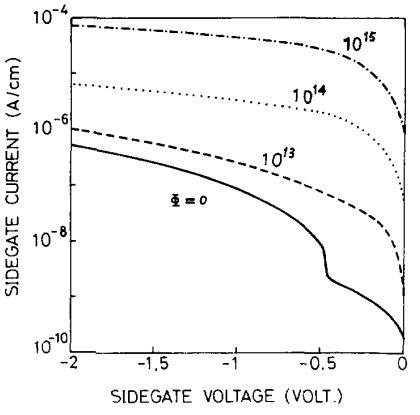
III. Results and Discussion

A. With the Schottky Bar: Sidegating Induced by Light Versus Schottky-i-n Conduction

First, the structure with a small Schottky bar placed between the FET and sidegate (see Fig. 1) is simulated. Fig. 2(a)–(c) show the calculated drain current, sidegate leakage current, and Schottky contact current as functions of negative sidegate voltage under different illumination conditions. Qualitatively, these results are in good agreement with the typically measured sidegating characteristics [10]–[12] as described in the following. In the dark, the rapid decrease in drain current and abrupt increase in sidegate current occur when the negative sidegate voltage exceeds a threshold. This sidegating threshold has been found to correlate with the conduction between the sidegate and the Schottky contact on SI substrate, or the hole injection from the Schottky contact [4]. While under illumination, the drain current increases with the incident photon flux but starts decreasing with the negative sidegate voltage even from sidegate voltages close to zero.



(a)



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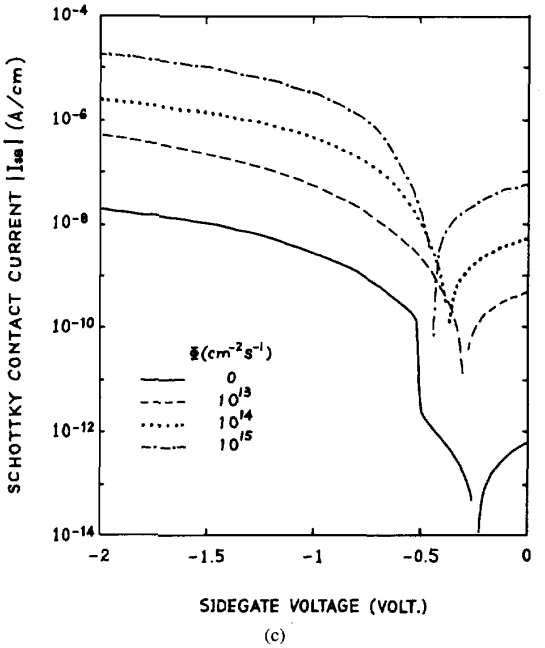

(c)

Fig. 2. Calculated (a) drain current, (b) sidegate current, and (c) Schottky contact current as functions of the sidegate voltage with the incident photon flux density equal to 0 (solid line), 10^{13} (dashed line), 10^{14} (dotted line), and 10^{15} $cm^{-2}\,s^{-1}$ (dash-dotted line).

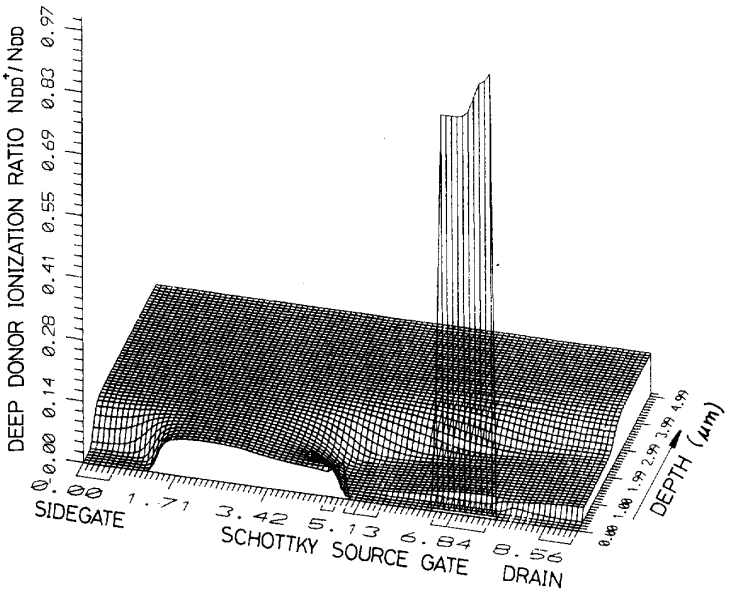

Fig. 3. The profile of ionization ratio of deep donors in the structure with a Schottky contact on the SI substrate, both in the dark and under illumination. The sidegate is biased at −2 V.

The former is due to the photovoltaic effect occurring at the channel/substrate interface [14]. The latter is the light-induced sidegating effect that causes the sidegate voltage to drop across the channel/substrate interface.

After the sidegating effect occurs, the profiles of ionization ratio, N_{dd}^{+}/N_{dd}, of all the deep donors are about the same for the cases in the dark and under illumination. This implies that the mechanism of light-induced sidegating is, *in a way*, similar to that of the sidegating caused by Schottky-i-n(sidegate) conduction. Fig. 3 shows the profile at sidegate voltage equal to −2 V. The ionization ratio is defined as the ratio of deep donors which become ionized by losing an electron or capturing a hole. It can be seen that N_{dd}^{+}/N_{dd} is close to 0.1 in almost the whole SI substrate except in the regions under and around the FET and the sidegate, where N_{dd}^{+}/N_{dd} is close to zero. Since the concentration of shallow acceptors are about 1/10 that of deep donors in the SI substrate, ionization ratio close to 0.1 corresponds to the charge neutrality of the substrate. While in the regions with N_{dd}^{+}/N_{dd} close to zero, the substrate is negatively charged due to the ionization of shallow acceptors. It is the negative charge under the FET that causes the depletion of channel electrons and results in the decrease of drain current.

To further clarify how the light-induced sidegating occurs, changes (with the illumination condition as well as sidegate voltage) in the respective ionization ratios of electron traps and hole traps under mid-gate are plotted in Fig. 4. At zero sidegate voltage and in the dark, hole traps are completely neutral and the shallow acceptors are compensated by electron traps only. Under illumination at zero sidegate voltage, about 85% of the hole traps become ionized by capturing the photo-generated holes, while the ionization ratio of the electron traps is reduced to 1.5%. In this case, the SI substrate is similar to the hole trap rich (HTR) substrate investigated in [4] in that they both contain a large number of hole traps which are occupied by holes. This point is further supported by the close similarity between the sidegating characteristics (see Fig. 2) of this illuminated SI substrate, which is electron trap rich, and those of the hole trap rich substrate reported in [4] (Fig. 2). According to [4] and [15], in the presence of these hole traps, the potential profile is nearly flat in the whole SI substrate and the negative voltage applied to the sidegate would be carried to the vicinity of the channel/substrate interface. Those ionized hole traps under the channel emit holes in response to the hole depletion, result in a negatively charged region there, and cause the reduction of the drain current.

B. Without the Schottky Contact: Sidegating Due to Illumination Versus Trap-Fill-Limited Conduction

From the results presented in the previous section it does not seem that the presence of the Schottky contact plays any role in the light-sensitivity of sidegating. To verify this point, the structure shown in Fig. 1 is simulated without the Schottky contact. Fig. 5 shows the calculated drain current and sidegate current as functions of negative sidegate voltage. As expected, when the top surface is illuminated with a photon flux of 10^{13} cm^{-2} s^{-1}, the drain current decreases rapidly, starting from zero sidegate voltage. The resulting profile of ionization ratio of deep donors is also similar to the one shown in Fig. 3.

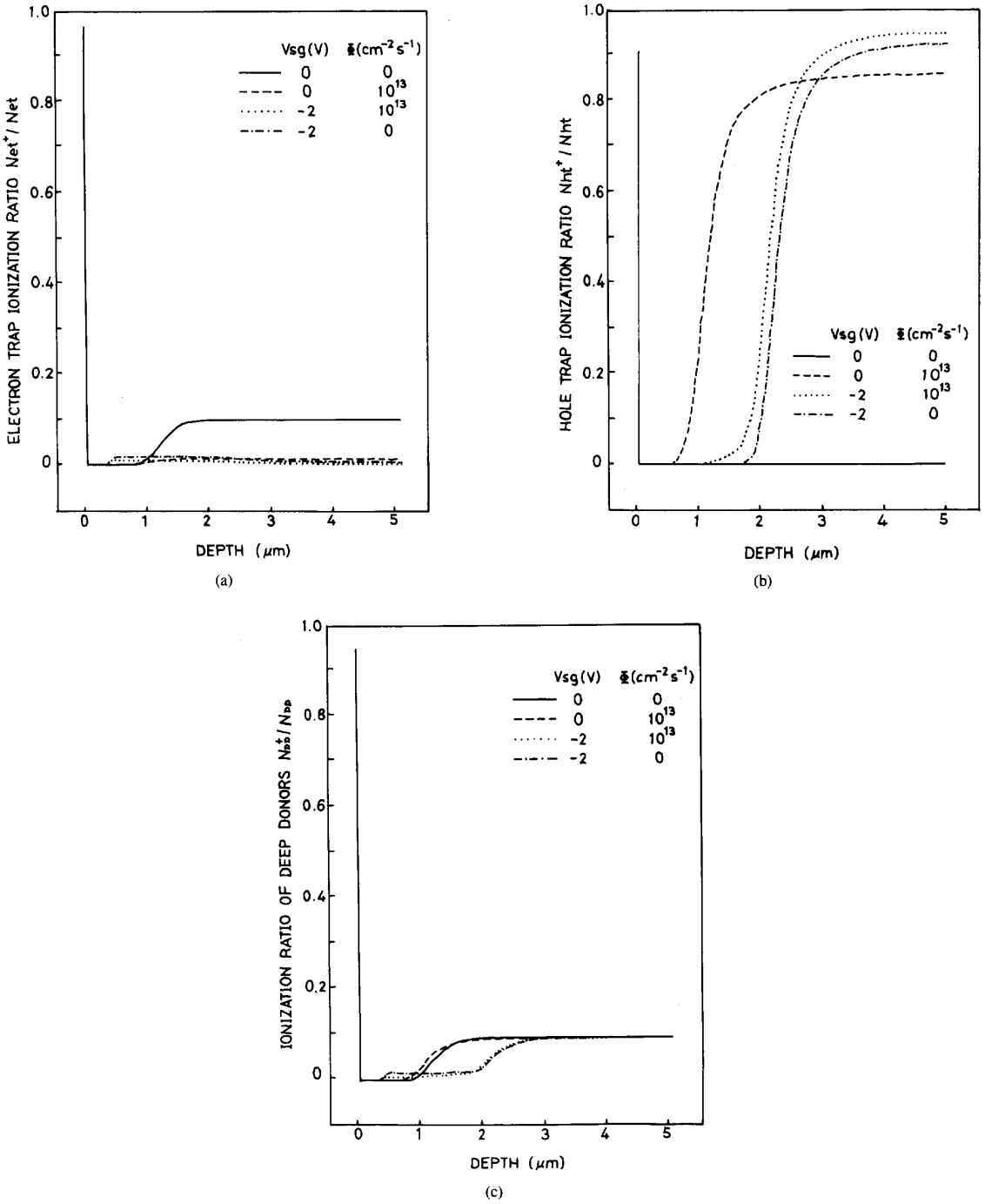

Fig. 4. Ionization ratio of (a) electron traps, (b) hole traps, and (c) all deep donors along the substrate under midgate.

On the other hand, when in the dark, no apparent sidegating threshold is observed and the decrease in drain current is gradual. In this case the sidegating effect is caused by the trap-fill-limited (TFL) conduction of the SI substrate, since the deep traps in the substrate between the sidegate and the FET are completely filled with electrons, as shown in Fig. 6. Because the sidegate current flows essentially through the region about 1–2 μm close to the surface, traps in this region will be filled first. Therefore, not only the estimation of the trap-filled-limit voltage,

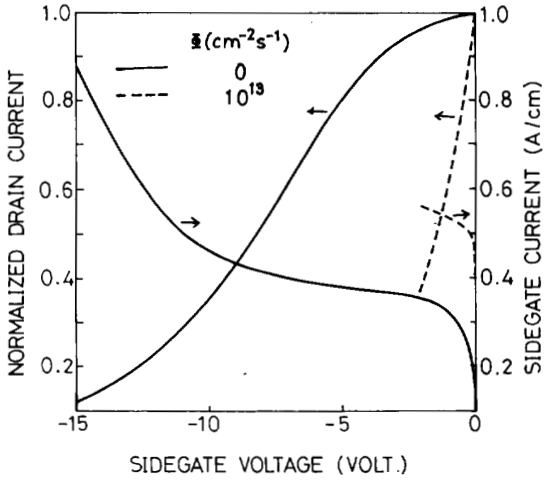

Fig. 5. Calculated drain current and sidegate current as functions of the sidegate voltage in the structure without a Schottky contact on the SI substrate.

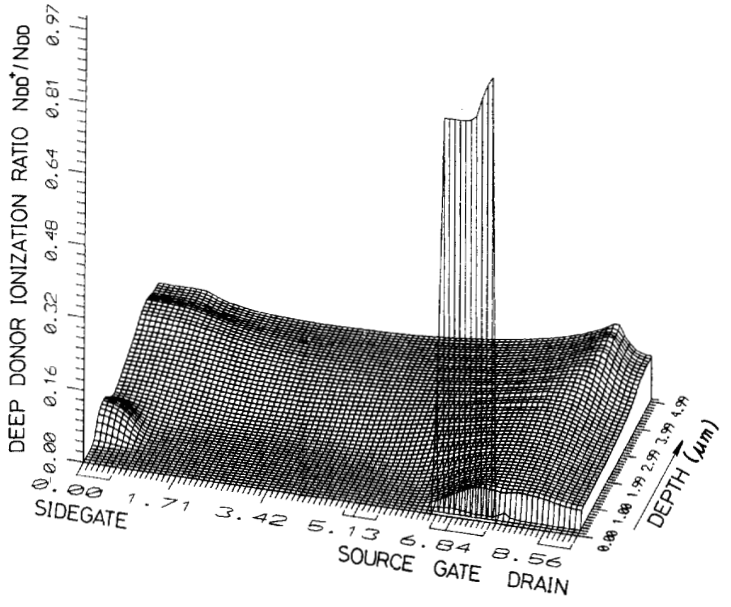

Fig. 6. Calculated ionization rato of all deep donors in the structure without the Schottky contact. The sidegate is biased at −20 V.

V_{TFL}, but also the current-voltage characteristics of the TFL model should take this 2-D nature of current flow into consideration.

Fig. 7(a) and (b) show the potential profile under illumination (at sidegate voltage, V_{sg}, equal to −2 V) and in the dark (at V_{sg} = −20 V), respectively. It can be seen that under illumination, the potential is nearly flat in the whole substrate region and the negative sidegate voltage drops across the channel/substrate interface. While in the dark, the potential is about linearly graded between FET and the sidegate, so that a larger negative sidegate voltage is required to cause the same amount of decrease in drain current.

IV. Conclusion

The light-induced sidegating effect, which occurs from zero sidegate voltage, has been found to be caused neither by the conduction of Schottky-i-n(sidegate) structure nor by the electron injection and trap-fill-limited conduction. Nevertheless, in contrast to the TFL model which involves electron injection, both the sidegating induced by light and that caused by Schottky-i-n conduction are due

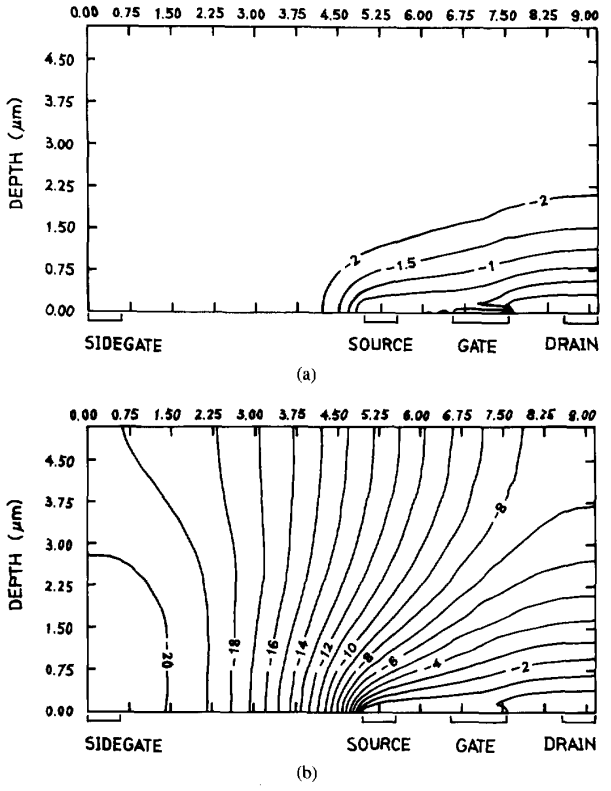

Fig. 7. The potential profile (a) under illumination at sidegate voltage, V_{sg}, equal to -2 V and (b) in the dark at $V_{sg} = -20$ V, for the structure without the Schottky contact.

to the injection of excess holes. It is the capturing of photo-generated holes by hole traps in the SI substrate that renders the electron trap rich SI substrate as susceptible to sidegating as hole trap rich substrates. Among the three possible mechanisms considered, if the substrate is free of hole traps, only the TFL conduction can cause sidegating. Therefore, it is possible that the serious sidegating effect in GaAs IC's can be greatly alleviated to a tolerable level even under illumination by minimizing the formation of hole traps in the substrate.

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