ESD Implantation for Subquarter-Micron CMOS Technology to Enhance ESD Robustness

Ming-Dou Ker, *Senior Member, IEEE*, Hsin-Chyh Hsu, *Student Member, IEEE*, and Jeng-Jie Peng, *Member, IEEE*

***Abstract*—A new electrostatic discharge (ESD) implantation method is proposed to significantly improve ESD robustness of CMOS integrated circuits in subquarter-micron CMOS processes, especially the machine-model (MM) ESD robustness. By using this method, the ESD current is discharged far away from the surface channel of nMOS, therefore the nMOS (both single nMOS and stacked nMOS) can sustain a much higher ESD level. The MM ESD robustness of the gate-grounded nMOS with a device dimension width/length (W/L) of 300 μm/0.5 μm has been successfully improved from the original 450 V to become 675 V in a 0.25-μm CMOS process. The MM ESD robustness of the stacked nMOS in the mixed-voltage I/O circuits with a device dimension W/L of 300 μm/0.5 μm for each nMOS has been successfully improved from the original 350 V to become 500 V in the same CMOS process. Moreover, this new ESD implantation method with the n-type impurity can be fully merged into the general subquarter-micron CMOS processes.**

***Index Terms*—Electrostatic discharge (ESD), ESD implantation, ESD protection, machine model.**

I. Introduction

COMPONENT-LEVEL ESD stresses on integrated circuit (IC) products had been classified as three models [1]: the human body model (HBM) [2]–[4], the machine model (MM) [5], [6], and the charged device model (CDM) [7], [8]. The ESD voltage ratio between HBM and MM ESD robustness of CMOS IC products was around $\sim$10 in the submicron ($1.0 \sim 0.5$ μm) CMOS processes [9], [10]. In the past, most of ESD design efforts were focused to improve HBM ESD robustness of IC products. With a high HBM ESD robustness, the IC products also had a high enough MM ESD level. Typically, a CMOS IC product, which has a HBM ESD robustness of 2 kV, can sustain a MM ESD stress of 200 V. However, the MM ESD robustness of IC products has been found to degrade much worse than its HBM ESD robustness in the subquarter-micron CMOS processes. This ratio has approached about 15–20 in the subquarter-micron CMOS processes. The CMOS IC fabricated by the subquarter-micron CMOS processes can still be designed to have a high HBM ESD robustness, but it becomes more challenging to have a high enough MM ESD level. When the IC products enter into the phase of mass production, the IC products are processed by a lot of automatic machines, such as the assembly and test machines, to have a throughput as fast as possible. So, the MM ESD robustness of such mass-production IC product is often more important then its HBM ESD robustness. How to effectively improve MM ESD robustness of IC products has become a challenge in the subquarter-micron CMOS processes. But, from the past literature, it is seldom to see the design or method for improving MM ESD robustness.

In order to enhance ESD robustness, some ESD implantations had been reported for including into process flow to modify the device structures for ESD protection [11]–[13]. The N-type ESD implantation was used to cover the lightly-doped drain (LDD) peak structure and to make a deeper junction in nMOS device for ESD protection [11]. The P-type ESD implantation with a higher doping concentration located under the drain junction of nMOS was used to reduce the junction breakdown voltage, and to earlier turn on the parasitic lateral n-p-n bipolar junction transistor (BJT) of the nMOS [12]. Moreover, both of the N-type and P-type ESD implantations were used in nMOS devices to create a higher ESD robustness [13]. The experimental results to compare the effectiveness among those ESD implantation methods had been investigated in a 0.18-μm CMOS process [14].

In the mixed-voltage circuit application, the stacked nMOS structure had been widely used in the mixed-voltage input/output (I/O) buffer [15] to solve the gate-oxide reliability issue without using the additional thick-gate-oxide process (also known as dual gate oxide in some CMOS processes) [16], or the power-rail ESD clamp circuit [17]. Unfortunately, in such mixed-voltage I/O circuits, the stacked nMOS often have a much lower ESD level, as compared to the buffer with single nMOS [18], [19].

In this paper, a new ESD implantation method to improve ESD robustness of both single and stacked nMOS is proposed and verified in a 0.25-μm CMOS processes. The MM ESD level has been an especially significant improvement [20]. The HBM/MM ESD level ratio in the single nMOS can be successfully kept at $\sim$10. On the other hand, the ratio between HBM and MM ESD levels in the stacked nMOS can be pulled down from 18.4 to 13.3 by this new ESD implantation method.

II. HBM and MM ESD Current Waveforms

In order to identify the underlying physical mechanisms of the HBM and MM, it is instructive to compare the ESD current discharging waveforms between HBM and MM ESD zapping. The real ESD current discharging waveforms of HBM and MM

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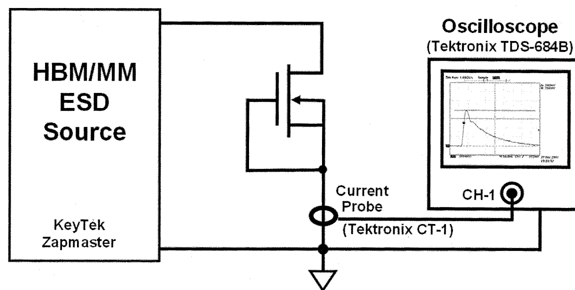
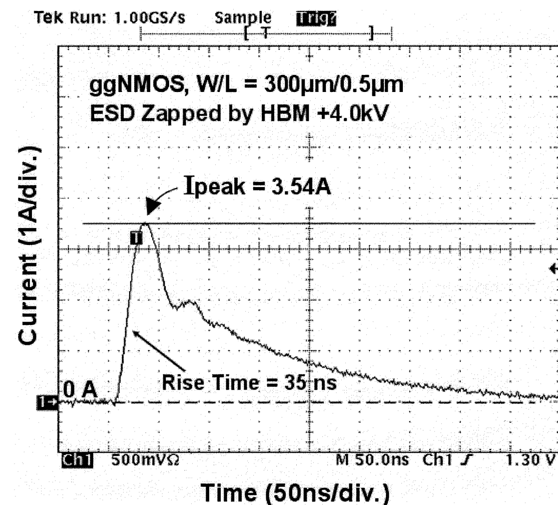


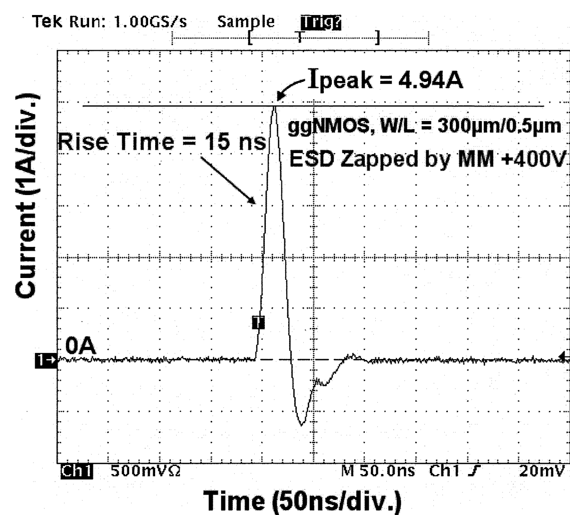
Fig. 1. Experimental setup to measure ESD transient current waveforms during ESD zapping.

ESD stresses through the gate-grounded nMOS (ggnMOS) are measured and compared to find the difference. The experimental setup to measure the current waveforms during ESD zapping is illustrated in Fig. 1, where the KeyTek Zapmaster is used to generate the HBM and MM ESD sources. The digital oscilloscope with a current probe of Tektronix CT-1 is used to measure the ESD transient currents in time domain.

The actual ESD current waveforms flowing through the ggnMOS with a device dimension width/length (W/L) of 300 μm/0.5 μm under 4-kV HBM and 400-V MM ESD stresses are measured and shown in Fig. 2(a) and (b), respectively. The current peak of 4-kV HBM ESD stress in Fig. 2(a) is 3.54 A, and the rise time is 35 ns. The current peak of 400-V MM ESD stress on the ggnMOS in Fig. 2(b) is as high as 4.94 A, and the rise time of the current is 15 ns. When comparing these two ESD current waveforms, the MM ESD stress has a much higher ESD current peak within a shorter current pulse width. This implies that the MM ESD event generates more heat in a shorter time period to burn out the device, and therefore to cause a much lower ESD robustness. So, ESD protection design against an MM ESD event has become more difficult than that against an HBM ESD event in subquarter-micron CMOS processes.



(a)



(b)

Fig. 2. Measured ESD current discharging waveform through the ggnMOS with the device dimension W/L of 300 μm/0.5 μm , which is zapped by (a) 4-kV HBM ESD voltage, and (b) 400-V MM ESD voltage.

III. ESD Implantation Methods

A. Device Structure

Since ESD robustness is strongly correlated with current distribution in the second breakdown region, observation of ESD current discharging paths of different device structures provides new insight to understand their different ESD performance. Generally, the ESD current flowing in a nMOS device has two discharging paths. One is the channel current of the MOSFET, and the other is the parasitic lateral n-p-n BJT current path through the bulk of MOSFET device. In subquarter-micron CMOS technology, the MOSFET fabricated with a high doped arsenic drain, the lightly doped drain (LDD) structure, and a salicided process to improve circuit performance. However, several problems may occur when these technologies are involved in ESD protection devices [21]. The high doped arsenic drain might reduce the breakdown voltage and snapback holding voltage of nMOS, which may improve ESD robustness. Unfortunately, the high doped arsenic drain increases the electric field in MOSFET to cause severe hot-carrier reliability issue. To solve this issue, the LDD structure is commonly implemented in nMOS device to overcome the impact of hot-carrier reliability, as the n-type lightly doped drain (NLDD) region shown in Fig. 3(a). Such an LDD structure, however, will encounter severe degradation on ESD robustness [21]. So, the hot-carrier reliability issue and ESD performance should be traded off, and the ESD protection device could be more difficultly designed in subquarter-micron CMOS processes. Moreover, the ESD protection device with salicided process is known to seriously degrade ESD robustness owing to insufficient ballast resistance [22], [23]. Several experimental results have been proven and then suggested to enlarge the clearance from drain contact to poly-gate edge (S_{DG}) for better ESD robustness [23], [24].

To improve ESD robustness, some CMOS processes provide one extra ESD-implantation mask to modify the nMOS devices of I/O circuits without the LDD peak structure [14]. One of the traditional ESD implantation methods, with n-type impurity for improving ESD robustness of nMOS, is shown in Fig. 3(b)

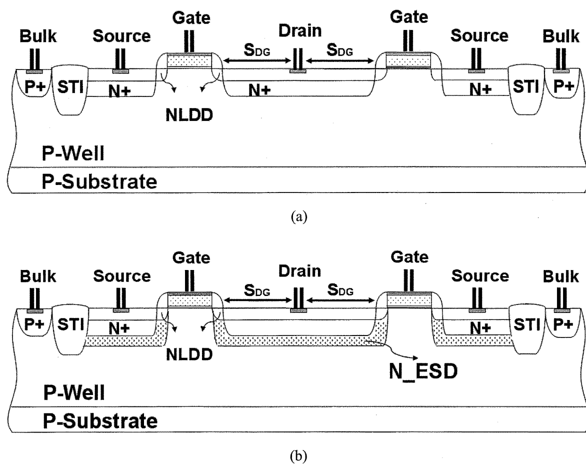


Fig. 3. nMOS devices with (a) lightly doped drain (LDD) structure to overcome the hot-carrier issue, and (b) traditional n-type ESD implantation to improve its ESD robustness.

with the extra N_ESD region. The n-type (N_ESD) impurity in subquarter-micron CMOS process often has a lower concentration than that of $N+$ drain/source source diffusion to overcome the hot-carrier reliability issue. However, the N_ESD impurity with a lower concentration increases the junction breakdown voltage and snapback holding voltage of nMOS, which reduces the turn-on efficiency of the parasitic lateral n-p-n BJT in the MOSFET. A comparison on the effectiveness of improving ESD robustness among the traditional ESD implantation methods had been experimentally investigated in [14].

To significantly improve ESD robustness of nMOS in I/O circuits, the new ESD implantation method is proposed in Fig. 4(a), where the blocking layout spacing "S" is the important layout parameter to be investigated. In Fig. 4(a), the ESD implantation region covers the whole drain region of nMOS device, except for the region around the drain contact. The corresponding layout top view of the nMOS with the new proposed ESD implantation method is drawn in Fig. 4(b), where the blocking layout spacing "S" is also indicated.

This new N_ESD implantation method is used on the stacked nMOS in the mixed-voltage I/O circuits. The cross-sectional view of the stacked nMOS with the proposed N_ESD implantation is shown in Fig. 5(a), where the spacing "S" is the important layout parameter to be investigated. In Fig. 5(a), the ESD implantation region covers the whole drain region of stacked nMOS device, but except the region around the drain contact. The corresponding layout top view of the stacked nMOS with the proposed ESD implantation method is drawn in Fig. 5(b), where the layout parameter "S," the clearance from drain contact to poly-gate edge (S_{DG}), and the spacing (C) between poly gate1 and poly gate2 of the stacked nMOS are also indicated.

This ESD implantation region has a doping concentration (N_ESD) lighter than that of the original $(N+)$ drain diffusion. The junction covered by the proposed ESD implantation method has a little increased junction breakdown voltage. But, the region not covered by this ESD implantation has the original junction breakdown voltage. When a positive ESD voltage is zapped to the pad in Figs. 4(a) and 5(a) with the VSS relatively grounded, the drain of the nMOS device is stressed by

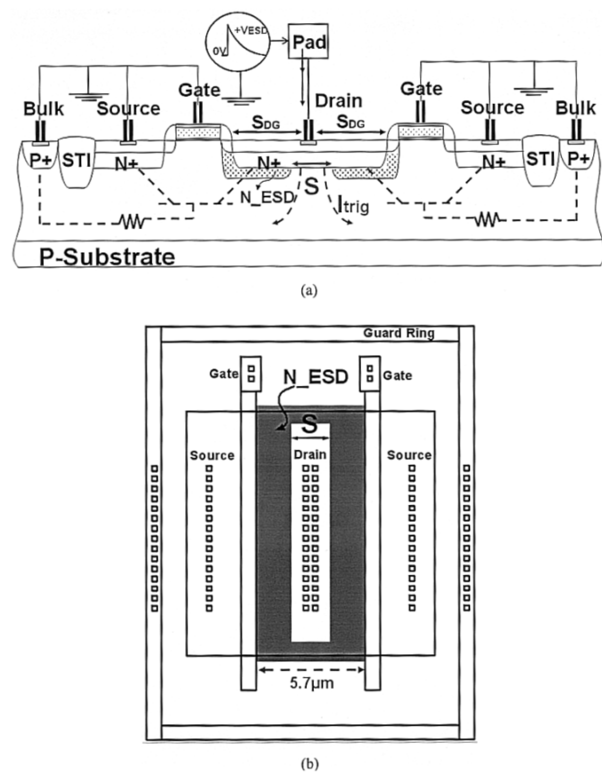


Fig. 4. (a) Cross-sectional view, and (b) layout top view, of the nMOS fabricated with the new proposed ESD implantation method to significantly improve its ESD robustness. The layout parameter "S" is also indicated in this figure.

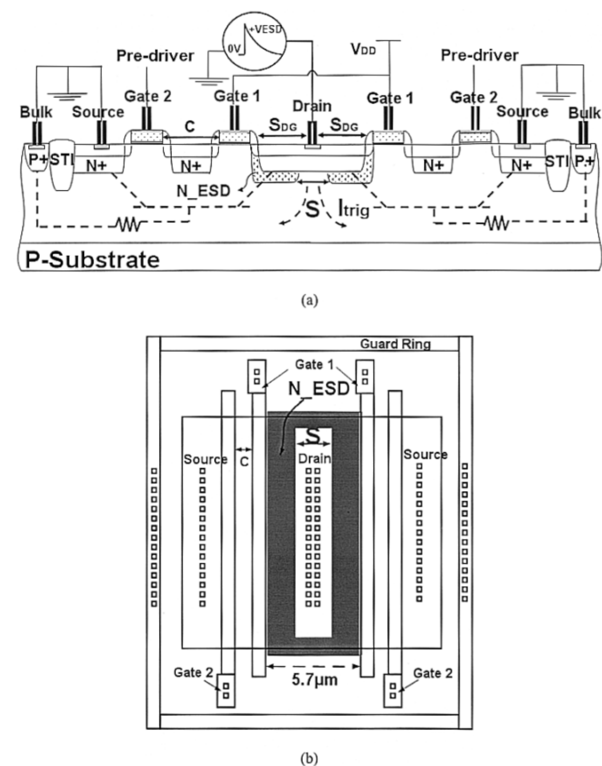


Fig. 5. (a) Cross-sectional view, and (b) layout top view, of the stacked nMOS fabricated with the new proposed ESD implantation method to significantly improve its ESD robustness. The layout parameter "S" is also indicated in this figure.

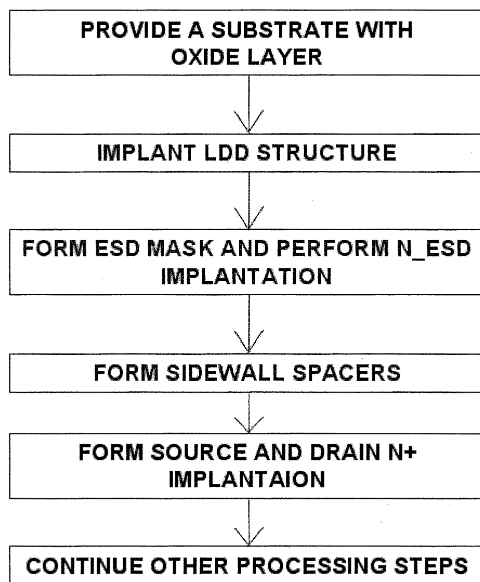


Fig. 6. Fabrication process flow to realize the proposed N_ESD implantation.

the ESD voltage, and therefore breaks down to clamp the overstress voltage on the pad. However, the region, which is not covered by the N_ESD implantation, has a lower junction breakdown voltage. So, the ESD current is first discharged through this region to generate the substrate current [*Itrig*, indicated in Figs. 4(a) and 5(a)] to quickly trigger on the parasitic lateral n-p-n BJT in the nMOS structure. With the self-generated substrate triggering current, the parasitic lateral n-p-n BJT in the nMOS structure can be fully turned on more quickly [25]. So, the fast transient current of ESD events, especially in the MM ESD zapping, can be quickly discharged through the parasitic lateral n-p-n BJT in the nMOS structure. Therefore, the ESD level of nMOS devices can be effectively improved.

B. Process Flow

The fabrication flow for forming the proposed ESD protection device with the new N_ESD implantation is shown in Fig. 6. The fabrication steps use the general fabrication methods for example, photolithography, ion-implantation, oxidation, and etching to implement the proposed ESD device. The detailed fabrication steps are described as follows:

1) Form gate electrodes of the ESD protection device, as that shown in Fig. 7(a)
2) Form LDD structure on the ESD protection device, as that shown in Fig. 7(b).
3) Use the ESD mask layer to define the ESD implantation region, and the light N-type dopant form the N_ESD region in the ESD protection device, as that shown in Fig. 7(c).
4) Form spacers by CVD interlayer dielectric (ILD) on the sidewall of the gate electrodes, as that shown in Fig. 7(d).
5) Apply the $N+$ diffusion mask to define the source and drain regions, and then form the source and drain $N+$ region in the ESD protection device, as that shown in Fig. 7(e).
6) Next, the subsequent conventional process steps are salicidation, metallization, and interconnection to complete the ESD protection device.

Two types of devices are investigated in this study: single nMOS and stacked nMOS, with a gate oxide thickness of ~ 54 Å (for 2.5 V voltage supply), a fixed gate oxide length of 0.5 μm, and a fixed clearance from contact to poly-gate edge ($\mathrm{S_{DG}}$) of 2.4 μm, have different blocking layout spacing "S" to be investigated. These layout parameters are indicated in the Figs. 4(a) and 5(a). The ESD implantation region in this ESD protection device has a lighter doping dosage of $1 \times 10^{15}\ \mathrm{ions/cm^2}$ and a junction depth of $\sim 0.2\ \mu$m. However, the drain/source $N+$ diffusion has a doping dosage of $5\ \times 10^{15}\ \mathrm{ions/cm^2}$ and a junction depth of $\sim 0.18\ \mu$m. The nMOS fabricated by this new process flow has the junction depth of ESD implantation slightly deeper than the junction depth of drain diffusion. This N_ESD implantation envelops the original LDD region of drain side, except the region around the drain contact in the ESD protection device.

IV. Experimental Results

To investigate the effectiveness of the new proposed ESD implantation method, test chips had been fabricated by a 0.25-μm CMOS technology with shallow trend isolation (STI) and salicided diffusion. Two types of devices, single nMOS and stacked nMOS, with different blocking layout spacing "S" in the ESD implantation region are investigated. This new proposed ESD implantation method (shown in Figs. 4(a) and 5(a)) on the test devices are directly realized by using the traditional ESD implantation mask with light n-type impurity, which had been an optional process step in general CMOS technologies provided by the most foundries. To simply investigate the dependence of the ESD-implanted region (adjusted by the spacing "S" in layout) on ESD robustness of both single and stacked nMOS structures, the layout spacing of the drain diffusion between the gates is fixed at 5.7 μm for all devices in the experimental test chips. The clearance ($\mathrm{S_{DG}}$) from drain contact to poly gate edge is 2.4 μm, and the spacing (C) between poly gate1 and poly gate2 of stacked nMOS is 0.4 μm. The devices fabricated with different spacing "S" are measured by the curve tracer to investigate DC I–V characteristics, by the transmission line pulsing (TLP) system [26]–[28] to investigate secondary breakdown current (It2), and by the ZapMaster ESD simulator to investigate HBM and MM ESD robustness. The experimental results are shown in Sections IV-A and B.

A. Experimental Results of ggnMOS With New N_ESD Implantation

1) DC Current–Voltage (I–V) Characteristics: The measured dc current–voltage (*I–V*) curves of the ggnMOS devices with different blocking layout spacing "S" in the ESD implantation region are compared in Fig. 8. The trigger (switching) voltages of the ggnMOS devices with $S = 0$ or 2.3 μm are 9.8 V, but that of the ggnMOS device with $S = 4.9\ \mu$m is 9.72 V. The holding points of the ggnMOS devices with the layout spacing "S" of 0, 2.3, and 4.9 μm have no obvious variation. The dc behaviors of those devices are almost the same, as those shown in Fig. 8. This implies that the new proposed ESD

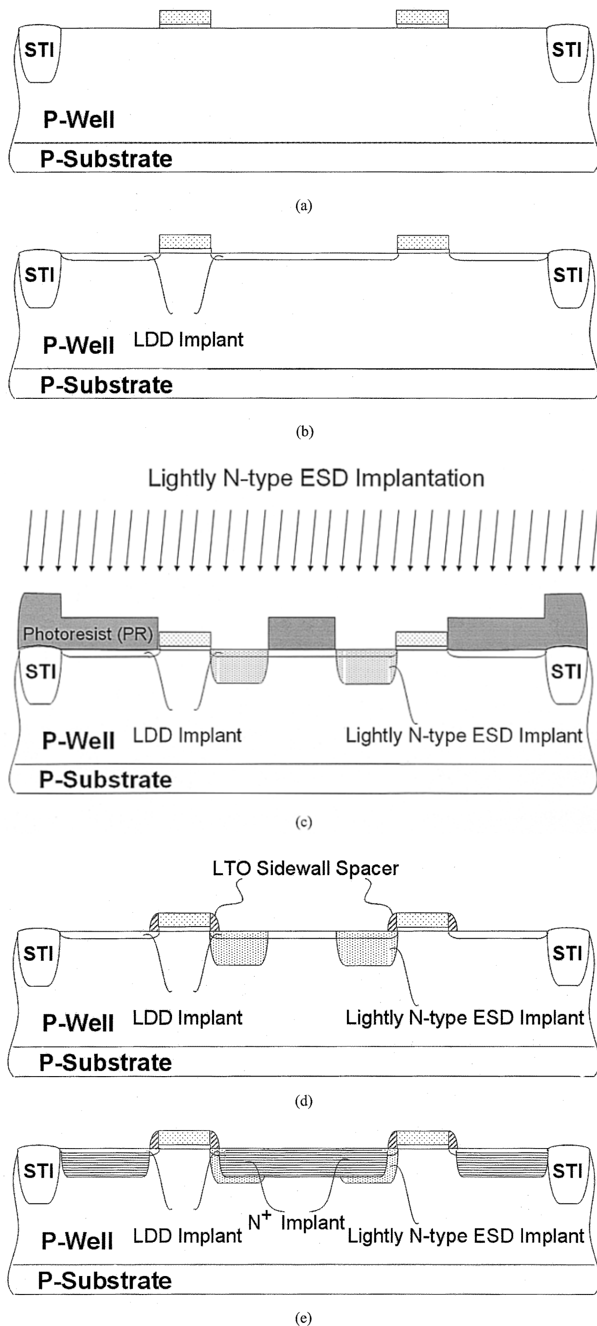


Fig. 7. Fabrication steps (a) form the gate electrode structure, (b) form the LDD structures, (c) use the light n-type ESD dopant to form the N_ESD region, (d) form spacers by chemical vapor deposition (CVD) interlayer dielectric (ILD) on the sidewall of the gate electrode, and (e) form source and drain $N+$ regions to realize the proposed ESD protection device.

implantation method does not modify the channel region of the nMOS devices. The trigger voltages of the nMOS devices with fixed channel length and unchanged channel region but different spacing S are the same, since the drain-to-source punch-through voltage dominates the dc characteristics of nMOS devices [29]. When such nMOS devices are used in the output buffer as the pull-down devices, their curves are similar to that of the normal nMOS device in the same CMOS process. This result provides the same device *I–V* behavior on the ESD-implanted nMOS, as that of normal nMOS, for working as the functional output devices in CMOS IC's.

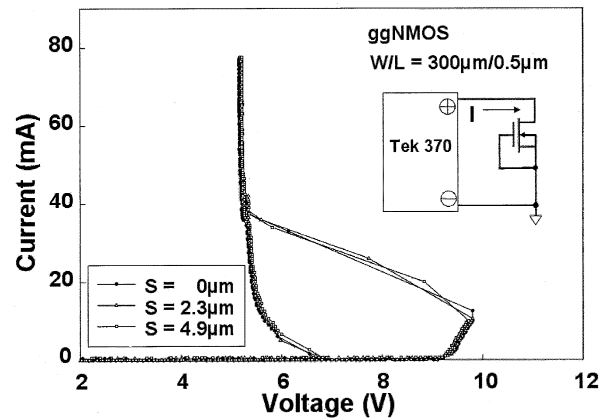
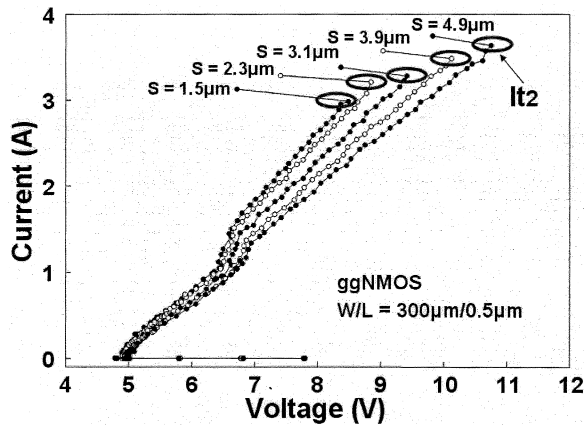


Fig. 8. Measured *I–V* curves of ggnMOS fabricated with the new proposed ESD implantation under different blocking layout spacing "S".

2) TLP I–V Characteristics: The TLP system has been widely used to measure the second breakdown characteristics of ESD protection devices to investigate the turn-on behavior of the device during ESD stress. The TLP system used in this measurement has been set up with a pulse width of 100 ns and a rise time of 10 ns to find the It2 of ESD protection devices [27]. When the ESD stress generated by the TLP system zapping on the ESD protection device is greater than its It2, the devices will be permanently damaged by the overstress current. The TLP-measured *I–V* curves of a ggnMOS with W/L = 300 μm/0.5 μm are shown in Fig. 9(a) under the different blocking layout spacing "S" in the ESD implantation region. The dependence of the It2 on the blocking layout spacing "S" of the ggnMOS fabricated with the new proposed ESD implantation method is shown in Fig. 9(b). The It2 of the ggnMOS with $S = 0$ μm is only 2.9 A, when it has a device dimension W/L of 300 μm/0.5 μm. But, its It2 can be significantly improved up to 3.64 A, when the spacing S is increased to 4.9 μm. Under the same layout area of the ggnMOS with W/L = 300 μm/0.5 μm (the drain diffusion between two poly gates is fixed at 5.7 μm), the It2 can be improved 25.5% by using the new proposed ESD implantation method. This implies that the blocking layout spacing "S" in the ESD implantation region is an important design parameter determining ESD robustness for the ggnMOS.

3) ESD Test Results: The ZapMaster ESD tester is used to investigate the HBM and MM ESD level of the fabricated test chips. The failure criterion is generally defined as the minimum ESD stress to cause the leakage current of the tested device greater than 1 μA under the voltage bias of 1.1 $\times$ VDD. To compare with the traditional design, the ggnMOS drawn with layout spacing S of 0 μm, where the ESD implantation is cover the whole drain diffusion, is also tested as a reference. The dependences of the HBM and MM ESD robustness on the layout spacing "S" of ESD-implanted ggnMOS, under a fixed device dimension W/L of 300 μm/0.5 μm, are shown in Fig. 10(a). With the same layout area and device dimension in the ESD-implanted ggnMOS, the wider spacing "S" can lead to higher HBM and MM ESD levels. The HBM ESD level of this ESD-implanted ggnMOS with a fixed device dimension W/L of 300 μm/0.5 μm is improved from the original 5.75 kV



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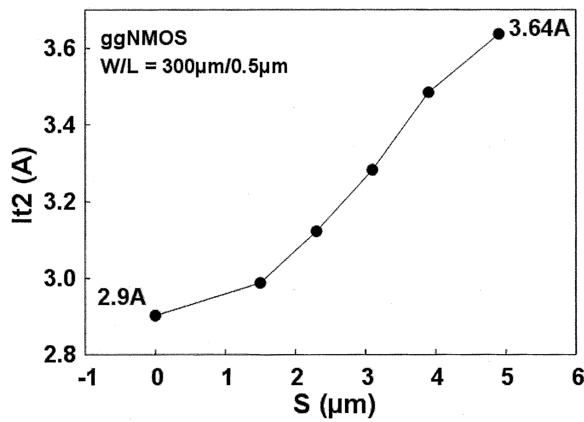
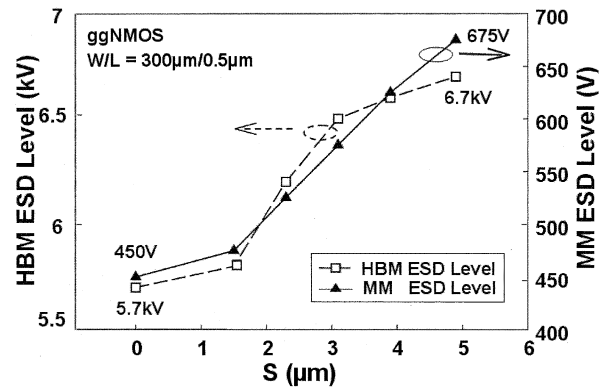


(b)

Fig. 9. (a) TLP-measured *I–V* curves, and (b) the second breakdown current (It2), under different blocking layout spacing "S" in the ESD implantation region of the ggnMOS.



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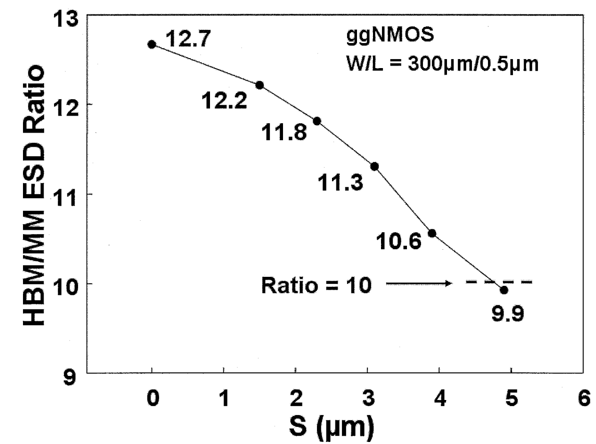


(b)

Fig. 10. Dependence of (a) HBM and MM ESD robustness, and (b) HBM/MM ratio, on different blocking layout spacing "S" in the ESD implantation region of the ggnMOS.

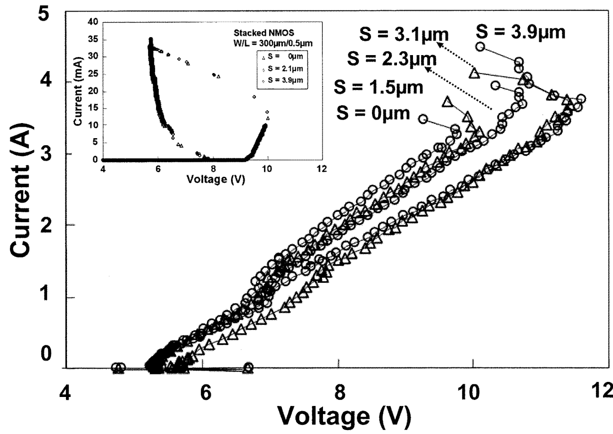
(with $S = 0$) to become 6.75 kV (with $S = 4.9\ \mu$m). The MM ESD level of this ESD-implanted ggnMOS, with W/L= 300 μm/0.5 μm, is also improved from the original 450 V (with $S = 0$) to become 675 V (with $S = 4.9\ \mu$m). This tendency is well consistent with that verified by the TLP-measured It2 in Fig. 9(b).

The ratio between the HBM and MM ESD levels on the layout spacing "S" of the ESD-implanted ggnMOS with W/L = 300 μm/0.5 μm are further compared in Fig. 10(b). Surprisingly, the HBM/MM ESD level ratio of the ESD-implanted ggnMOS with W/L = 300 μm/0.5 μm has a value of 12.7 when the spacing $S = 0\ \mu$m. As seen in Fig. 10(b), this HBM/MM ESD level ratio can be decreased to 9.9, when the spacing "S" is enlarged to 4.9 μm in the ESD-implanted ggnMOS. From the experimental results, the new proposed ESD implantation method can significantly increase ESD level of the nMOS devices in subquarter-micron CMOS processes, especially MM ESD robustness. Moreover, the HBM/MM ESD level ratio can be successfully kept at $\sim$10 by this new ESD implantation method.

B. Experimental Results of Stacked nMOS With New N_ESD Implantation

1) DC I–V and TLP I–V Characteristics: The TLP-measured *I–V* curves of stacked nMOS with W/L = 300 μm/0.5 μm, fabricated in a 0.25-μm CMOS process with the new proposed ESD implantation method, are shown in Fig. 11(a) under the different layout spacing "S." The measured dc *I–V* curves of the stacked nMOS with different layout spacing "S" are also inserted in Fig. 11(a). The dc behaviors of those test devices are almost the same, which imply that the new proposed ESD implantation method does not modify the channel region of nMOS devices [29]. The dependence of the It2 on the layout spacing "S" of the stacked nMOS, fabricated with the new proposed ESD implantation method, is shown in Fig. 11(b). The It2 of the stacked nMOS with $S = 0\ \mu$m is only 3.25 A, when it has a device dimension W/L of 300 μm/0.5 μm. But, its It2 can be significantly improved up to 4.03 A, when the spacing S is increased to 3.9 μm. Under the same layout area of the stacked nMOS with W/L= 300 μm/0.5 μm, the It2 can be improved 24% by using the new proposed ESD implantation method.

2) ESD Test Results: The ESD-implanted stacked nMOS devices are also verified by the ZapMaster ESD simulator under both HBM and MM ESD stresses. The ESD failure criterion of the stacked nMOS under ESD stresses is the same as measuring the single ggnMOS. The dependences of HBM and MM ESD levels on the channel width of stacked nMOS with $S = 0$ or 1.5 μm are shown in Fig. 12. The HBM and



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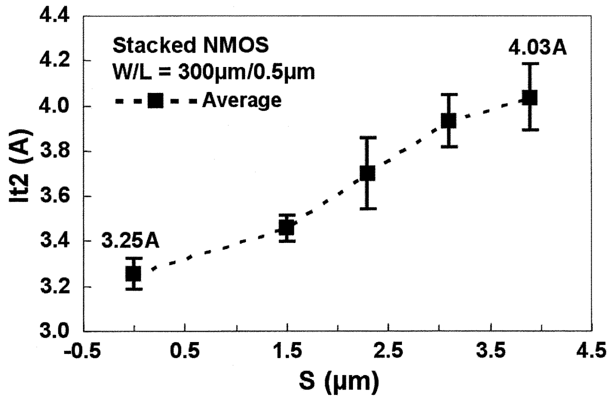


(b)

Fig. 11. (a) TLP-measured *I–V* curves with the inset of dc *I–V* curves, and (b) the second breakdown current (It2), under different blocking layout spacing "S" in the ESD implantation region of stacked nMOS.

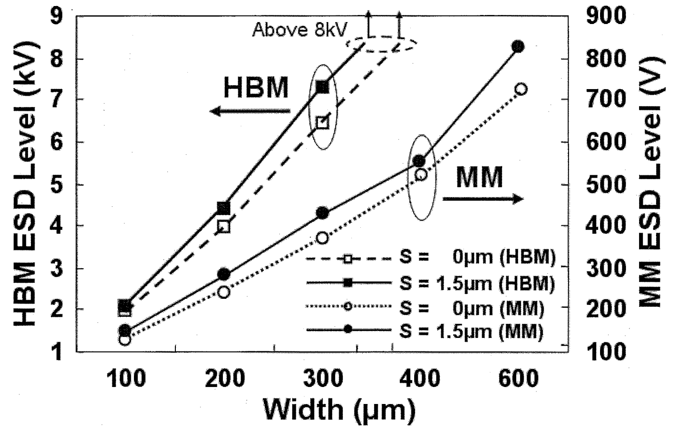
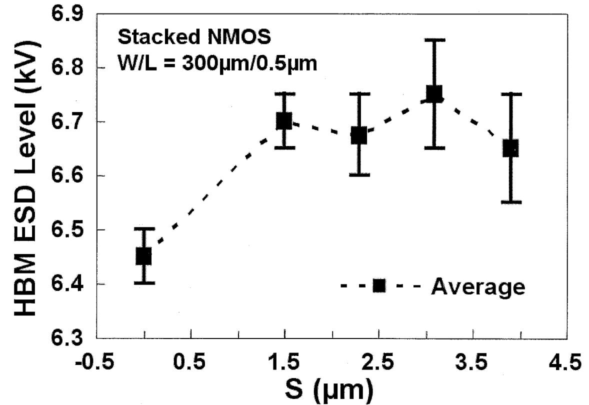
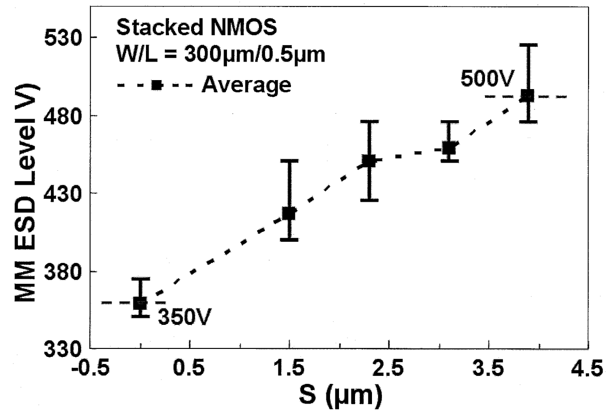


Fig. 12. Dependence of HBM and MM ESD robustness on the channel width of ESD-implanted stacked nMOS with $S = 0$ or 1.5 μm.



(a)



(b)

Fig. 13. Dependence of (a) HBM, and (b) MM, ESD robustness on the blocking layout spacing "S" in the ESD implantation region of the stacked nMOS.

MM ESD levels are linearly increased, when the channel width of the stacked nMOS is increased. This implies that the ESD implantation method leads to uniformly turn on, and the ESD level is improving when the total channel width increasing. However, as comparing the lines between the HBM and MM ESD levels under different layout spacing S, the MM ESD level has an obvious improvement if the stacked nMOS is drawn with a wider S.

The dependences of the HBM and MM ESD robustness on the layout spacing "S" of ESD-implanted stacked nMOS, under a fixed device dimension of W/L = 300 μm/0.5 μm, are shown in Fig. 13(a) and (b), respectively. With the same layout area and device dimension in the ESD-implanted stacked nMOS, the wider spacing "S" can lead to higher HBM and MM ESD levels. The average HBM ESD level of this ESD-implanted stacked nMOS with a fixed device dimension of W/L = 300 μm/0.5 μm is slightly improved from the original 6.45 kV (with $S = 0$ μm) to become 6.65 kV (with $S = 3.9$ μm), as shown in Fig. 13(a). However, the averaged MM ESD level of this ESD-implanted stacked nMOS, with W/L = 300 μm/0.5 μm, is significantly improved from the original 350 V (with $S = 0$ μm) to become 500 V (with $S = 3.9$ μm), as that shown in Fig. 13(b). The MM ESD level can be greatly improved 43% by using the new proposed N_ESD implantation method.

The ratio between the HBM and MM ESD levels on the layout spacing "S" of the ESD-implanted stacked nMOS with W/L = 300 μm/0.5 μm are further compared in Fig. 14. The HBM/MM ESD level ratio of the ESD-implanted stacked nMOS has a value of 18.4 when the spacing $S = 0$ μm. As seen in Fig. 14, this HBM/MM ESD level ratio can be decreased to 13.3, when the spacing "S" is enlarged to 3.9 μm

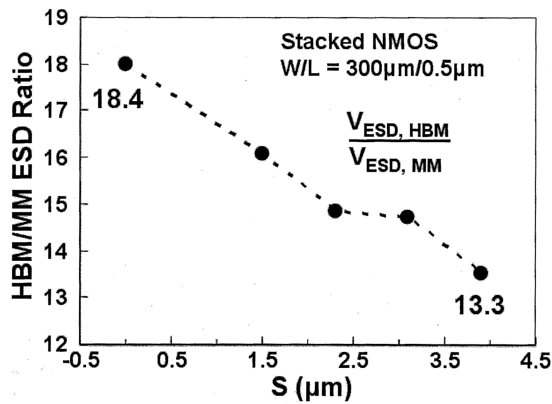


Fig. 14. Dependence of the HBM/MM ratio on the blocking layout spacing "S" in the ESD implantation region of stacked nMOS.

in the ESD-implanted stacked nMOS. From the experimental results, the new proposed N_ESD implantation method can significantly increase the MM ESD level of the stacked nMOS devices in subquarter-micron CMOS processes. The HBM/MM ESD level ratio can be successfully decreased 28% by using the new proposed N_ESD implantation method. This tendency is also consistent with that of ggnMOS. However, the HBM ESD levels of the stacked nMOS drawn with a wider "S" have a little improvement. Future work on this point, including device simulation and failure analysis, will be performed to optimize the new proposed ESD implantation method for application on the IC products.

V. Conclusion

On-chip ESD protection design with a new N_ESD implantation method to significantly improve ESD robustness of both ggnMOS and stacked-nMOS devices, especially MM ESD robustness, has been practically verified in a 0.25-μm CMOS process. Moreover, the HBM/MM ESD level ratio of both single and stacked nMOS is also decreased. The proposed ESD implantation method, which is process compatible to general CMOS processes with an additional noncritical mask layer of light-doping ESD implantation, is very suitable for using in IC products to improve MM ESD robustness without adding any extra silicon area.

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