Device Transfer Technology by Backside Etching (DTBE) for Poly-Si Thin-Film Transistors on Glass/Plastic Substrate

2003 Jpn. J. Appl. Phys. 42 L1044

(http://iopscience.iop.org/1347-4065/42/9A/L1044)

Jpn. J. Appl. Phys. Vol. 42 (2003) pp. L 1044–L 1046
Part 2, No. 9A/B, 15 September 2003

Device Transfer Technology by Backside Etching (DTBE) for Poly-Si Thin-Film Transistors on Glass/Plastic Substrate

Shuo-Cheng WANG*, Ching-Fa YEH, Chien-Kai HUANG and Yuan-Tung DAI[1]

Department of Electronics Engineering & Institute of Electronics, National Chiao-Tung University, 1001 Ta-Hsueh Road, Hsinchu, Taiwan, R.O.C.
[1]*Electronics Research & Service Organization of Industrial Technology Research Institute, Bldg. 15, Chung Hsing Rd., Chutung, Hsinchu, Taiwan, R.O.C.*

(Received January 14, 2003; accepted for publication July 8, 2003)

This work presents a novel method entitled "device transfer by backside etching (DTBE)" for transferring thin-film devices from Si wafers to a glass or plastic substrate. First, high performance poly-Si thin-film transistors (TFTs) were fabricated on a Si wafer and then adhered to glass or plastic substrates. The remaining Si was removed delicately using wafer backside chemical-mechanical polishing (CMP) and wet chemical etching. The devices after transferring exhibit comparable electrical characteristics to the original ones on Si substrates. The new transfer scheme has quite attractive applications for fabricating high-quality displays on low-cost substrates with low melting temperatures. [DOI: 10.1143/JJAP.42.L1044]

KEYWORDS: thin-film transistor, poly-Si, glass substrate, plastic substrate, CMP, wet etching

The feasibility of developing poly-Si thin-film transistors (poly-Si TFTs) that use glass, steel or plastic based backplanes has received increasing interests.[1–4] For example, liquid-crystal light valves in small projectors or TFT-driving circuits for liquid crystal display (LCD) panels can be integrated on glass substrates to reduce manufacturing costs. Also, plastic displays are promising solutions for mobile appliances, offering advantages of lightness, thinness and robustness. However, the conventional TFT process including thin-film deposition, crystallization, oxidation or activation can not be accomplished with a furnace or even a plasma enhanced chemical vapor deposition (PECVD) system because the melting temperature of glass is less than 600°C, and the deformation temperature of plastic substrate is generally below 200°C. Besides, the device performance of low-temperature processed (LTP) poly-Si TFTs also seriously deteriorates.

Recently, excimer laser annealing (ELA) method has been proven to be a potential solution for LTP poly-Si devices on the low-melting-temperature substrates.[4–6] Although poly-Si TFTs formed by ELA exhibit large driving current with high field effect mobility, the uniformity of device characteristics, the throughput and the cost remain major issues in mass production. Alternatively, T. Shimoda *et al.* ever realized a new surface free technology (SUFTLA)[7] that enables devices to be fabricated primarily on quartz, and then transferred to another plastic substrate by laser ablation.[8] Besides, A. Asano *et al.* demonstrated a similar experiment for fabricating TFTs on glass and then removing unwanted substrates by HF acid to accomplish the transfer sequences.[9] These methods open up the possibility of alleviating the temperature-limitations on processing materials, making feasible the transference of high-performance driving and display circuits to any substrate. Nevertheless, some critical issues must be addressed before such a goal of system on glass technology can be reached.

In this letter, we proposed a novel device transfer technology by backside etching (DTBE) to transfer poly-Si TFTs from Si wafers to glass or plastic substrates. This process requires no ELA facility but uses the matured chemical mechanical polishing and wet-etching equipment. Furthermore, the process temperature of poly-Si TFTs can be elevated above 1000°C since the starting material is Si wafer rather than glass or polymeric substrates. Compared with a reflective-type liquid-crystal on Si (LCOS) module, a transmissive panel with similar resolution and higher light efficiency can be fulfilled by DTBE.

The DTBE method consists of two major steps: The first is to fabricate TFT devices on a Si wafer, and the second is to transfer TFT devices to the glass/plastic substrate.

Figure 1(a) schematically depicts the n-channel poly-Si TFT structure. The detailed process sequences can be found elsewhere.[10] In brief, a 500-nm SiO_2 was thermally grown on the Si substrate to serve as an etching stop layer in the transfer process. An α-Si layer was then deposited with LPCVD method. The gate insulator was formed by liquid-phase deposition (LPD) method at 25°C. After poly-Si deposition (at 620°C by LPCVD), gate electrode patterning and self-aligned ion implantation steps, a TEOS SiO_2 passivation layer was deposited. A 5-nm thick Ni layer was subsequently deposited in the contact windows to perform metal-induced lateral crystallization. Next, furnace annealing at 550°C in N_2 ambient for 48 h recrystallized the high-quality channel region and simultaneously activated the doped area. Finally, all samples underwent a standard back-end process to form contact pads. After the poly-Si TFTs were fabricated on Si wafers, electrical characteristics such as I_{DS}-V_{GS} curves and transconductance were measured.

Following the measurement, a layer of PECVD TEOS oxide was deposited on the wafer surface. To overcome the restriction of our chemical-mechanical polishing (CMP) facility, the wafers were cut into pieces of 4 cm × 2 cm. Thereafter, as shown in Fig. 1(b), the sample was glued with front-side down to the glass/plastic substrate using high-transparency optical adhesive. Next, CMP was utilized to polish the wafer backside to a thickness of 20–40 μm. The optimized wet-etching solution, composed of HF and HNO_3, was used to etch the remaining Si at 1.2 μm/min with a very high Si/SiO_2 selectivity up to 80. Finally, lithography was used to open the contact pads and the TFT's electrical properties were measured again after the device was transferred. Figure 1(c) illustrates the finished structure.

Figure 2(a) illustrates the DTBE poly-Si TFTs on the rigid plastic substrate (metallocene cyclic olefin copolymer, 1000-μm thick). The area of the device is 4 cm × 2 cm. The contours of the chip were protected by wax; otherwise, the Si

*E-mail address: scwang.ee88g@nctu.edu.tw

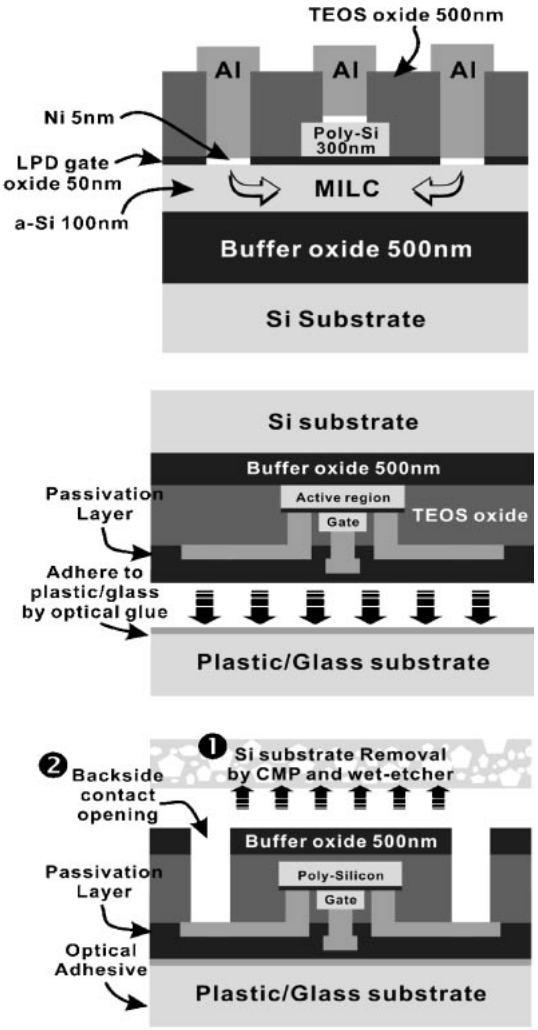

Fig. 1. (a) Schematic diagram of poly-Si TFTs before DTBE, (b) TFTs were passivated by TEOS oxide and then glued to glass/plastic substrate with high-transparency optical adhesive, (c) Si substrate was removed by CMP and wet-etcher followed by contact opening to accomplish DTBE process.

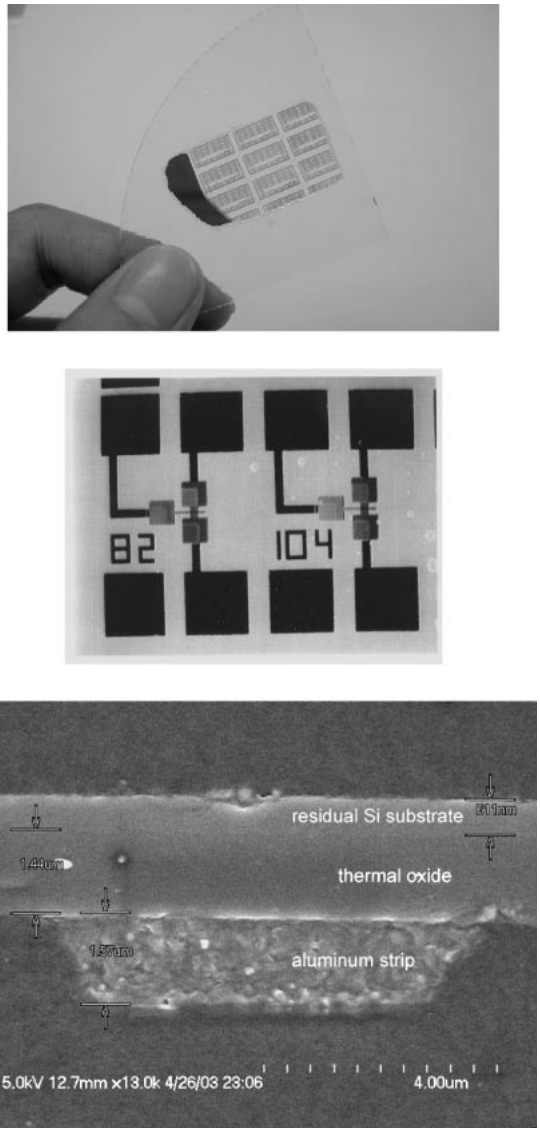

Fig. 2. (a) The appearance of the DTBE poly-Si TFTs after being transferred from a Si wafer to the plastic substrate, (b) The optical microscope picture of TFTs on a plastic substrate, (c) The SEM cross-sectional view of an aluminum strip after DTBE.

etcher would have damaged the exposed part of optical adhesive and caused film peeling. Figure 2(b) shows the optical microscope (OM) photograph of TFTs on a plastic substrate, observed with a back light source. The gray parts are TFTs (semi-transparent) while the dark areas are Al pads, which are opaque to light. The photograph reveals that the remaining Si was completely removed; no physical damage was observed. Besides, Fig. 2(c) shows a scanning electoron microscopy (SEM) cross-section view of an aluminum strip having been transferred to a plastic substrate. In order to clearly observe the surface geometry after transference, thick Al strips with buffer oxide of 1.4 μm was deposited, and some backside Si was deliberately kept at the chemical etching step. Each material indicated in the picture has been confirmed by energy-dispersive spectrometer (EDS). It can be found that the residual Si substrate, polished by CMP and wet-chemical etching, exhibits low surface roughness and uniform thickness; the Al strip is well protected by thermal oxide layer. In the fabrication process of TFTs, the total thickness variation of a Si wafer was 25 μm, and thickness of the SiO_2 etching stop layer was 500 nm. Both CMP and backside chemical etching affect the uniformity of thinning process. However, typical CMP equipment provided quite high planarity because no difficulties concerning dishing, erosion, or pattern dependence. Since the rate of wet chemical etching of Si is 80 times faster than that of SiO_2, the maximum tolerable thickness variance was 40 μm (80 × 500 nm), much larger than that attributed to the thickness variation of substrate itself and the subsequent removal processes of backside Si. The satisfactory transparency of plastic in Figs. 2(a) and 2(b) shows that the practical result is very consistent with the above estimation. Therefore, combining CMP/wet-etching process of modern complementary metal oxide semiconductor (CMOS) technology, DTBE shows a great promise of transferring devices to a substrate as large as 12 inch.

Figure 3 compares the I_{DS}-V_{GS} and transconductance curves of poly-Si TFTs before and after DTBE process. Clearly, no device degradation was observed after adhesion, CMP and wet etching process. On the contrary, the device characteristics, such as ON/OFF current ratio, swing, threshold voltage and mobility were a little better than those

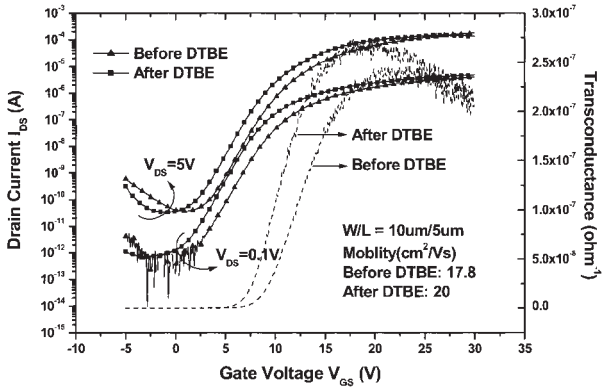

Fig. 3. I_{DS}-V_{GS} and transconductance curves before and after DTBE process.

before DTBE. For these devices, conventional hydrogen passivation process was never performed but a final SiO_2 layer was capped above the Al interconnection when finishing electrical measurements before transferring. This oxide layer was deposited in a 13.56 MHz parallel plate reactor at 300°C in a 300 mtorr gas mixture of 7 sccm TEOS and 450 sccm O_2. Because metal-induced crystallization process would contribute to large number of intra-granular defects and defective crystallization front, the O_2 radicals in the plasma could partially passivate the trap states in the channel region of poly-Si TFTs, resulting in the fluctuation of device characteristics after DTBE.[10]

The difference of ON current between device transferring steps has been statistically evaluated by the following equation

$$\text{Difference}(\%) = \frac{I_{\text{ON-after}} - I_{\text{ON-before}}}{I_{\text{ON-before}}} \times 100\% \qquad (1)$$

Both the mobility and OFF-state leakage current have been treated in the same manner. Figure 4 summarizes the results for devices with various channel length/width. It is found that both mobility and ON current after DTBE increased while the OFF-state leakage current decreased. Notably, however, for large devices (W/L = 20 μm/9 μm), not only the OFF current but also the transconductance apparently degrades after DTBE. It can be attributed to the stress-induced damage because the thermal expansion coefficient of optical adhesive is 6.2×10^{-5} /°C, which is 25 times larger than that of Si (2.4×10^{-6} /°C). While suffering annealing or cooling steps during bonding and photo-resist baking, larger devices tends to generate more micro-defects than the smaller ones, resulting in noticeable degradation of electrical properties. To suppress the induced extrinsic stress, a thick oxide or even nitride layer could be deposited on the wafer surface before bonding, and the curing temperature of optical adhesive would be modified. Further investigation is still in progress to clarify the relationship between the extrinsic stress and the device performance.

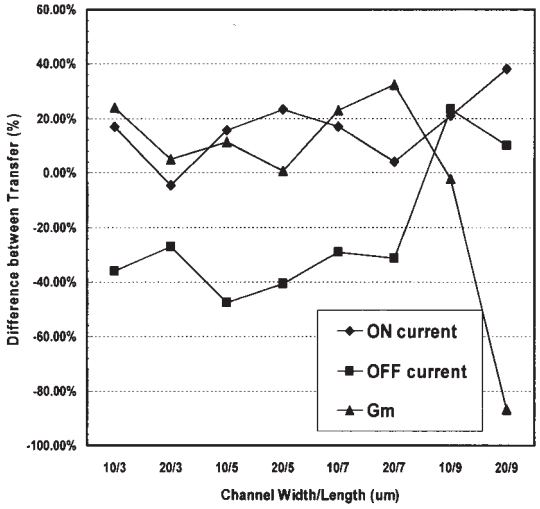

Fig. 4. Statistical differences in properties of devices including ON current, OFF current and Gm with various channel length/width due to transfer processes.

In this research, the process temperature of poly-Si TFTs did not exceed 620°C, so that the average field-effect mobility (μ_{FE}) was only 20 $cm^2/V{\cdot}s$. Nevertheless, several high temperature processes, including high-quality gate oxidation and MILC with 950°C post annealing, can be introduced to optimize the device performances.[11] Undoubtedly, DTBE technology can provide the feasibility of high temperature processes required to integrate devices on glass/plastic substrates.

In summary, we have successfully demonstrated a DTBE method for transferring poly-Si TFTs from Si wafer to glass/plastic substrate. Thanks to the lithographic technique of CMOS process, not only active matrix devices but also high-density peripheral circuits can thus be integrated with low-cost and low-melting temperature materials, contributing to wide applications in multi-functional portable displays, LCD projector or rear-projection TVs. Additionally, the DTBE process is familiar to the semiconductor foundry industry. Mass production with a high yield can be expected.

1) C. E. Forbes, A. Gelbman and C. Turner: SID Dig. (2002) p. 1200.
2) T. Serikawa and F. Omata: IEEE Trans. Electron Devices **49** (2002) 820.
3) D. P. Gosain, T. Noguchi and S. Usui: Jpn. J. Appl. Phys. **39** (2000) L179.
4) S. D. Theiss, P. G. Carey, P. M. Smith, P. Wickboldt, T. W. Sigmon, Y. J. Tung and T. J. King: IEDM'98 Tech. Dig. (1998) p. 257.
5) D. H. Choi, E. Sadayuki, O. Sugiura and M. Matsumura: Jpn. J. Appl. Phys. **33** (1994) 70.
6) R. T. Fulks, J. Ho and J. B. Boyce: IEEE Electron Device Lett. **22** (2001) 86.
7) SUFTLA is a trademark.
8) T. Shimoda and S. Inoue: IEDM'99 Tech. Dig. (1999) p. 289.
9) A. Asano and T. Kinoshita: SID Dig. (2002) p. 1196.
10) C. F. Yeh, S. S. Lin, T. Z. Yang, C. L. Chen and Y. C. Yang: IEEE Trans. Electron Devices **41** (1994) 173.
11) M. Wong, Z. Jin, G. A. Bhat, P. C. Wong and H. S. Kwok: IEEE Trans. Electron Devices **47** (2000) 1061.
12) H. Wang, M. Chan, S. Jagar, V. M. C. Poon, M. Qin, Y. Wang and P. K. Ko: IEEE Trans. Electron Devices **47** (2000) 1580.