A Pseudomorphic GaInP/InP MESFET with Improved Device Performance

K. C. Lin, Y. M. Hsin, C. Y. Chang, and E. Y. Chang

***Abstract*—A high band-gap GaInP epitaxial material was grown on InP to increase the Schottky barrier height of the InP MESFET. The Schottky gate materials used in this study were Au and Pt_2Si. The pseudomorphic GaInP/InP MESFET with Au gate has a Schottky barrier height of 0.54 eV and the reverse leakage current of the device is 10^{-2} times lower than the conventional InP MESFET. The extrinsic and intrinsic transconductance of the pseudomorphic MESFET were 66.7 and 104.2 mS/mm respectively for the 5 µm gate length GaInP/InP MESFET.**

I. INTRODUCTION

Indium phosphide exhibits excellent transport properties that make it suitable for high-speed electronic applications. However, the lack of high Schottky barrier height material makes it hard to form a good field-effect transistor. In this work, we used a high band-gap GaInP epilayer grown by low-pressure Metal-Organic Chemical Vapor Deposition (LP-MOCVD) on InP to increase the Schottky barrier height of the InP MESFET. The choice of GaInP as the high band-gap epilayer on InP to increase the InP Schottky barrier is because it does not cause the Fermi level pinning and is not easily oxidized during the process [1]-[4].

In this work, the dc performance of the novel pseudomorphic GaInP/InP MESFET with 5 μm gate length showed excellent device characteristics. The Schottky barrier height is increased by about 0.1 eV due to the incorporation of the thin GaInP layer on the InP MESFET, the reverse leakage current is 10^{-2} times lower than the conventional InP MESFET, and the intrinsic transconductance of the 5 μm gate GaInP/InP is as high as 104.2 ms/mm.

II. EXPERIMENTAL

There are four major steps in the MESFET process: epitaxy growth, isolation, ohmic contact, and Schottky contact. The critical thickness for GaInP material on InP with 18% Ga content is 150 Å [2]. In this work, we grew 150 Å GaInP material with 10% Ga content on InP. All the epitaxy layers in this work were grown by LP-MOCVD on S.I. InP substrates using triethylgallium (TEGa), trimethylindium (TMIn) and PH_3 as Ga, In and P sources respectively. After finishing the initial clean of the S.I. InP wafer, the wafer was put into the resistor heated horizontal reactor. The growth temperature was 665°C for all layers. The dopant concentration of the InP buffer layer (3000 Å) and InP active layer (1000 Å) were about 10^{16} and 2×10^{17} cm^{-3}, respectively. A conventional InP MESFET was also grown on S.I. InP wafer for comparison. The growth of the pseudomorphic GaInP/InP MESFET starts with an undoped InP buffer layer of 3000 Å, then an n-type InP active layer of 1000 Å, and stops at the undoped $Ga_{0.1}In_{0.9}P$ strained layer. The existence of the GaInP layer is analyzed by SIMS, double-crystal X-ray and Photoluminescence. From the double-crystal X-ray and PL spectrum measurements, the calculated Ga content is about 10%.

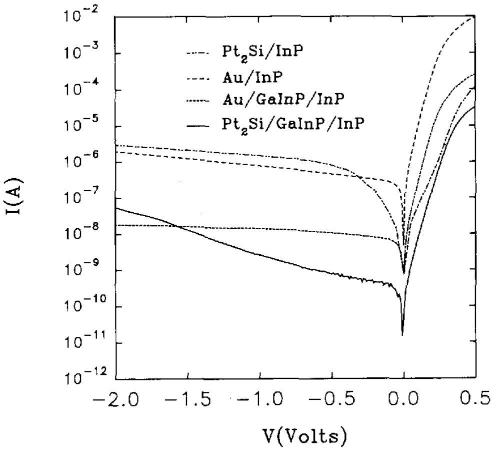

Fig. 1. The *I-V* characteristics of Schottky diodes with and without $Ga_{0.1}In_{0.9}P$ layer.

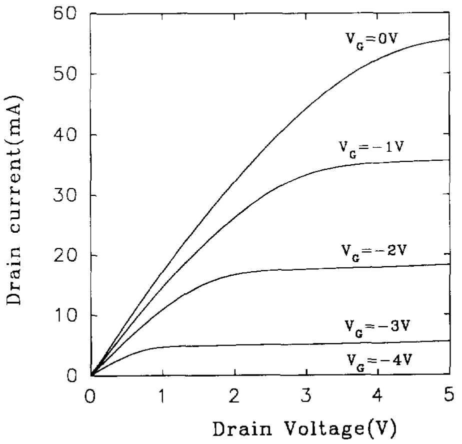

Fig. 2. The I_d-V_d curves of $Ga_{0.1}In_{0.9}P$/InP MESFET with Au gate.

Devices were processed by conventional optical lithography technique using AZ1350J photoresist. The $H_3PO_4:H_2O_2 = 1:1$ solution was used for etching the InP and $Ga_{0.1}In_{0.9}P$ layer to form mesa isolation. Ohmic metal of AuGe (12% Ge by weight) was deposited with a thickness of 2500 ~ 3000 Å on the wafer by thermal evaporator at a chamber pressure within 4×10^{-6} torr. After lift-off, the deposited metals were sintered in the conventional furnace at 360°C under N_2 and H_2 ambient for five minutes. Gate recess was performed using the H_3PO_4/H_2O_2 solution to control the pinch-off voltage. Au and Pt_2Si were used as Schottky contact metals for InP and $Ga_{0.1}In_{0.9}P$/InP MESFET's. The Au film was deposited by thermal evaporator. The single phase Pt_2Si films were formed by co-evaporation of Pt and Si elements in the dual electron gun evaporator followed by furnace annealing. This annealing is carried out with a 2000 Å SiO_2 cap. After annealing,

Manuscript received June 8, 1993; revised July 16, 1993. This work was supported in part by the National Science Council under Contracts NSC-81-0417-E009-12. The review of this brief was arranged by S. Furukawa.

K. C. Lin, Y. M. Hsin, and C. Y. Chang are with the Institute of Electronics, National Chiao-Tung University, Hsin-Chu, Taiwan, R.O.C.

E. Y. Chang is with the Institute of Materials Science and Engineering, National Chiao-Tung University, Hsin-Chu, Taiwan, R.O.C.

IEEE Log Number 9212637.

0018-9383/93$03.00 © 1993 IEEE

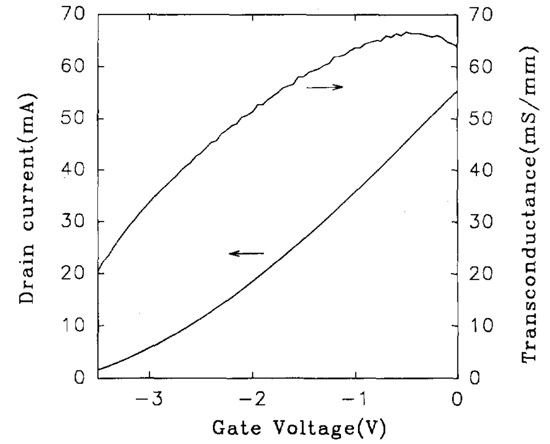

Fig. 3. The I_d-V_d and G_m-V_g curves of $Ga_{0.1}In_{0.9}P$/InP MESFET with Au gate at V_{ds} = 5 V.

the SiO_2 cap layer was removed and an overlaying Au metal was deposited on ohmic metal to improve the surface morphology and reduce the sheet resistance.

III. Results

The I-V characteristics of the Schottky diode with and without $Ga_{0.1}In_{0.9}P$ layer using Au and Pt_2Si as Schottky metal are shown in Fig. 1. As shown in this figure, when the Au Schottky metal was formed on a 150 Å $Ga_{0.1}In_{0.9}P$/InP diode, the Schottky barrier height is increased by about 0.1 eV and resulting in at least 10^{-2} times smaller reverse leakage current density in comparison with the conventional Au/InP Schottky barrier diode. The same effect is observed when Pt_2Si is used as Schottky metal on this pseudomorphic diode. The Pt_2Si/GaInP/InP diode shows a Schottky barrier height of 0.63 eV and a reverse current of 10^{-9} A. The GaInP/InP MESFET with improved Schottky characteristics has demonstrated superior device performance to the conventional InP MESFET. The conventional n-channel InP MESFET with 5 μm × 300 μm Au gate and n-type 10^{17} cm^{-3} InP active layer has shown a transconductance of 46.7 mS/mm and a Schottky barrier height of 0.46 eV. Meanwhile, the pseudomorphic $Ga_{0.1}In_{0.9}P$/InP MESFET with 5 μm × 300 μm Au gate has shown a 0:54 eV Schottky barrier height. The I-V characteristics of the pseudomorphic MESFET are shown in Fig. 2. The extrinsic transconductance with R_S = 18 Ω is 66.7 mS/mm (Fig. 3) and the intrinsic transconductance is as high as 104.2 mS/mm at $V_g = -0.45$ V and V_{ds} = 5 V.

IV. Conclusions

A thin GaInP epitaxial layer is grown on the InP MESFET to increase the Schottky barrier of the device. These MESFET's show better electrical characteristics with increased barrier heights and smaller leakage current and higher transconductance when compared to the conventional InP MESFET. For GaInP/InP MESFETs with Au gate, the Schottky barrier height observed is 0.54 eV and the reverse leakage current is 10^{-2} times lower than the conventional InP MESFET, and an intrinsic transconductance of 104.2 mS/mm is achieved for these 5 μm MESFET's.

References

[1] M. Eizenberg, M. Heiblum, M. I. Nathan, N. Braslau, and P. M. Mooney, "Barrier heights and electrical properties of intimate metal-AlGaAs junctions," *J. Appl. Phys.*, vol. 61, p. 1516, 1987.

[2] S. Loualiche, A. Ginudi, A. Le Corre, D. Lecrosnier, C. Vaudry, L. Henry, and C. Guillemot, "Pseudomorphic GaInP Schottky diode and high electron mobility transistor on InP," *Appl. Phys. Lett.*, vol. 55, p. 2099, 1989.

[3] Y.-J. Chan, D. Pavlidis, M. Razeghi, and F. Omnes, "$Ga_{0.51}In_{0.49}P$/GaAs HEMT's exhibiting good electrical performance at cryogenic temperatures," *IEEE Trans. Electron Devices*, vol. 37, p. 2141, Oct. 1990.

[4] T. F. Kuech, J. O. McGaldin, "Compositional dependence of Schottky barrier heights for Au on chemically etched $In_xGa_{1-x}P$ surface," *J. Vac. Sci. Technol.*, vol. 17, no. 5, p. 891, Sept./Oct. 1980.

Characteristics of $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$/InP HEMT's with n- and p-Channel Doping

H. Tian, K. W. Kim, M. A. Littlejohn, and U. K. Mishra

***Abstract*—The effects of modified n and p channel doping on the characteristics of 0.25 μm $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$/InP HEMTs are studied. The introduction of n- or p-channel doping (in addition to the modulation doping in the donor supply layer) is intended to modify the potential well and carrier distribution in the device channel for improved device performance. Self-consistent Monte Carlo simulations and experimental results both show considerably reduced output conductance and increased transconductance for the HEMT employing modified p-channel doping compared with those for the HEMT with modified n channel. The performance enhancement for the HEMT with modified p-channel doping is attributed to improved carrier confinement in the potential well of the channel and reduced spread in the channel electric field profile.**

The progress made in achieving high performance $In_{0.42}Al_{0.48}As/In_{0.53}Ga_{0.47}As$/InP HEMT's has been impressive. However, reports of high output conductance for devices fabricated from this lattice-matched material system have been consistent, which establishes severe limitations for high frequency and power applications [1]-[6]. The physical origin of this high output conductance has been suggested to result from: 1) weak impact ionization in the $In_{0.53}Ga_{0.47}As$ channel layer [2]; 2) electron conduction in the $In_{0.52}Al_{0.48}As$ buffer layer [2], [7]; and 3) deep level traps in the top $In_{0.52}Al_{0.48}As$ donor supply layer [4]. Experimental efforts have been made to reduce output conductance by using an undoped surface layer [3], a low-conductance drain design [6], and low temperature MBE-prepared $In_{0.52}Al_{0.48}As$ buffered layers [7]. In this brief, we examine an alternative approach for reducing the output conductance of the $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$/InP HEMT. This approach employs various amounts of intentional

Manuscript received February 17, 1993; revised August 7, 1993. The work performed at NCSU was supported in part by the Office of Naval Research and the National Science Foundation, U. K. Mishra was supported by an NSF Presidential Young Investigator Award. The review of this brief was arranged by Associate Editor P. M. Solomon.

H. Tian, K. W. Kim, and M. A. Littlejohn are with the Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC 27695.

U. K. Mishra is with the Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106.

IEEE Log Number 9212788.