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Heuristic PAC model for hybrid MTO and MTS production environment

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Abstract

Two distinct types of semiconductor plants in Taiwan are integrated device manufacturing (IDM) plants and foundry plants. Most IDM plants are make-to-stock (MTS) operations, focusing on throughput and machine utilization. However, foundry plants are make-to-order (MTO) operations, focusing on due date and cycle time. Besides the challenge of different process technology, the mode of hybrid operation (a combination of MTO and MTS operations) is also a formidable task for these plants. This study develops a heuristic production activity control model to achieve the two different criteria in a hybrid wafer production environment.

Keywords: Wafer fabrication make-to-stock; Make-to-order; Production activity control; Theory of constraints

1. Introduction

Two distinct types of semiconductor plants in Taiwan are integrated device manufacturing (IDM) plants and foundry plants, both with different operation environments. Most IDM plants are make-to-stock (MTS) operations, focusing on throughput and machine utilization, while the foundry plants are make-to-order (MTO) operations, focusing on due date and cycle time. For strategic reasons, most IDM plants in Taiwan are gradually switching their capacity to enter foundry business. Besides the challenge of different process technology, the mode of hybrid operation (combining MTO and MTS operations) is also a big challenge for these plants.

Numerous investigations, such as Samadhi and Hoang (1995), Sipper and Bulfin (1997), and Vollman et al. (1997) have discussed operating differences between MTO and MTS. Kogan et al. (1998), Adan and van de Wal (1998), Williams (1984), Nguyen (1998) and New and Szwejczewski (1995) all focused on issues of in combining MTO and MTS. These investigations agreed that planning and controlling production in a hybrid production environment is challenging. However,

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none of their research considered semiconductor plants, with their particularly complex manufacturing processes.

Many studies have considered production planning and control in semiconductor plants, which can be categorized into closed-loop and open-loop. Basically, closed-loop control is superior to open-loop control (Miller, 1990). The optimal WIP level is crucial in closed-loop systems, and the wafer is released according to the difference between actual and projected WIP levels (Graves et al., 1995). Starvation avoidance (SA) (Glassey and Resende, 1988a, b), workload regulating (WR) (Wein, 1988), two-boundary (TB) (Lou, 1989; Lou and Kager, 1989; Yan et al., 1996), CONWIP (Spearman et al., 1989; Spearman and Zazanis, 1992), fixed-WIP (Burman et al., 1986; Glassey and Resende, 1988a, b; Wein, 1988; Roderick et al., 1992), and load-oriented order release (Bechte, 1988a, b, 1994; Wiendahl et al., 1992; Wiendahl, 1995; Chang et al., 2001; Huang et al., 2001) are several well-known closed-loop control policies. However, most of these focused on the problems of either MTS or MTO, and none considered a hybrid operation environment.

In a hybrid production environment, due date and minimizing cycle time are critical for MTO orders. Filling the finished product buffer size to the required level is the focus for MTS orders. The different requirements necessitate different production plan criteria. For MTO orders, the fact that due date and minimizing cycle time are key so a rigid order release plan and dispatching control are important. The release plan ensures that the order is not released too early or too late, while the dispatching control aims to expedite late orders to achieve on time delivery. For MTS orders, owing to the focus is filling the finished product buffer size to the requisite level so a rigid order release plan and dispatching control is not important. Instead, the key is to release the order to utilize remaining capacity (after planning for MTO orders) without disturbing the released MTO orders.

Since hybrid operation is a new operating mode in wafer production, a new method of production planning and control must be developed. This work aims to develop a heuristic production activity control (PAC) model to achieve the different production criteria (for MTO and MTS) in the hybrid production environment. Fig. 1 illustrates the heuristic PAC model for hybrid wafer production. The model inputs are: workstation information, WIP information, production orders (MTO + MTS) to be processed and current shop floor information. The model itself consists of three sub-modules, the bottleneck identification sub-module, order release sub-module and order dispatch sub-module, which are detailed herein. A simulation is created to test the feasibility of the model, and a comparison drawn with other PAC methods, with the comparative results revealing that the proposed heuristic model outperforms other methods.

2. Bottleneck identification sub-module

According to the theory of constraints (TOC) (Goldratt, 1991), the throughput, due date and WIP are dominated by the utilization of bottleneck resources rather than the resources of the entire system, and thus controlling the bottleneck is crucial. First, the location of the bottleneck during the planning period must be identified. Eq. (1) is employed to calculate capacity utilization. The workstation with the highest predicted utilization (U_w) is identified as the bottleneck workstation, while workstations with 80% utilization or more are identified as capacity constrained resources (CCR). The remaining workstations are identified as non-bottleneck workstations.

$$U_w = \frac{\sum_i \sum_j X_{ij} R_{ij}}{24PN(\mathrm{MTBF}_w/(\mathrm{MTBF}_w + \mathrm{MTTR}_w))B_w}, \tag{1}$$

where 24 represents 24 h/day, U_w is utilization of workstation w, P is the length of planning period, N the number of machines in the workstation, B_w the maximal quantity that workstation w can process per unit time, MTBF_w the mean time between failure of workstation w, MTTR_w the mean time to repair of workstation w, X_{ij} the quantity of product i, jth time in the same workstation, R_{ij} the average process time of

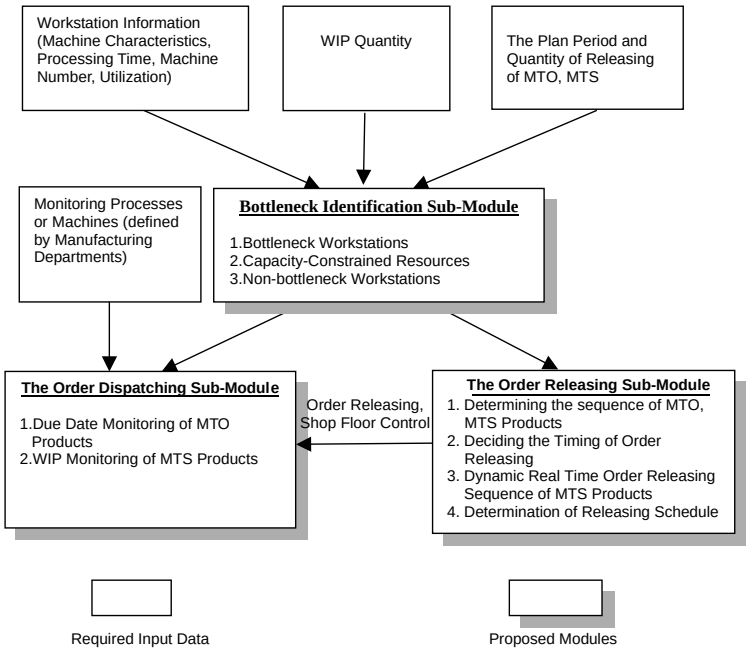

Fig. 1. The proposed model.

product i, jth time in the same workstation, i the type of product, j the number of times at same workstation, and w the number of workstation.

In Eq. (1), the denominator represents capacity available during the planning period and the numerator is the required capacity. X_{ij} is difficult to identify and control, and comprises two major elements: present WIP loading in the shop and loading for the planned releasing orders. Assume that MTO and MTS orders are distributed uniformly during the planning period. Finally, the standard cycle time is determined from historical data and is used to estimate the loading of each workstation.

3. Order releasing sub-module

As mentioned in Section 1, the release plan for MTO orders is aimed to ensure that the order is not released too early or too late. However, for MTS orders, owing to the focus on filling the finished product buffer size to the required level, a rigid order release plan is not required. Instead, the central concern is releasing the order to utilize remaining capacity (after the planning of MTO orders) without disturbing the released MTO orders. Fig. 2 displays the flow of the sub-module. The flow involves three major functions: determining the order release sequences for MTO orders, determining the order release sequences for MTS orders, and determining the time of order release for MTO and MTS orders. Each function is detailed below.

3.1. Determine the order release sequence for MTO orders

Critical ratio (CR) is applied herein as the criteria for determining the order release sequence of MTO orders. MTO orders are sequenced according the calculated CR value, with release priority increasing with decreasing CR value. Because the order release sequence depends on the capacity loading of the shop floor, it is difficult to estimate the CT_i for the first period. Consequently, the UNIFORM and FIFO are integrated and used as the rule for estimating the CT_i during

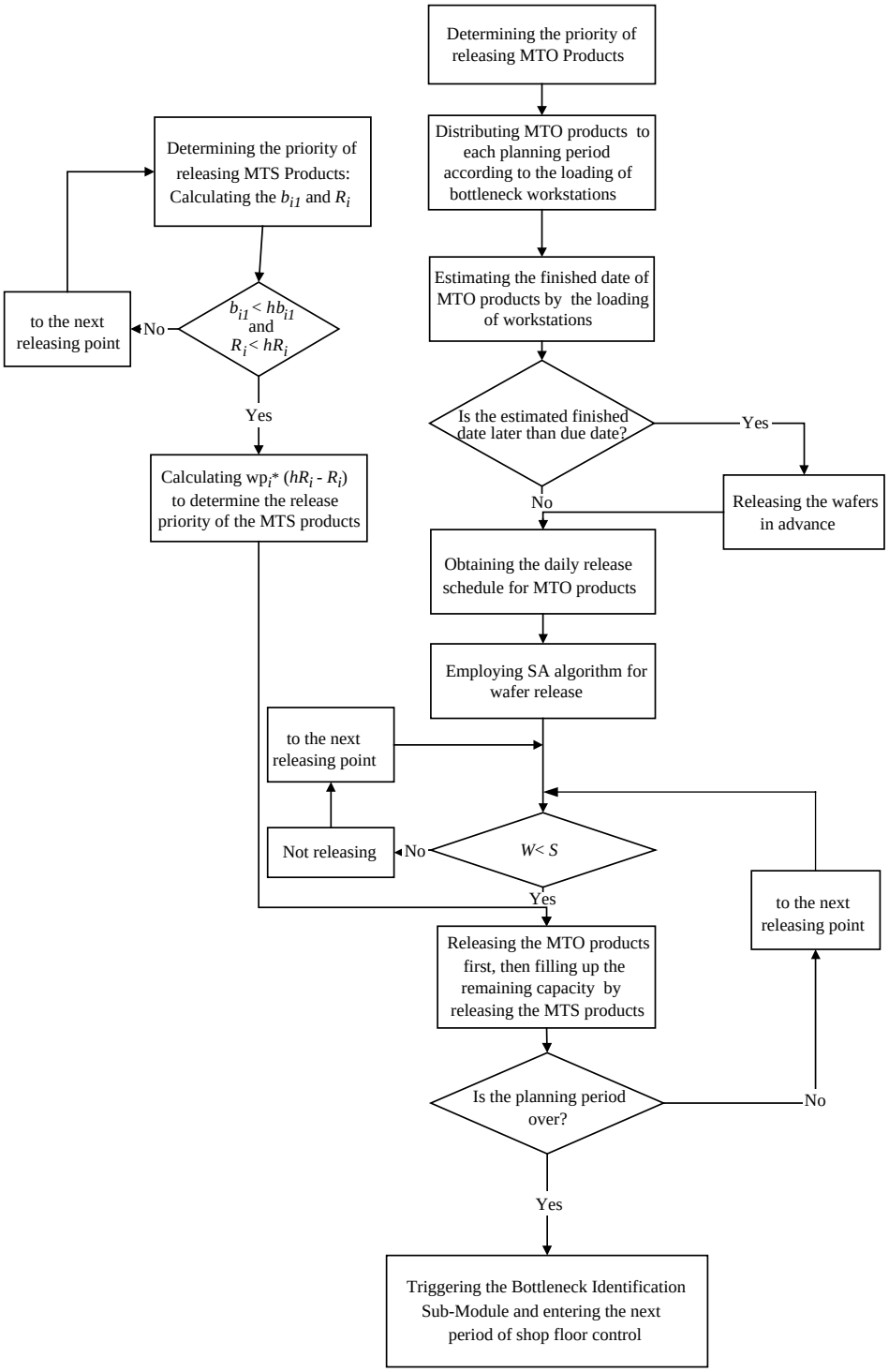

Fig. 2. The flow of order releasing sub-module.

the first production period. The CR value is calculated as follows:

$$CR_{i,k} = (T_{due\ i,k} - T_{now})/CT_i, \quad (2)$$

where $CR_{i,k}$ is the CR of ith product for kth batch, $T_{due\ i,k}$ the due date of ith product for kth batch, T_{now} the present time, CT_i the predicted cycle time of product i.

According to Park and Salegna (1995), the leveling of the bottleneck loading determines the cycle time and due date performance. Therefore, the bottleneck loading is leveled with the MTO orders for each planning period. Continuing this approach, the next step is to allocate the sequenced MTO orders to the planning horizon according to bottleneck loading. The slack capacity of the bottleneck after leveling will provide for insertion of the MTS orders. However, this leveling approach is still unable to guarantee that all MTO products will meet the due dates if the non-bottleneck becomes a temporary constraint, and this situation must still be identified before order release, and the delayed orders must be released again in advance of the original planned schedule. The sequenced MTO orders are allocated based on the average daily loading of the bottleneck of each planning horizon. The average daily loading (DL_{MTO}) is calculated using the following expressions:

$$TL_{MTO} = \sum_{i \in MTO} \sum_{j} X_i R_{ij}, \quad (3)$$

$$DL_{MTO} = TL_{MTO}/P, \quad (4)$$

where X_i is the quantity of product i planning to release during the planning horizon, R_{ij} the average processing time of product i, jth time at bottleneck resources, P the length of planning period.

The accumulated daily loading of the bottleneck cannot exceed DL_{MTO}.

3.2. Determine the order release sequence for MTS orders

The release of MTS is planned so as to fill up the capacity remaining after the scheduling of MTO orders. Therefore, a dynamic real time order release approach is specified here to deal with problems related to the release of MTS orders. The release of an MTS order is planned only when the shop floor loading is below a certain level (S) Δb_{il} and ΔR_i (Eq. 5) are used to determine which MTS orders should be scheduled for release.

$$\begin{aligned} \Delta b_{i1} &= hb_{i1} - b_{i1} > 0, \\ \Delta R_i &= hR_i - R_i > 0, \end{aligned} \quad (5)$$

where i is the product type, b_{i1} the actual WIP (visit the bottleneck first time) before the bottleneck, hb_{i1} the accumulated WIP before the product i visit the bottleneck first time, R_i the actual accumulated output, hR_i the projected accumulated output.

If both b_{i1} and R_i are below hb_{i1} and hR_i, then activate the MTS order. If more than two MTO orders can be released, the value of $(wp_i \Delta R_i)$ where wp_i is denoted as the MTS order weighting, is used as release priority, with release priority increasing with the value of $(wp_i \Delta R_i)$.

3.3. Release the planned MTO and MTS orders

The SA approach developed by Glassey and Resende (1988a) is employed here to release orders. The buffer time (S) before the bottleneck and the loading time of the bottleneck (W) are obtained first using the following equation:

$$L = \max(L_i), \quad (6)$$

$$S = \alpha L, \quad (7)$$

$$W = T_Q + T_R, \quad (8)$$

where α is the number of bottleneck workstations (Chung et al., 1997), L_i the total time of all operations of product i from release to bottleneck workstation, T_Q the time that needed process all wafer batches with the maximal total processing time less or equal to L, T_R the total workstation repair time before bottleneck workstation.

In the SA approach, the higher the value of α, the better for preventing starvation of bottleneck workstations. In this work, α represents the number of bottleneck workstations (Chung et al., 1997). If the value of W is less than that of S, the

orders are released, and otherwise they are not released until the next evaluation period. If the orders are released, the MTO orders are released first according to the MTO order releasing sequence, after which the MTS products are released.

4. Order dispatching sub-module

The order dispatching sub-module attempts to dynamically prioritize orders at each control point. The bottleneck, capacity constraint resources and management assigned critical resources are defined as the control point in the dispatching sub-module. Table 1 summarizes the proposed dispatching rules for MTO and MTS at different types of workstations. Meanwhile, Fig. 3 illustrates the flow of the order dispatching sub-module. The details of the flow are as follows.

4.1. Dispatching rules for MTO orders

Every MTO order, upon arrival at the control point, initiates computation of the SLACK time (Eq. 9):

$$S_{ike} = (D_{ik} - T_{\text{now}}) - R_{ike}, \tag{9}$$

where S_{ike} is the slack of product i, kth wafer batch, eth process; D_{ik} the due date of product i, kth wafer batch; T_{now} the present time; R_{ike} the total remaining standard processing time of product i, kth wafer batch, eth process.

If the SLACK is negative, then the order will be unavoidably delayed unless action is taken, and the order is placed in queue 1. Otherwise, computation of operational SLACK continues. The equation is

$$\text{OS}_{ike} = (\text{OD}_{ike} - T_{\text{now}}) - T_{ie}, \tag{10}$$

$$\text{OD}_{ike} = D_{ik} - (D_{ik} - r_{ik})\frac{\sum_{l=e+1}^{E_i} T_{il}}{\sum_{l=1}^{E_i} T_{il}}, \tag{11}$$

where OS_{ike} is the slackness of product i, kth wafer batch, eth process; OD_{ike} the due date of product i, kth wafer batch, eth process; T_{ie} the processing time of product i, kth wafer batch, eth process; r_{ik} the releasing time of product i, kth wafer batch; E_i the last process of product i; L the processing step.

If the operational SLACK is negative, then the order is delayed at this operation only, and the order is placed in queue 2. Otherwise, the order has not delayed and is put into queue 3.

The dispatching priority is ranked according to the orders in queues 1, 2, and 3. The SRPT dispatching rule is used to prioritize orders in the same queue. Integrating the three queue control concepts with the SRPT policy can achieve due date, cycle time, and throughput simultaneously (Blackstone et al., 1982).

4.2. Dispatching rules for MTS orders

Since the MTS orders are scheduled to maximize throughput of the bottleneck, they are automatically placed in queue 4 upon arriving at the bottleneck. The SRPT rules are applied to schedule MTS orders in queue 4 after the scheduling of all orders in queues 1, 2 and 3. However, the problem with this approach is that too many MTS WIPs stay in front of the bottleneck workstation or too few MTS WIPs remain in

Table 1
Releasing disciplines of MTO and MTS products on different workstation

Workstation	MTO product	MTS product
Bottleneck workstation	Breaking into three pseudo-queueing lines to show the rush of order as well as adjust the production priority	Avoiding short of material for bottles and keeping producing products smoothly
Capacity-limited workstation	Breaking into three pseudo-queueing lines to show the rush of order as well as adjust the production priority	Keeping the quantity of WIP under control to avoid temporary bottleneck and producing products smoothly
Non-bottleneck workstation	FIFO*	FIFO

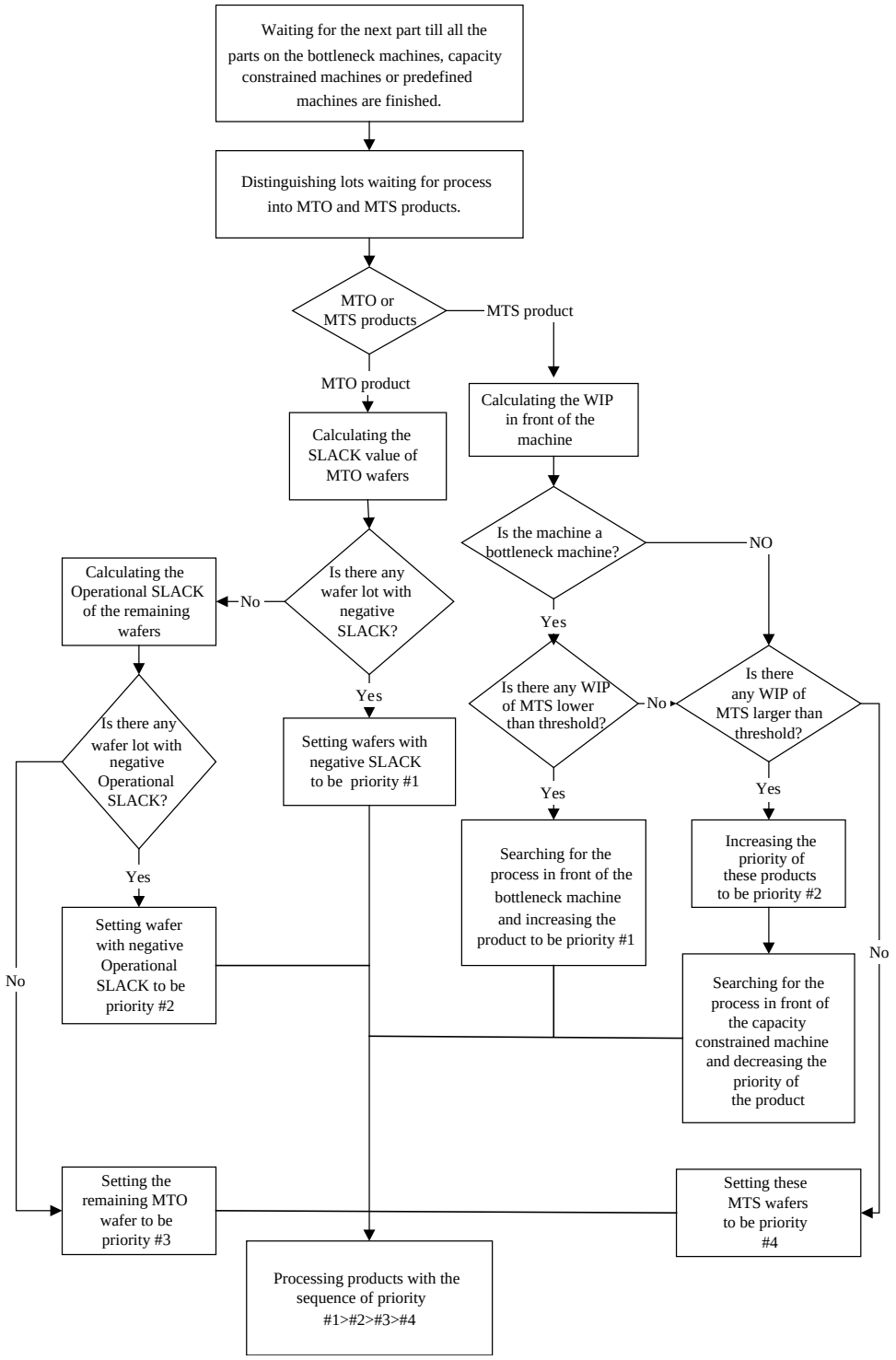

Fig. 3. The flow of the order dispatching sub-module.

the processes before the bottleneck. The former compromises the smooth output of MTS orders, while the latter causes starvation of the bottleneck workstation. Should either one of these occur, the MTS priority needs to be adjusted. The upper and lower bounds of the WIP of the bottleneck are used as a guide to adjust the priority of the MTS orders.

If the WIP of MTS(b_{ie}) is less than the lower bound of WIP(Lhb_{ie}), then WIP of the MTS order is insufficient. An order is supposed to pass to the previous workstation to accelerate the throughput of MTS orders. The following rule is borrowed from JIT. The order dispatching priority for MTS in the previous workstations is revised as $wp_i * (Lhb_{ie} - b_{ie})$, with the priority increasing with the value of this formula.

If the WIP of MTS(b_{ie}) exceeds the upper bound of WIP (Uhb_{ie}), then the WIP of the MTS order is too high. The priority of MTS products in front of the bottleneck workstation should be increased to ensure that the throughput of MTS products is smooth. In this case, the MTS orders with threshold values exceeding the set value are assigned to queue #2 to increase the priority of the MTS order.

A threshold (*UhCCRie*) is required to control the WIP of capacity constrained workstations. The processing priority is altered to #2 when WIP (*CCRie*) is larger than *UhCCRie*. To reduce the number of orders coming from upstream workstations, the processing priority should be decreased. Another index $(CCRie - UhCCRie)/\mathrm{wp}_i$ is employed here to determine the processing priority when some *CCRie* are larger than *UhCCRie*. The priority decreases with increasing $(CCRie - UhCCRie)/\mathrm{wp}_i$.

The FIFO dispatching rule is applied to non-bottleneck workstations because of their sufficient capacity. The FIFO discipline can reduce cycle time and throughput variation (Wiendahl, 1995). However, the previous rules should be adjusted when the WIP of downstream bottleneck workstations is too high.

5. Simulation experiments

To confirm the usefulness of the proposed model, a virtual wafer fabrication shop was designed with the SIMPLE++. The data were obtained from a Taiwan semi-conductor manufacturing plant, and four different products were created (A, B, C, and D). Products A and B are MTS products, while products C and D are MTO products. The system contains a total of 24 workstations (from W1 to W24). Stations W1, W2, W3, and W4 are batch process stations, with a batch size of six. The ratio of MTS to MTO products is assumed to be 5:5. From the viewpoint of long term, the product mix ratio of MTS and MTO is as follows: A:B:C:D = 1:1:1:1. However, to verify the capability of the proposed model for dealing with the change of product mix, the proportion of MTS and MTO products of products A, B, C, D is generated as follows: A:B = 2:1 and C:D = 1:2 randomly. Due dates are based on the capacity of the MTO products. Finally, the due date for each MTO order is determined using

$$D_{ik} = a_{ik} + P_i\, R(a, b), \tag{12}$$

where D_{ik} is the due date of product i, kth order; a_{ik} the arrival date of product i, kth order; P_i the total processing time of product i; $R(a, b)$ the random distribution, the interval between a and b; i the MTO product.

To simplify the problem, we assume that only one kind of product of MTO orders exists. Owing to the due date of MTS products being more flexible than that of MTO products, the due dates of MTS products (A and B) are obtained by multiplying 1.5 from Eq. (12). The values of a and b in Eq. (12) depend on the system loading. Generally, the ratio of actual to theoretical cycle time is between 2.5 and 10 (Lu et al., 1994). The values of a and b are 3.5 and 5.5, respectively, in this study. The simulation period was 140 days, with the first 70 days being for initial simulation, while data were collected after the 70th. Thirty iterations were conducted to test the hypothesis statistically.

Before running the system, the bottleneck resources, CCR, orders release time, and threshold values of MTS products releasing rule have to be identified. Eq. (1) identified workstation W14 as a bottleneck workstation with 100% utilization, while workstation W7 was identified as a capacity

constrained workstation with 94% utilization. The next step is to calculate the duration of the first time (L_i) of arrival at the bottleneck workstation (W14) of four kinds of products, A, B, C and D, and select the maximum value of four vales (L). Here, $L = L_C = 100{,}260$ seconds. Since 14 workstations are used, the value of buffer time (S) is 300,780 ($3L$) seconds. The fixed-WIP approach is employed to obtain threshold values for MTS products releasing and dispatching rules. Simulation is used to estimate the minimum WIP capable of maximizing utilization and throughput. The above calculation can be used to obtain hb_{i1}, hR_i of MTS products.

Table 2
Overall performance analysis

Performance index	PAC methods	Average	Results of Duncan testing
WIP (lots)	Proposed method	152.4	A
	Uniform-SRPT*	190.6	B
	FW-FIFO*	192.0	B
	Uniform-EDD*	233.7	C
	Uniform-FIFO	237.1	D
	Uniform-SLACK	275.3	E
Cycle time (h)	Uniform-EDD	960.1	A
	Proposed method	1020.8	B
	Uniform-SRPT	1028.5	BC
	FW-FIFO	1050.2	C
	Uniform-SLACK	1270.3	D
	Uniform-FIFO	1325.1	E
Throughput (lots)	Proposed method	286.2	A
	FW-FIFO	279.8	B
	Uniform-SRPT	275.4	B
	Uniform-EDD	268.2	C
	Uniform-FIFO	262.6	C
	Uniform-SLACK	255.3	D

System performance is evaluated from three perspectives: total performance, performance of MTO products, and performance of MTS products. To demonstrate the advantages of the proposed approach, several PAC order releasing policies: Uniform-FIFO (first-in first-out), Uniform-SRPT (shortest remaining processing time), Uniform-EDD (earliest due date), Uniform-SLACK, and FW-FIFO (fixed-wip–first-in first-out) are compared herein. Duncan's Multiple Range Test is used to analyze all indices, and the indices are graded into five levels, namely A, B, C, D, and E, ordered decreasingly. Table 2 compares overall performances. The proposed approach outperforms the alternative methods in terms of WIP, cycle time, and throughput. Table 3 lists the performance of MTO products, revealing that the proposed approach outperforms other methods in terms of cycle time, average tardiness, and achievement of target due date. Meanwhile, Table 4 lists the comparison of standard deviation of cycle time and average tardiness with the

Table 3
Statistic analysis of the average cycle time, average tardiness, and achievement percentage of due dates of MTO products

Performance index	PAC methods	Average	Results of Duncan testing
Cycle time (h)	Proposed method	726.5	A
	Uniform-EDD	1016.4	B
	Uniform-SLACK	1039.5	BC
	Uniform-SRPT	1050.5	C
	FW-FIFO	1100.9	D
	Uniform-FIFO	1404.2	E
Average tardiness (h)	Proposed method	2.2	A
	Uniform-SLACK	112.4	B
	FW-FIFO	162.0	C
	Uniform-SRPT	171.2	C
	Uniform-EDD	172.7	C
	Uniform-FIFO	459.3	D
Due date achievement percentage (%)	Proposed method	92.4	A
	Uniform-EDD	51.1	B
	Uniform-SLACK	47.5	C
	Uniform-SRPT	37.4	D
	FW-FIFO	19.0	D
	Uniform-FIFO	00.0	E

Table 4
Statistic analysis of standard deviation of cycle time and standard deviation of average tardiness of MTO products

Performance index	PAC methods	Average	Results of Duncan testing
Standard deviation of cycle time (h)	Proposed method	72.4	A
	FW-FIFO	103.1	B
	Uniform-FIFO	140.2	C
	Uniform-SRPT	284.4	D
	Uniform-SLACK	294.4	D
	Uniform-EDD	375.9	E
Standard deviation of average tardiness (h)	Proposed method	53.1	A
	FW-FIFO	126.8	B
	Uniform-FIFO	167.9	C
	Uniform-SRPT	231.9	D
	Uniform-SLACK	260.4	E
	Uniform-EDD	422.3	F

Table 5
Analysis of average cycle time and through rate of MTS products

Performance index	PAC methods	Average	Results of Duncan testing
Average cycle time (h)	Uniform-EDD	913.4	A
	Uniform-SRPT	979.9	B
	FW-FIFO	1001.9	B
	Uniform-FIFO	1266.5	C
	Proposed method	1405.9	D
	Uniform-SLACK	1555.9	E
Through rate (lots/week)	FW-FIFO	13.8	A
	Uniform-FIFO	13.5	AB
	Uniform-EDD	13.4	AB
	Uniform-SRPT	13.1	ABC
	Proposed method	12.9	BC
	Uniform-SLACK	12.5	C

application of different order releasing rules. The proposed approach has clear advantages in reducing the deviation of both cycle time and tardiness, both of which are extremely important in MTO products. Due dates are easier to estimate and thus control, while deviation of cycle time and tardiness are small. Table 5 indicates that the proposed approach for MTS products only outperforms Uniform-SLACK discipline in average cycle time and throughput rate. The reason is that the order releasing rules of MTS products focus more on preventing the starvation of bottleneck workstations rather than due date. However, the proposed approach differs little from Uniform-FIFO, Uniform-EDD, and Uniform-SLACK in the results of the Duncan test. Finally, Table 6 lists that the performance of the proposed approach for MTS products is around the middle of all methods in terms of standard deviation of cycle time and throughput. Basically, the proposed approach outperforms other PAC approaches for MTO products, but displays no obvious advantage for MTS products.

6. Conclusion

This work developed a heuristic production activity control model to schedule and control wafer manufacturing in a hybrid wafer production environment (MTO and MTS). The proposed model considered due date and cycle time reduction for MTO orders, and thus developed a rigid order release plan and dispatching control. The rigid release plan ensures that the order will not be released too early or late, while the dispatching control expedites late orders to allow timely delivery. However, for MTS orders, owing to the focus on filling the finished product buffer size to an appropriate level, a rigid order release plan and dispatching control is not important. Instead, the proposed model developed a method of releasing the orders so as to fill up remaining capacity (after the MTO orders have planned) without disturbing the released MTO orders. A comparison was drawn with other PAC methods, with the comparative results showing that the proposed heuristic model outperformed the other methods.

Table 6
Statistic analysis of the standard deviation of cycle time and the standard deviation of throughput of MTS products

Performance index	PAC methods	Average	Results of Duncan testing
Standard deviation of cycle time (h)	FW-FIFO	105.2	A
	Uniform-FIFO	107.5	A
	Uniform-EDD	326.9	B
	Proposed method	329.8	B
	Uniform-SRPT	365.4	C
	Uniform-SLACK	425.4	D
Standard deviation of throughput (lots)	FW-FIFO	4.0	A
	Uniform-EDD	4.3	AB
	Uniform-FIFO	4.5	BC
	Proposed method	4.8	C
	Uniform-SRPT	5.5	D
	Uniform-SLACK	6.3	E

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