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Single-inductor dual-output (SIDO) DC–DC converters for minimized cross regulation and high efficiency in soc supplying systems

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Abstract A compact size and high efficiency single-inductor dual-output (SIDO) DC–DC converter is proposed. The proposed SIDO DC–DC converter not only provides dual output sources (one buck and one boost outputs) but also has minimized cross regulation without using any external compensation components. Generally speaking, it is important to minimize the number of components and footprint area in the design of SIDO converters. However, usually large external compensation resistors and capacitors are required to stabilize DC–DC converters. Importantly, our proposed hysteresis mode operation can effectively avoid the oscillation problems that may exist in many SIMO designs. Furthermore, the dynamic dc current level like that in the continuous conduction mode (CCM) operation can make the proposed SIDO DC–DC converter achieve high conversion efficiency at light loads owing to small conduction loss. Experimental results show a high efficiency from 85% at light loads to 94% at heavy loads.

Keywords Single-inductor dual-output (SIDO) DC–DC converter · Continuous conduction mode (CCM) · SoC system · Cross regulation

1 Introduction

Among the numerous requirements included in the ability to build high-performance system-on-chip (SoC) systems, the imperative demand is to supply multiple voltages by only using single inductor. For example, for providing the supply multiple voltages to control the LCD panel, the system needs many DC–DC converters to generate different supply voltage levels. The disadvantage is the demand of many large inductors. Compact size and low cost solution is the most popular demand for reducing footprint area of portable devices. In order to have the advantage of compact size, several popular commercial products like TPS65120 (http://focus.ti.com/docs/prod/folders/print/tps65120.html) and MAX1518 (http://www.maxim-ic.com/quick_view2.cfm/qv_pk/5154) provide three to four output voltage levels to supply an LCD panel by using only one inductor. As we know, the compact solution and low power consumption is needed for LCD panels. In other words, single-inductor-multiple-output (SIMO) converters have the advantage of power supplying system using only one large inductor. The footprint area can be effectively reduced. It is necessary to provide good regulation performance and simultaneously ensure the regulator's stability for the design consideration for SIMO DC–DC converters. In other words, several techniques are demanded for improving regulation performance and reducing voltage ripples in order to supply multiple voltages to SoC systems. Thus, it is important to design a converter with single inductor to supply multiple output voltage levels. That is how to use minimized the number of switches and cross regulation becomes the most important design issue.

SIMO DC–DC converters [1–3] can provide a compact, high efficiency and low cost solution for portable applications. The design methodology of SIMO DC–DC converters is to minimize cross regulation and the number of switches [1–3]. Therefore, it is a challenge for SIMO DC–DC converters to provide one buck and one boost outputs at the same time when the design is limited to minimized the number of switches and cross regulation.

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There are many single-inductor-dual-output (SIDO) converters proposed to provide dual buck or boost outputs [4–8]. However, the number of switches cannot be effectively reduced due to the cross regulation performance.

The design of SIDO converter that contains one buck and one boost outputs [1] provides a solution with minimized the number of switches and the value of cross regulation. It is interesting to use only four switches to deliver two outputs (one buck and one boost outputs) like the other SIDO converters with two boost outputs. The advantage of this design technique is the simple compensation gained from the existence of freewheel stage like the operation of discontinuous conduction mode (DCM). The inductor is shorted and the energy is reserved at the freewheel stage. The advantage of the freewheel stage is that the behavior of the system is like that operating in DCM mode. Thus, the proportional-integrator (PI) compensator can be used to extend the system bandwidth. However, the instability problem may happen in the SIMO converters [1–3] when the inductor current cannot be decreased because the energy stored in the inductor cannot be released. The energy is accumulated in the inductor when the buck output gets energy. The inductor current cannot be decreased to its predefined DC level when the boost output gets energy. Thus, the instability problem occurs and the regulation is deteriorated. Besides, the power conversion is seriously decreased at light load condition due to fixed and large dc level for pseudo-continuous conduction mode (PCCM) operation [1]. In the meanwhile the output ripples are enlarged owing to slow response of the comparators and large dc current in the inductor.

The PCCM converter can provide large current by storing enough dc current in the inductor at the starting of every switching period and minimize cross regulation by keeping the freewheel stage at the end of every switching period. Besides, large-gain bandwidth and fast transient response are easily achieved because there is only one low-frequency pole in the power-stage transfer function. For the design of SIMO converters, it is a difficult problem to implement a dual output converter to have one buck and one boost with minimized switch transistors. An interesting SIDO with charge-control and PCCM techniques was proposed in [1]. The advantages of this circuit are simple compensation requirements and fast transient response. Besides, it can also simultaneously provide step-up and step-down converters that adopt the time-multiplexing charge-control scheme with a reduced number of switches. The time-multiplexing charge-control PCCM technique exhibits advantage to regulate output value and reduce the number of switches.

It is obvious to find the disadvantages of this technique. The predefined level of I_{dc} only provides limited power to the load and deteriorates power conversion efficiency at light load condition. Thus, a dynamic I_{dc} proportional to the load variations is needed for not only having the capability to handle large current variations, but also improving power conversion efficiency at light load condition.

In this paper, a PCCM SIDO DC–DC converter with charge reservation circuit, load dependent DC-level circuit, and mode switch mechanism is proposed to meet large load transient demand. The remainder of the paper is organized as follows. Section 2 describes the charge-control time-multiplexing SIMO converters. Section 3 describes the dynamic dc level and the hysteresis mode in the proposed SIDO DC–DC converter. In Sect. 4, experimental results show the minimized cross regulation and performance of the proposed circuit. Finally, a conclusion is made in Sect. 5.

2 Limitations of the charge-control time-multiplexing SIMO converters

For charge-control time-multiplexing SIMO converters, the charge derived from the inductor current is monitored cycle by cycle [1]. At the beginning of the operation, the inductor current is charged to a predefined level of I_{dc}, which is set to a dc level that is high enough to provide the maximum load current for both output loads. At light load operation, the converter stays at freewheel stage for a long time and thus the conversion efficiency is decreased due to the high level of I_{dc} value. On the other hand, at heavy loads, the controller leaves the SIMO converter to operate in PCCM. The efficiency is raised to be compatible to the converter operated in CCM. However, during the transition from light to heavy load condition, the period of freewheel stage may disappear as shown in Fig. 1. The converter behaves as a voltage-mode converter operated in CCM. Namely, the converter contains the dual LC poles like the voltage-mode operation in CCM mode. The system may be unstable due to the dual poles generated by the output inductor and capacitor. All the advantages of PCCM operation like those in DCM mode operation disappear and the settling recovery time is extended. In other words, the system compensation needs the complex and expensive proportional-integrator-differentiator (PID) compensator even that the system contains only one pole that is compensated by PI compensator at light and medium loads [1–3].

Furthermore, when the time-multiplexing charge-control converter with PCCM technique operates at standby or slight loads, the two output voltages may be unstable due to slow recovery time of charging capacitors in the charge control circuit. The large predefined level of I_{dc} may overcharge the capacitors C_{ia} and C_{ib}. The overcharging problem and the slow response of comparators make the

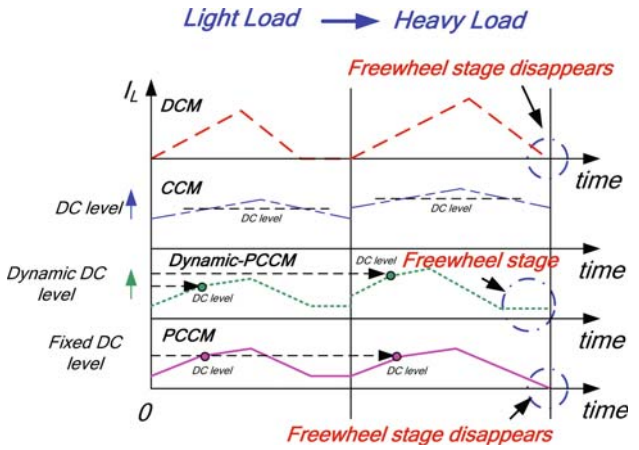

Fig. 1 Scenarios of different operation modes when load current changes from light to heavy

two outputs be increased to a high voltage level. An unstable possibility may exist in time-multiplexing charge-control converter with PCCM technique.

Another one oscillation problem not mentioned in the literature is an instability problem occurring when the power dissipation of the buck output is large than that of the boost output. The charge flowing from the supply source is not only delivered to the buck output but also accumulated in the inductor during the period of the buck mode. The reason of the instability problem is that the output of the buck converter gets energy from power supply source and accumulates energy in the inductor at the same time. The dc level of the inductor current is further increased every switching cycle. Owing the higher and higher the dc level of the inductor, extra energy will be stored at the boost output of the SIDO converter. It is the instability problem caused by the current accumulation during the period of the buck mode. As a result, the cross regulation is more and more serious. Figure 2 shows the scenario of the instability problem. Thus, it is important to provide a method to solve the instability when the power dissipation of the buck output is larger than that of the boost output. At the same time, the control of the dc level is also an important issue to minimize the cross regulation and improve the conversion efficiency at light loads. The dynamic dc level and the hysteresis mode can effectively solve the instability problem and improve the conversion efficiency.

3 Dynamic DC level and the hysteresis mode in the proposed SIDO DC–DC converter

The schematic of the proposed SIDO converter is shown in Fig. 3. The circuit contains three basic sub-circuits, which are charge reservation circuit in Fig. 4, load-dependent DC-level circuit in Fig. 5(a), and PWM control logic generator in Fig. 6(a). The following subsections describe the functions of these circuits.

3.1 Charge reservation circuit

The charge reservation control circuit is utilized to decide the duties of the two outputs. Owing to the predefined dc level, which is controlled by the load current condition, the slope compensation that is needed in current-mode control for stabilizing the system in case of current perturbation is not required. The prior technique has the disadvantage of overcharging problem because of the limited response of comparator in case of light load current. It is obvious that if the charge on the internal capacitor is fully discharged, the internal capacitor needs a long recovery time to have a voltage to determine the duty by the error amplifier. At light loads, it will incur an overcharging current and make the system unstable. Therefore, a new charge reservation circuit is proposed in Fig. 4.

Different from the previous design of SIDO converters, our proposed charge conservation circuit copies the charge condition at the output capacitors for precisely control the charging/discharging time. The discharging capability of capacitor C_{ia} or C_{ib} is proportional to the load current I_{La} or I_{Lb}, respectively. Thus, only a little of charge on internal capacitor C_{ia} or C_{ib} is discharged during the discharging period for buck or boost outputs. It

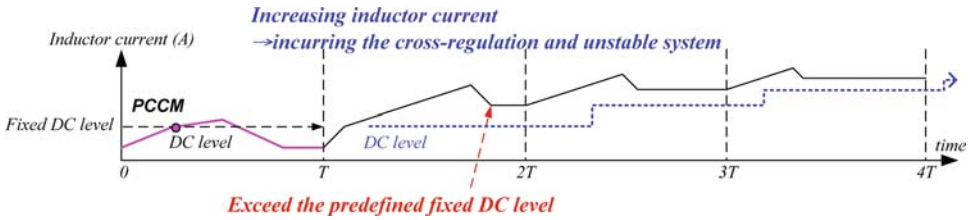

Fig. 2 There is a serious cross regulation since the output of the boost output is affected by the heavy-load buck output. The inductor current cannot be pulled down since the power dissipation of the boost output is smaller than that of the buck output

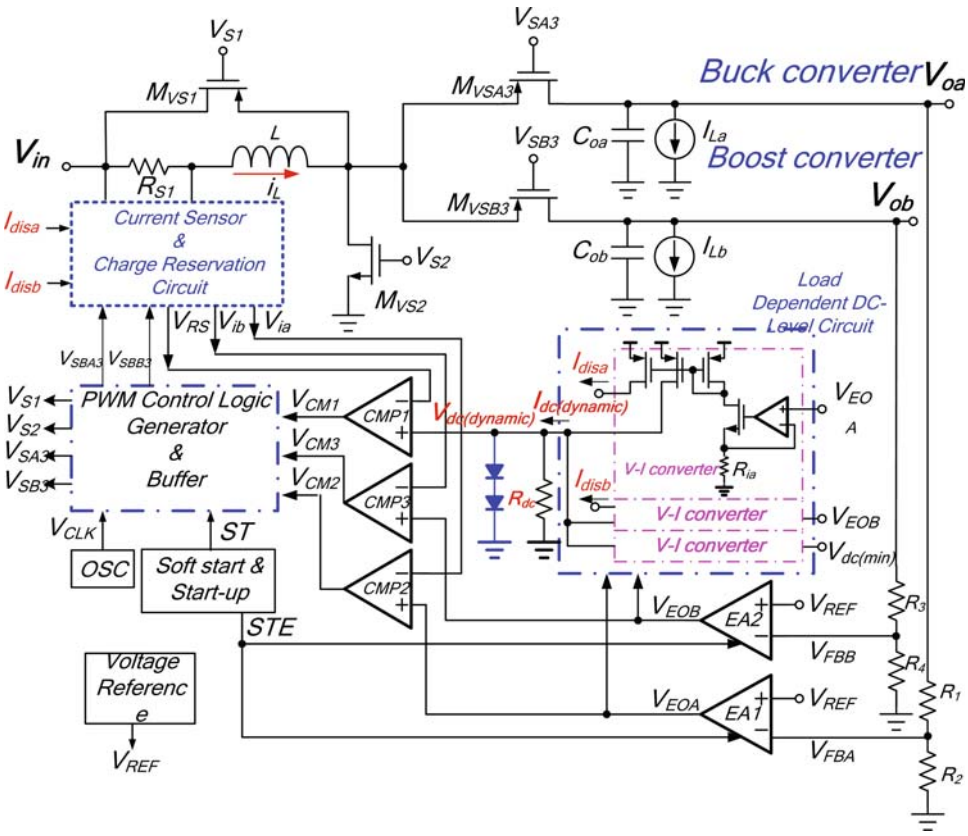

Fig. 3 SIDO converter with load dependent DC-level circuit for higher power conversion efficiency and charge reservation circuit for fast transient response at light loads

means that only a little charge is restored back to the buck or boost output at light loads. The overcharging problem is solved since capacitor C_{ia} or C_{ib} is charged according to the load condition. The advantage of the charge reservation circuit is that the internal capacitor C_{ia} or C_{ib} can faithfully represent the buck or boost output voltage status. Hence, the dual outputs have small ripples and are regulated even when the converter operates at very light load.

In Fig. 4, assume that the two output ripples ΔV_{oa} and ΔV_{ob} of two outputs are:

$$\Delta V_{oa} = \frac{1}{k_a}\Delta V_{ia}, \tag{1}$$

for the buck output of the SIDO converter

$$\Delta V_{ob} = \frac{1}{k_b}\Delta V_{ib}, \tag{2}$$

for the boost output of the SIDO converter

The values of k_a and k_b are the ratios of the input sensing voltages that converted from sensing currents to the output ripples, respectively. The values of ΔV_{ia} and ΔV_{ib} are set within the input range of the comparator in Fig. 3.

Beside, the value of I_L is N times that of I_{sense}, which is the sensing current of the buck or boost output. Thus, the values of internal capacitors C_{ia} and C_{ib} are given by (3) and (4), respectively.

$$C_{ia} = \frac{I_{sense}}{I_{La}}\frac{1}{k_a}C_{oa} = \frac{1}{Nk_a}C_{oa}, \tag{3}$$

for the buck output of the SIDO converter

$$C_{ib} = \frac{I_{sense}}{I_{Lb}}\frac{1}{k_b}C_{ob} = \frac{1}{Nk_b}C_{ob}, \tag{4}$$

for the boost output of the SIDO converter

In order to get a discharging current proportional to the load current, the values of the resistors R_{ia} or R_{ib} shown in the V–I converter of Fig. 5(a) is needed to be carefully defined. As a result, the charge reservation circuit in the SIDO converter can accurately discharge the charge stored in the capacitor C_{ia} or C_{ib} by the discharging current that is proportional to V_{EOA}/R_{ia} or V_{EOB}/R_{ib} for the buck or boost output.

$$V_{ia} = I_{disa}\frac{t_a}{C_{ia}} = \frac{V_{EOA}}{R_{ia}}\frac{t_a}{C_{ia}} \tag{5}$$

$$V_{EOA} = G(V_{REF} - \beta_a V_{oa}) = G\left(V_{REF} - \beta_a \frac{I_{La}t_a}{Nk_aC_{ia}}\right) \tag{6}$$

V_{EOA} and G are the output error signal and transconductance of the error amplifier $EA1$, respectively. β is the feedback factor in the closed loop. The value of t_a represents the discharging time of the capacitor C_{ia}. The discharging current I_{disa} is defined as (7), which is

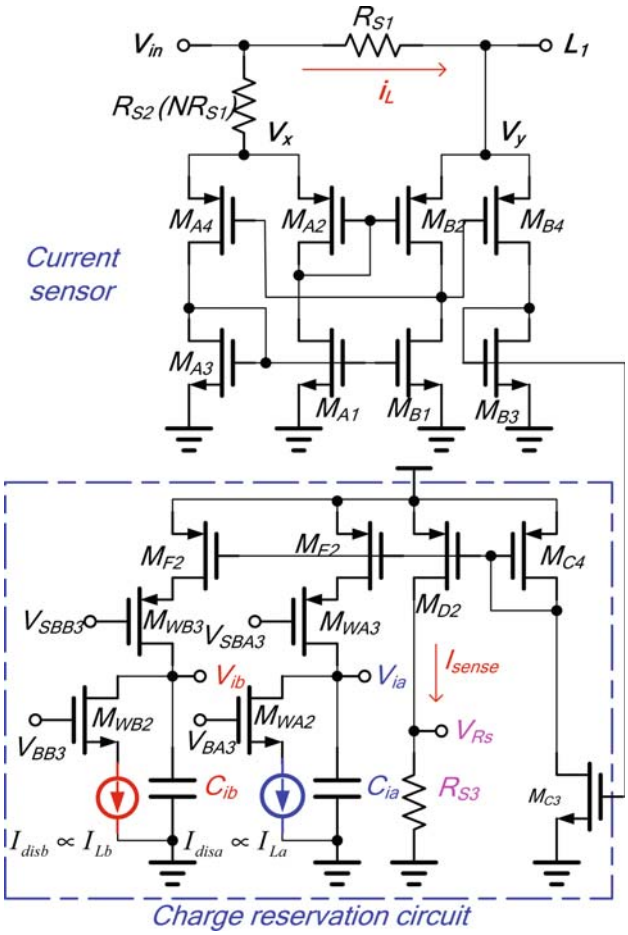

Fig. 4 The current sensor [1] and charge reservation circuits for reducing the output ripples

expressed as that the error signal V_{EOA} is divided by the internal resistor R_{ia}.

$$I_{disa} = \frac{V_{EOA}}{R_{ia}} = \frac{G(V_{REF} - \beta_a V_{oa})}{R_{ia}} = \frac{G}{R_{ia}}\left(V_{REF} - \beta_a \frac{I_{La} t_a}{N k_a C_{ia}}\right) \quad (7)$$

Differentiate both sides of (7) by load current I_{La} and set the value equal to one as shown in (8) for getting a discharging current that is proportional to the output load current. Consequently, Eq. 9 defines the value of the resistor R_{ia} in the charge reservation circuit for the buck output of the SIDO converter.

$$\frac{\partial I_{disa}}{\partial I_{La}} = \frac{G\beta_a t_a}{R_{ia} N k_a C_{ia}} = 1 \quad (8)$$

$$R_{ia} = \frac{G\beta_a t_a}{N k_a C_{ia}}, \quad (9)$$

for the buck output of the SIDO converter

Similarly, the value of the resistor R_{ib} for the boost output of the SIDO converter can be expressed as (10).

$$R_{ib} = \frac{G\beta_b t_b}{N k_b C_{ib}}, \quad (10)$$

for the boost output of the SIDO converter

According to the operation of the charge reservation circuit, the value of the resistor R_{ia} or R_{ib} ensures that the discharging current is proportional to the load current at the buck or boost output of the SIDO converter. The value of the discharging current is expressed as Eq. 11 or 12 for the buck or boost output, respectively. Hence, it is obvious that the charge stored on internal capacitor C_{ia} or C_{ib} can effectively represent the regulated output voltage at the buck or boost output. In other words, the proposed charge reservation circuit can avoid the oscillation problem that is caused by the long charging time of capacitor C_{ia} or C_{ib} at very light loads.

$$I_{disa} = V_{EOA} \frac{N k_a C_{ia}}{G\beta_a t_a}, \quad (11)$$

for the buck output of the SIDO converter

$$I_{disb} = V_{EOB} \frac{N k_b C_{ib}}{G\beta_b t_b}, \quad (12)$$

for the boost output of the SIDO converter

3.2 Load-dependence DC-level circuit for improving the light-load efficiency

The cross regulation problem is the most important design consideration for the design of SIMO converters. The load transient of one converter needs to have little effect on the other converter. Thus, how to prevent the converters from being influenced by the cross regulation problem becomes an urgent topic. The cross regulation comes from two major scenarios. One scenario is that the inductor lacks energy due to the ineffective control of the energy storage. The other one is the inductor has no path to release the extra energy during low demand cycles. Thus, the problem of cross regulation can be simplified as how to rapidly and effectively store and release the energy in the inductor.

In order to reduce the effect of cross regulation, a load-dependence DC-level circuit is proposed to dynamically adapt the dc level of the SIDO converter to the variation of load current and the circuit is shown in Fig. 5(a). A lot of energy is needed to be stored in the inductor at heavy loads. On the other hand, a little energy is demanded at light loads. The load transient response is a continuous behavior and sensed by the voltage feedback loop. In other words, the outputs (*EA1* and *EA2*) of error amplifiers stand for the load conditions of two outputs. When the output load current changes from light to heavy, the output voltage of the error amplifier is increased

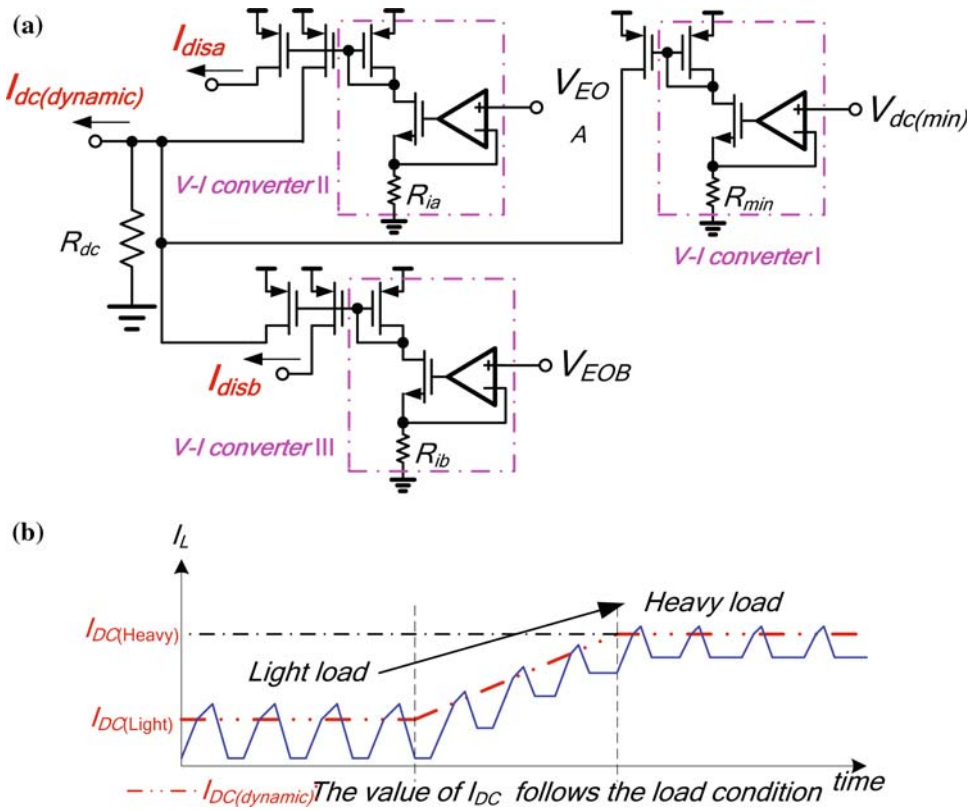

Fig. 5 (**a**) The control circuit of the dynamic dc-level adjustment. (**b**) The waveform of the dynamic inductor current is raised from low to high when load current changes from light to heavy

immediately in order to get a large duty cycle. Similarly, the output voltage of the error amplifier is decreased to minimize the duty cycle when load current steps from heavy to light. In the design of the load dependent DC-level circuit, two additional *V–I* converters (*V–I* convert II and III in Fig. 5(a)) are used to convert the two voltage signals V_{EOA} and V_{EOB} to current signals for dynamically adjusting DC level. The DC level stands for the pre-charged energy in the inductor to react to the large load variations. It is obvious that a large value of DC level means an inefficient power conversion at light loads. Contrarily, a small value of DC level may have the problem that the converter doesn't have the capability to handle the large load current step. It is important to define upper and lower bound limitations to prevent the SIDO converter from over or under storing energy. The lower limitation current is defined by the *V–I* converter I in Fig. 5(a). The value of $V_{dc(min)}$ defines the minimum dc level. On the other hand, the upper limitation circuit is simply implemented by a diode clamp in order to prevent the transient spike occurred at the node of the $I_{dc(dynamic)}$. The load-dependent DC level control not only can effectively raise the power conversion efficiency at light loads but also can effectively handle much higher load current conditions. The adjustment of the dynamic inductor current is shown in Fig. 5(b) when the load current changes.

3.3 Pulse width modulation control logic generator and mode switch controller for the operation hysteresis mode

The pulse width modulation (PWM) control logic generator in Fig. 6(a) can generate control signals BV_{S1}, BV_{S2}, BV_{SA3}, and BV_{SB3} according to the signals V_{clk}, V_{CM1}, V_{CM2}, and V_{CM3}, which are the clock signal and the output signals of the three comparators. These signals BV_{S1}, BV_{S2}, BV_{SA3}, and BV_{SB3} are converted by the buffer shown in Fig. 6(b) to signals V_{S1}, V_{S2}, V_{SA3}, and V_{SB3}, which are used to control the switches M_{VS1}, M_{VS2}, M_{VSA3}, and M_{VSB3}. The buffer contains a level shifter to raise the voltage to a higher voltage level to reduce the value of the on-resistance and to have ability to fully turn off the switch. Besides, the buffer also contains a non-overlapping mechanism to avoid the shoot-through current from the supply voltage to ground.

The switching cycle is decided by the clock generator shown in Fig. 6(c). The charging or discharging current is defined by the current I_{BIASH} or I_{BIASL}, respectively. The ratio of the current I_{BIASH} to the current I_{BIASL} is 1:9. Thus, the clock frequency is decided by (13).

$$f_{osc} = \frac{0.9I_{BIASH}}{(V_{refH} - V_{refL})C_{osc}} \tag{13}$$

At the beginning of the clock, the value of BV_{S2} is set to high for storing the predefined dc inductor current. The

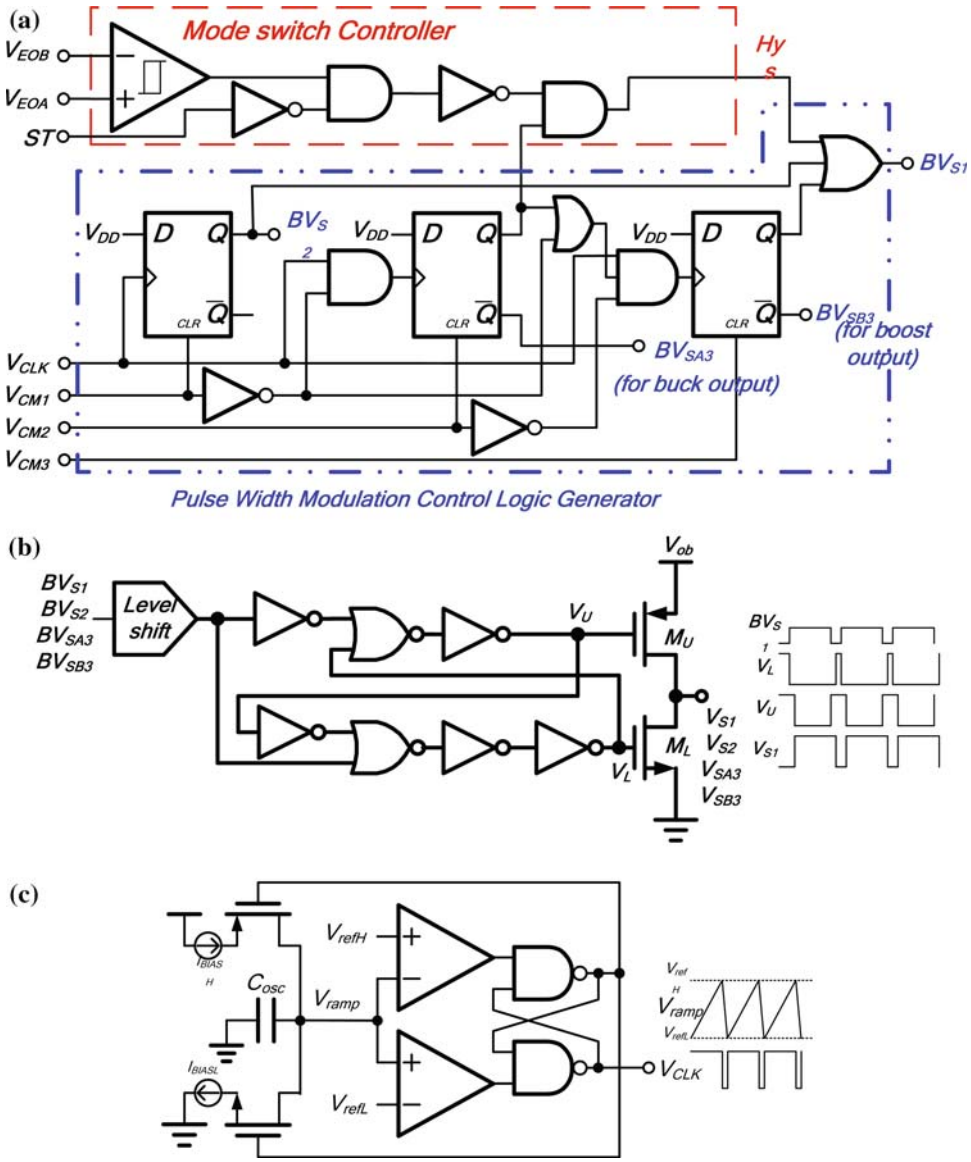

Fig. 6 (**a**) The pulse width modulation control logic generator and the mode switch controller. (**b**) The buffer contains a level shifter and a non-overlapping circuit. (**c**) The clock generator

value of the signal V_{CM1} is set to high at the beginning of every cycle. Once the value of V_{RS} is larger than that of $V_{dc(dynamic)}$ in Fig. 3, the value of V_{CM1} is set low by the comparator *CMP1*. At this time, the inductor current is raised to the dynamic dc current level and the stored energy is ready to be delivered to the two outputs. The signals V_{CM2} and V_{CM3} are used to control the load conditions of the buck and boost outputs, respectively. At first, the signal V_{CM2} is set to high to start the buck period when the signal V_{CM1} is set to low. The value of BV_{SA3} is set to low at the same time for storing energy to the buck output. The signal V_{CM2} at the output of the comparator *CMP2* changes from high to low when the buck output gets enough energy from the inductor. Contemporaneously, the signal V_{CM3} is set to high to start the boost period. The value of BV_{SB3} is set to low at the same time for storing energy to the buck output. The signal V_{CM3} at the output of the comparator *CMP3* changes from high to low when the boost output gets enough energy from the inductor. Then, the period of freewheel stage starts and the energy is reserved in the inductor. The longer the period of freewheel stage is, the lower the conversion efficiency is. Fortunately, owing to the adjustment of the dc level of the inductor current, the power loss can be reduced at light loads.

If the power dissipation of the boost output is larger than that of the buck output, the inductor current can be pulled down by the boost output. Since there is only one path for the inductor current to be pulled down, the load condition of the boost output must be larger than that of the buck output. In order to prevent the current from accumulating

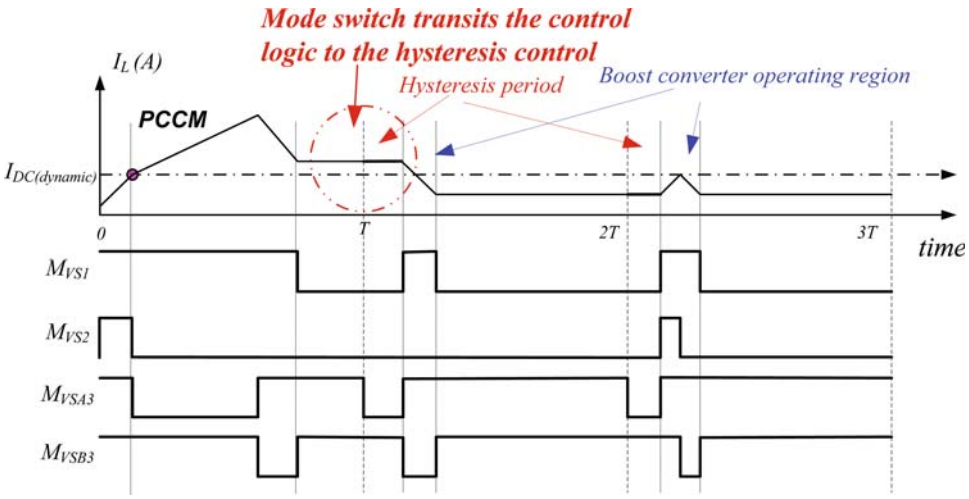

Fig. 7 Timing diagram of the proposed dynamic DC-level PCCM control with hysteresis mode operation

in the inductor when the power dissipation of the buck output is larger than that of the boost output, a mode switch controller shown in Fig. 6(a) is used to decide the operation mode of the SIDO converter. The SIDO converter operates in the dynamic dc-level PCCM control when the power dissipation of the buck output is smaller than that of the boost output. On the other hand, the mode switch controller has to switch the dynamic dc-level PCCM control to the hysteresis control mode when the load condition of the buck converter is larger than that of the boost converter. When the value of V_{EOA} is larger than that of V_{EOB} after the soft-start period ($ST = 0$), the signal Hys is set to low to switch the mode to the hysteresis control mode. The energy flows from power source via switches M_{VS1} and M_{VSA3} in Fig. 3 to the buck output. It means that no current flowing into the inductor to incur the accumulation problem. Thus, the instability scenario in Fig. 2 is eliminated. The waveform of the inductor current is shown in Fig. 7. When the converter enters the hysteresis operation mode, the buck output gets energy via M_{VS1} and M_{VSA3} and the boost output gets energy from the inductor. There is a trade-off between system stability and output ripple of the buck output. During the hysteresis operation, the output ripple of the buck output is larger than that at the normal dynamic dc-level PCCM operation. However, the inductor current will not be increased to make the system unstable. The inductor current is maintained below the value of the predefined dc-level. In other words, the cross regulation is alleviated compared to the previous designs, which may have the oscillation problem due to the accumulation of energy in the inductor.

The hysteresis operation can be terminated and the SIDO converter is set back to the dynamic dc-level PCCM control when the power dissipation of the buck converter is smaller than that of the boost converter. Here, a hysteresis window is added to the hysteresis operation to prevent the system from oscillating between two operation modes. As we know, the charging path of the buck converter is isolated from that of the boost converter. In other words, the charge accumulation and the cross regulation have been eliminated. A hysteresis operation is an important operation mode for a SIDO converter with minimized the number of switches without any oscillation problems.

3.4 The power-on sequence of the proposed SIDO converter

The feedback signals V_{FBA} and V_{FBB} are used to compare with the reference voltage V_{REF} to decide the error signals V_{EOA} and V_{EOB}, respectively. Then, the error signals V_{EOA} and V_{EOB} are used to decide the duties of the buck and boost outputs, respectively. However, during the power-on period, the two outputs are close to zero voltage. Thus, the duties of the two outputs are near to the maximum duties. The two outputs have the overshoot problem due to the inrush current. To avoid the large start up current, the soft start circuit shown in Fig. 8 is proposed to avoid the inrush current. After the soft start period, the duty is controlled by

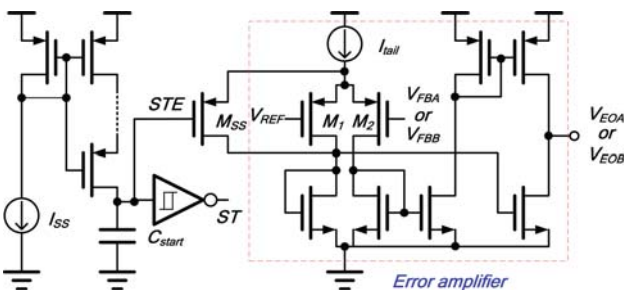

Fig. 8 The soft-start circuit for the proposed SIDO converter

feedback closed loop and the converter enters the normal dynamic dc-level PCCM control.

At the beginning of the power-on period, the voltage on the capacitor C_{start} is 0 V. The values of *ST* and *STE* are high and low, respectively. Since the signal *STE* is low and connected to the gate of the transistor M_{SS} in Fig. 8, transistor M_{SS} dominates one branch of the error amplifier. Transistor M_1 controlled by the reference voltage V_{REF} has little control ability compared to transistor M_{SS}. The small biasing current I_{SS} is used to slowly charging the voltage of the C_{start}, which decides the values of *ST* and *STE*. When the value of *STE* approaches to the reference voltage V_{REF}, the system begins to be switched to the normal dynamic dc-level PCCM operation. Finally, the values of *ST* and *STE* are low and high, respectively.

4 Measurement results

The proposed SIDO converter with dynamic-PCCM technique was fabricated in TSMC 0.35 μm 2P4 M process. The micrograph of SIDO converter is shown in Fig. 9. The proposed SIDO converter provides one buck output of 1.2 V and one boost output of 2.4 V.

The cross regulation of the two converters are estimated by stepping the load current with rising time and falling time of 1 μs changes from 0 to 50 mA, or vice versa. The waveforms of the estimation in the cross regulation are shown in Fig. 10. The cross regulation of our proposed SIDO converter is minimized because of dynamic-PCCM technique. The cross regulation can be alleviated to be smaller than 3 mV. This is owing to the effective control the energy in the inductor. Besides, the oscillation appeared in literature [1] can be eliminated in our proposed hysteresis operation, which is shown in Fig. 11. It is obvious to find that the output ripples are

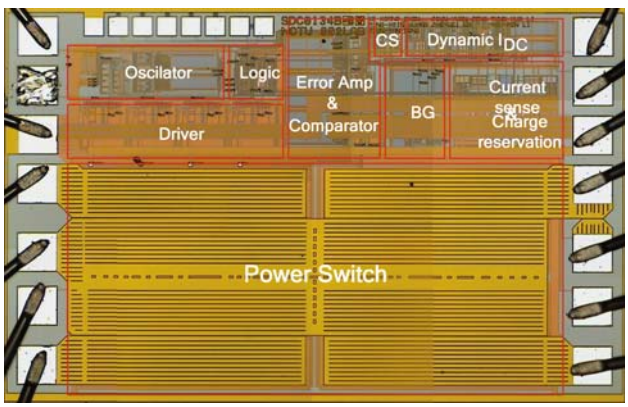

Fig. 9 Micrograph of the proposed SIDO converter and the chip size is 1800*1500 μm^2

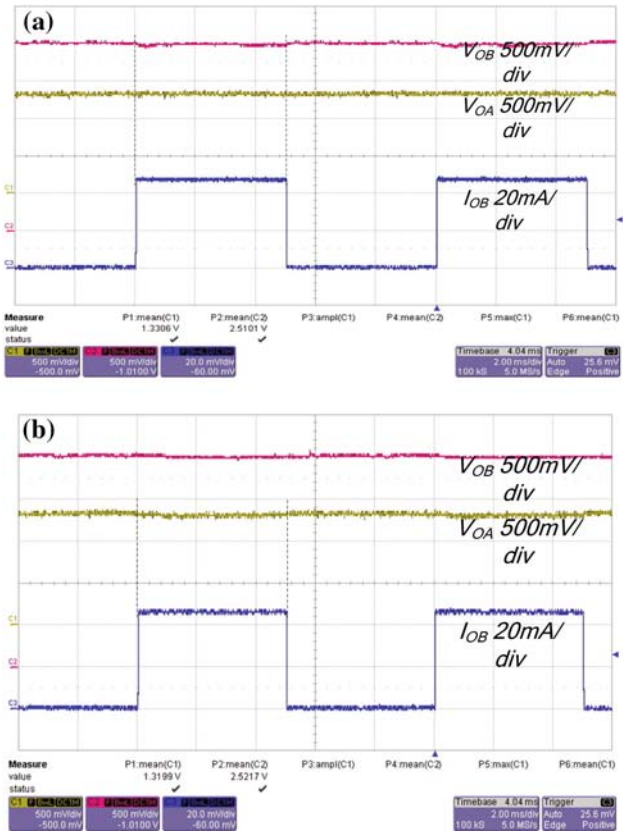

Fig. 10 Cross regulation estimation. (**a**) The cross regulation of the boost output when the load current steps from 0 to 50 mA and back to 0 mA at the buck output ($@I_{OB} = 10$ mA). (**b**) The cross regulation of the buck output when the load current steps from 0 to 50 mA and back to 0 mA at the boost output ($@I_{OA} = 10$ mA)

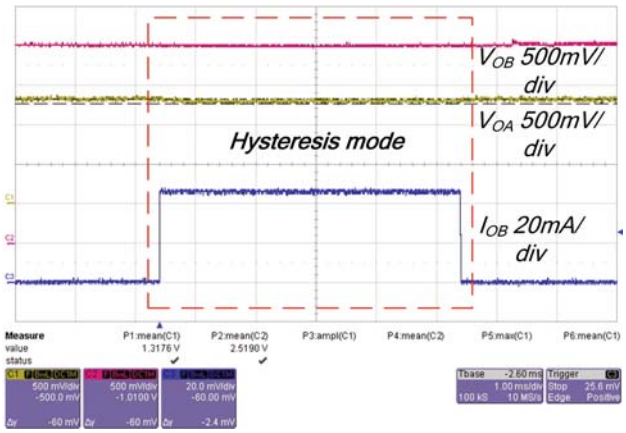

Fig. 11 The enlarged waveform of the buck output at the hysteresis operation when the load of buck output is larger than that of the boost output ($I_{OB} = 10$ mA)

larger than those at the normal operation of dynamic DC level. This is a trade-off between the efficiency and system stability. The oscillation problem appeared in the previous design [1] is really eliminated. It means that the

Table 1 Summary of the performance

Supply voltage	1.8–2.0 V @ Temperature = −10 ∼ 120°C	
Inductor	10 μH (±10%)	
Oscillator frequency	300 kHz	
Process	TSMC 0.35 μm CMOS	
Chip area	1800*1500 μm^2	
Converters	Buck	Boost
Output voltage	$V_{oa} = 1.2$ V	$V_{ob} = 2.4$ V
Output ripples	15 mV @ $I_{La} = 50$ mA	5 mV @ $I_{Lb} = 50$ mA
Filter capacitor	10 μF w/i low ESR (smaller than 50 mΩ)	10 μF w/i low ESR (smaller than 50 mΩ)
Load regulation	0.12 V/A	0.2 V/A
Line regulation	6.5 mV	7.3 mV
Cross regulation estimation (a)	(from 0 to 50 mA)/ (from 50 to 0 mA)	3 mV/3 mV
Cross regulation estimation (b)	3 mV/3 mV	(from 0 to 50 mA)/ (from 50 to 0 mA)

proposed SIDO converter can operate at any load conditions whether the load of the buck output is larger than that of the boost output or not.

The performance is summarized in Table 1. Furthermore, the power conversion efficiency is shown in Fig. 12. The light load efficiency is improved from 65% of conventional PCCM to about 85% due to low dc-level inductor current in the dynamic dc-level technique.

5 Conclusion

This paper proposes a compact size and high efficiency single-inductor dual-output (SIDO) DC–DC converter for supplying a SoC system. The new proposed SIDO with minimized switch transistors really utilizes only a single inductor to provide one buck and one boost outputs. The energy stored in the inductor can be effectively delivered to the buck and the boost outputs without stability problems. In other words, the proposed hysteresis mode operation provides a method to solve the oscillation that may exist in many SIMO converters. Importantly, to implement DC–DC converters with minimized the number of components only occupies a small footprint area for a SoC system. Thus, the proposed SIDO DC–DC converter not only provides one buck and one boost outputs but also has minimized cross regulation. Furthermore, owing to dynamically adjusting dc current level like CCM operation, the SIDO DC–DC converter achieves high conversion efficiency at light loads. Experimental results show a high efficiency from 85% at light loads condition to 94% at heavy loads.

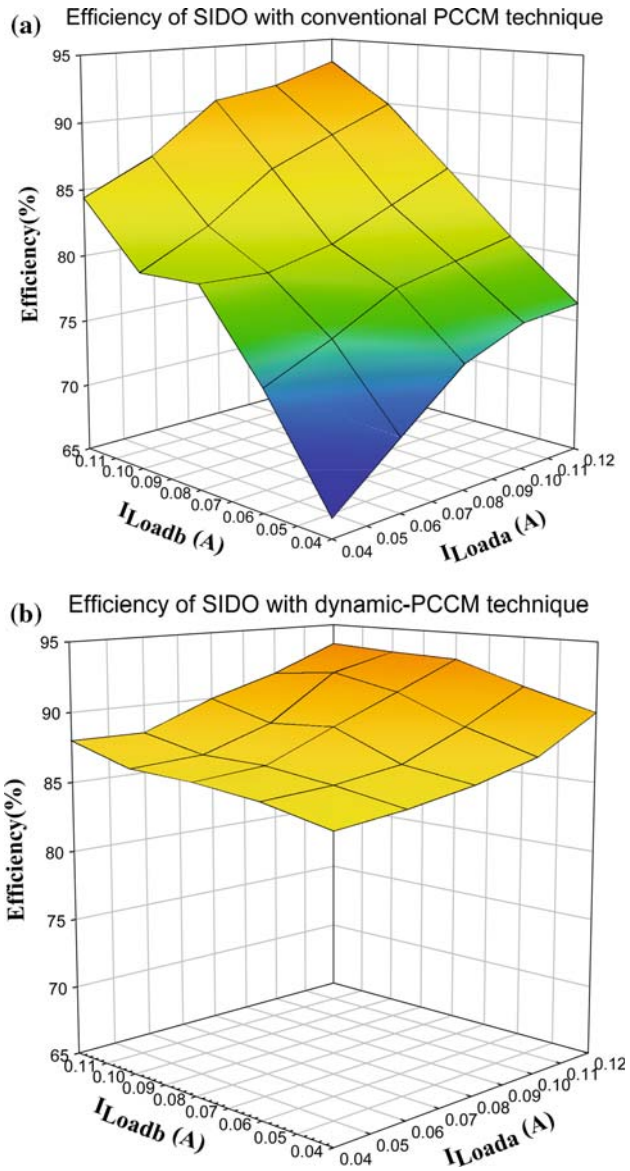

Fig. 12 Power conversion efficiency. (**a**) SIDO with conventional PCCM technique. (**b**) SIDO with dynamic-PCCM technique

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