SCR Device With Double-Triggered Technique for On-Chip ESD Protection in Sub-Quarter-Micron Silicided CMOS Processes

Ming-Dou Ker, *Senior Member, IEEE,* and Kuo-Chun Hsu, *Student Member, IEEE*

***Abstract*—Turn-on efficiency is the main concern for silicon-controlled rectifier (SCR) devices used as on-chip electrostatic discharge (ESD) protection circuit, especially in deep sub-quarter-micron CMOS processes with much thinner gate oxide. A novel double-triggered technique is proposed to speed up the turn-on speed of SCR devices for using in on-chip ESD protection circuit to effectively protect the much thinner gate oxide in sub-quarter-micron CMOS processes. From the experimental results, the switching voltage and turn-on time of such double-triggered SCR (DT_SCR) device has been confirmed to be significantly reduced by this double-triggered technique.**

***Index Terms*—Double-triggered technique, electrostatic discharge (ESD), ESD protection circuit, silicon-controlled rectifier (SCR).**

I. Introduction

With THE process evolution, the gate-oxide thickness has been scaled down to increase circuit operating speed under lower voltage supply. For oxide reliability concerns, the normal operating voltage has been limited to some voltage level for each CMOS technology, but the electrostatic discharge (ESD) event often has a much higher overstress voltage, which can burn out the junction or rupture the gate oxide. Therefore, in order to effectively protect the thinner gate oxide from ESD stresses, on-chip ESD protection circuit must have lower clamping voltage and faster turn-on speed. Among the various ESD protection devices, the silicon-controlled rectifier (SCR) has the lowest holding voltage ($V_{\rm hold}$, about $\sim$1 V in general CMOS processes). SCR is composed of parasitic n-p-n and p-n-p transistors in CMOS process, and its turn-on mechanism is essentially a current triggering event. With the best area-efficient ESD robustness, SCR had been used as on-chip ESD protection for a long time [1], [2], but SCR has some drawbacks in CMOS IC applications, such as higher switching voltage ($V_{\rm t1}$) and latchup issue [3]–[5]. Some reports have presented solutions to overcome these issues [6]–[8].

In this paper, the novel double-triggered SCR (DT_SCR) device is proposed and verified in a 0.25-μm salicided CMOS process. The purpose of the double-triggered technique is to reduce the $V_{\rm t1}$ and to enhance the turn-on speed of the SCR device. The DT_SCR device is designed to be triggered on without involving the junction avalanche breakdown mechanism. Therefore, the much thinner gate oxide in sub-quarter-micron CMOS processes can be effectively protected by such DT_SCR device. With a suitable ESD-detection circuit, the DT_SCR device is designed to be kept off during normal circuit operating conditions, and to be quickly triggered on during ESD-zapping conditions.

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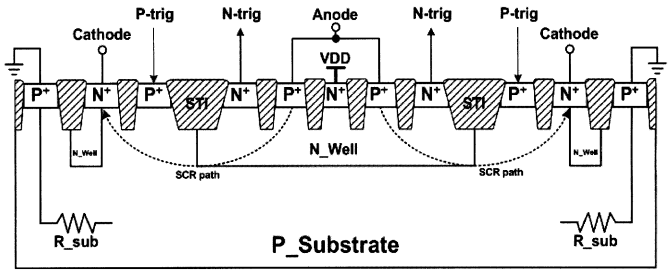

Fig. 1. Device structure of the DT_SCR device.

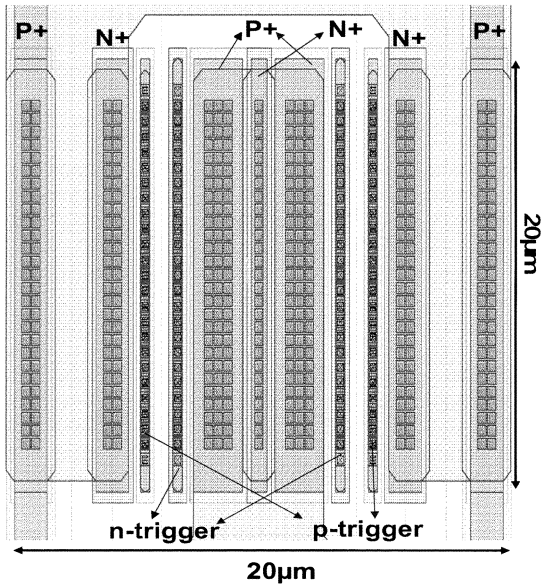

Fig. 2. Layout top view of the DT_SCR device.

II. Double-Triggered SCR Device

A. Device Structure

The proposed DT_SCR device is shown in Fig. 1. The ESD current path in the DT_SCR device is indicated by the dashed lines shown in Fig. 1. As compared with the traditional lateral

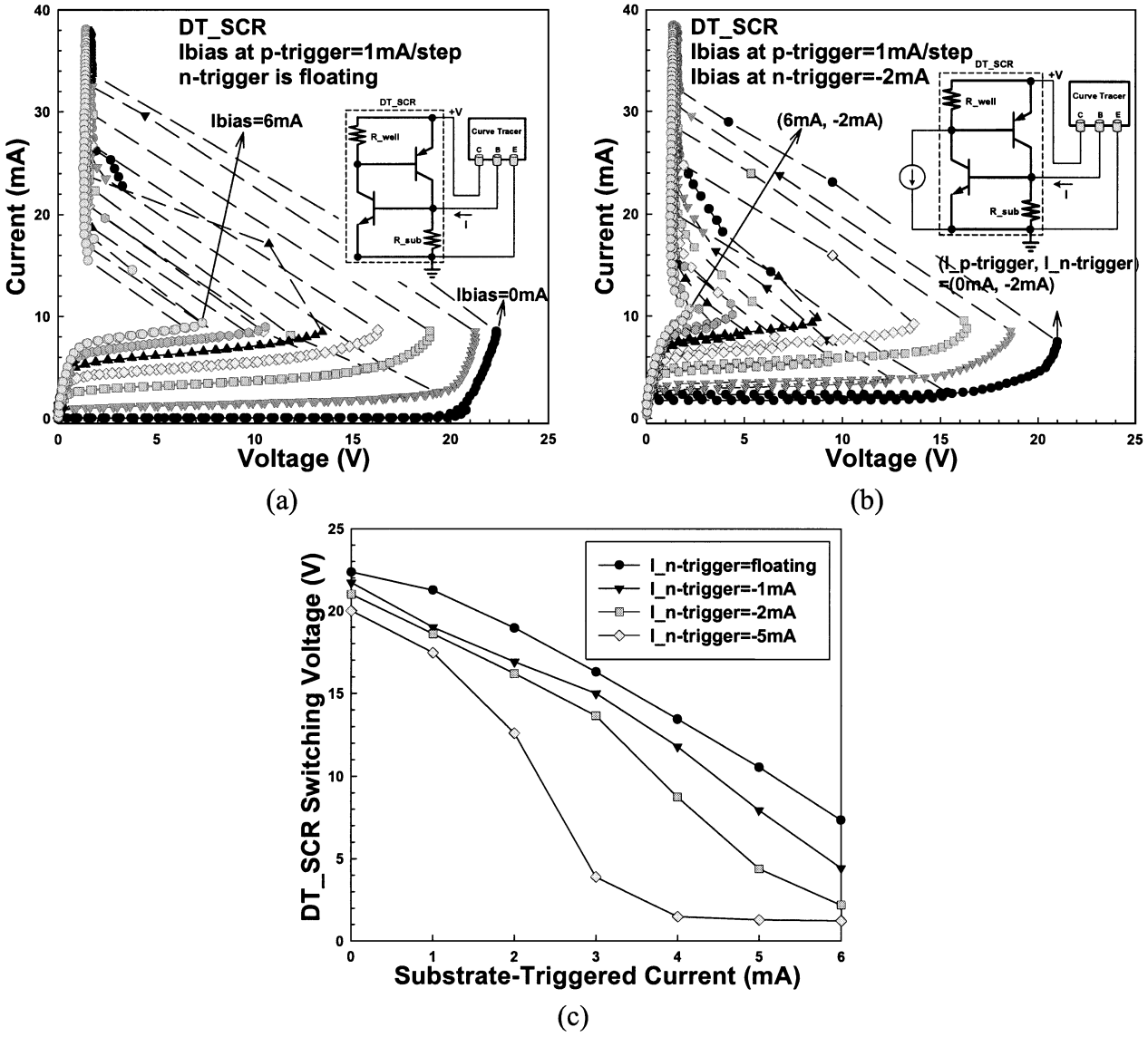

Fig. 3. (a) Measurement setup and measured dc I–V curves of DT_SCR under different substrate-triggered currents but no n-well triggered current. (b) Measured dc I–V curves of DT_SCR under different substrate-triggered currents and the additional n-well triggered current of -2 mA. (c) Dependence of switching voltage of DT_SCR on substrate-triggered current under different n-well triggered currents.

SCR device structure [1], extra p+ and n+ diffusions are inserted into the p-substrate and n-well, respectively, of the DT_SCR device structure. The inserted p+ and n+ diffusions are connected out as the p-trigger and n-trigger nodes of the DT_SCR device. When a trigger current is applied to p-trigger node, the n-p-n bipolar transistor in the SCR structure is active, and the collector current of the n-p-n is generated to bias the p-n-p bipolar transistor. When the p-n-p transistor is turned on, the collector current of the p-n-p is generated to further bias the n-p-n transistor. The positive feedback regeneration mechanism [9] of latchup is initiated by the substrate-triggered current in the SCR structure instead of the avalanche breakdown mechanism, so the DT_SCR will be triggered into its latching state. When a trigger current is drawn out from the n-trigger node, the DT_SCR will be also triggered on into its latching state through the positive feedback regeneration mechanism. In this work, two trigger currents can be synchronously applied to trigger on the DT_SCR device.

B. Device Characteristics

The fully silicided DT_SCR device in Fig. 1 has been fabricated in a 0.25-μm salicided CMOS process. The layout top view of the DT_SCR device is shown in Fig. 2. The active area of the DT_SCR device is 20 μm $\times$ 20 μm. Fig. 3(a) shows the measured dc I–V curves of the DT_SCR, which are measured with different substrate-triggered currents into the p-trigger node of the DT_SCR but no n-well triggered current. The measurement setup is shown as the inset in Fig. 3(a). The V_{t1} of the DT_SCR is reduced with the increase of the substrate-triggered current. When the triggered current at the p-trigger node is increased from 0 to 6 mA, the V_{t1} of the DT_SCR is reduced from $\sim$22 to $\sim$7 V. If the triggered current is continually increased, the V_{t1} will be nearly reduced to its holding voltage. Moreover, in Fig. 3(b), the double-triggered solution is used to further reduce the V_{t1} to a relatively lower voltage level. Based on the similar measurement of Fig. 3(a),

an extra n-well current of 2 mA is drawn out from the n-trigger node of the DT_SCR, and the measured I–V curves under different substrate-triggered currents into the p-trigger node are shown in Fig. 3(b). The double-triggered measurement setup is also indicated in the inset of Fig. 3(b). The V_{t1} of the DT_SCR under the substrate-triggered current of 6 mA is further reduced from $\sim$7 to only $\sim$2 V when the n-well triggered current is increased from 0 to -2 mA. (The negative sign on the current in this paper is used to represent the current flowing out from the node.) The dependence of the switching voltage of the DT_SCR device on the substrate-triggered current under different n-well triggered currents is depicted in Fig. 3(c). The V_{t1} of the DT_SCR device can be nearly reduced to the holding voltage ($\sim$1.5 V) more efficiently when both the substrate-triggered and n-well triggered currents are applied to the DT_SCR device. These results have proven that the V_{t1} of the DT_SCR device can be significantly reduced by the proposed double-triggered technique.

The measured dc I–V curves of the DT_SCR under a substrate-triggered current of 2 mA into the p-trigger node and different n-well triggered currents out from the n-trigger node are shown in Fig. 4(a). The measurement setup is also illustrated as the inset in Fig. 4(a). When the n-well triggered current is increased from 0 to -3 mA, the V_{t1} of the DT_SCR under the substrate-triggered current of 2 mA is significantly reduced from $\sim$15 to only $\sim$1.5 V, which is near to its holding voltage. The dependence of V_{t1} of the DT_SCR on the n-well triggered current under different substrate-triggered currents is shown in Fig. 4(b). The V_{t1} of the DT_SCR under the n-well triggered current of -3 mA is further reduced from $\sim$21 to $\sim$1.5 V, when the substrate-triggered current is increased from 0 to 2 mA. The characteristics of the DT_SCR in Fig. 4(b) are similar to those in Fig. 3(c). In the p-type substrate, because the current gain of the n-p-n transistor is higher than that of the p-n-p transistor, the substrate-triggered current (used to trigger the n-p-n transistor in the DT_SCR device) seems to have more significant effect than the n-well triggered current (used to trigger the p-n-p transistor in the DT_SCR device) to reduce the V_{t1} of the DT_SCR and to quickly trigger on the DT_SCR [10]. The ESD protection device with lower switching voltage can be turned on more quickly to protect the internal circuits from ESD damage.

Another issue of using the SCR device as the ESD protection device is the transient-induced latchup concern when the CMOS IC is operating under normal circuit operations. The total holding voltage of the ESD protection circuit with SCR devices must be designed to be greater than the maximum voltage level of V_{DD} during normal circuit operating conditions to avoid the latchup issue. This can be achieved by stacking the DT_SCR devices in the ESD protection circuits. Fig. 5 shows the dependence of the total holding voltage of stacked DT_SCR devices on the temperature under different numbers of stacked DT_SCR devices. The measurement setup to measure the I–V curves of stacked DT_SCR devices is depicted in Fig. 5(a). The I–V curves of two (three) DT_SCR devices in stacked configuration, which is marked as 2DT_SCR (3DT_SCR), under different temperatures are measured in Fig. 5(b) [Fig. 5(c)]. The insets in Fig. 5(b) and (c) are the enlarged views around the holding points. The total holding voltage has some degradation when the temperature is increased, because the current gains β

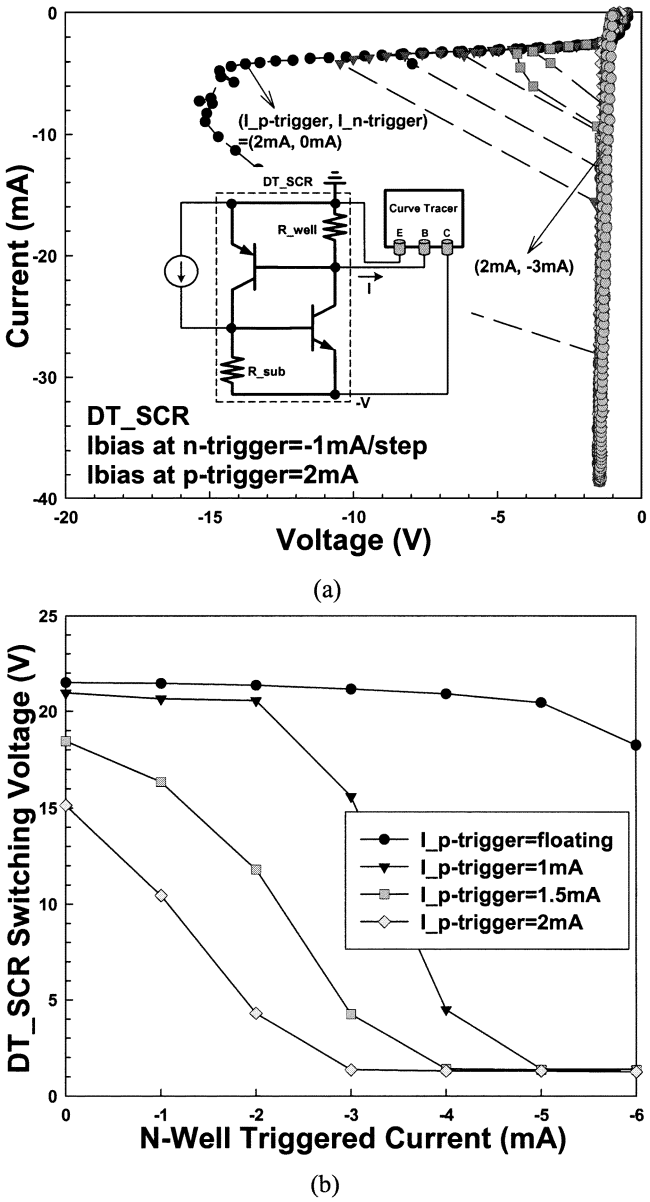

Fig. 4. (a) Measurement setup and measured dc I–V curves of DT_SCR under different n-trigger currents and the substrate-triggered current of 2 mA. (b) Dependence of switching voltage of DT_SCR on the n-well triggered current under different substrate-triggered currents.

of the parasitic bipolar transistors in the SCR device are increased with the increase of temperature. The holding voltages of 1DT_SCR, for example, are 1.4, 1.24, and 1.18 V under the temperatures of 25 °C, 75 °C, and 125 °C, respectively. The total holding voltage, however, can be still raised by increasing the number of the stacked DT_SCR devices. The holding voltages of 1DT_SCR, 2DT_SCR, and 3DT_SCR at the temperature of 125 °C are 1.18, 2.5, and 3.9 V, respectively. The dependence of the holding voltage on temperature in the stacked DT_SCR devices is compared in Fig. 5(d). Although the DT_SCR devices in stacked configurations have increased total switching voltage, such stacked DT_SCR devices can still be quickly triggered on to provide effective ESD protection when the double-triggered technique is synchronously applied to all stacked DT_SCR devices.

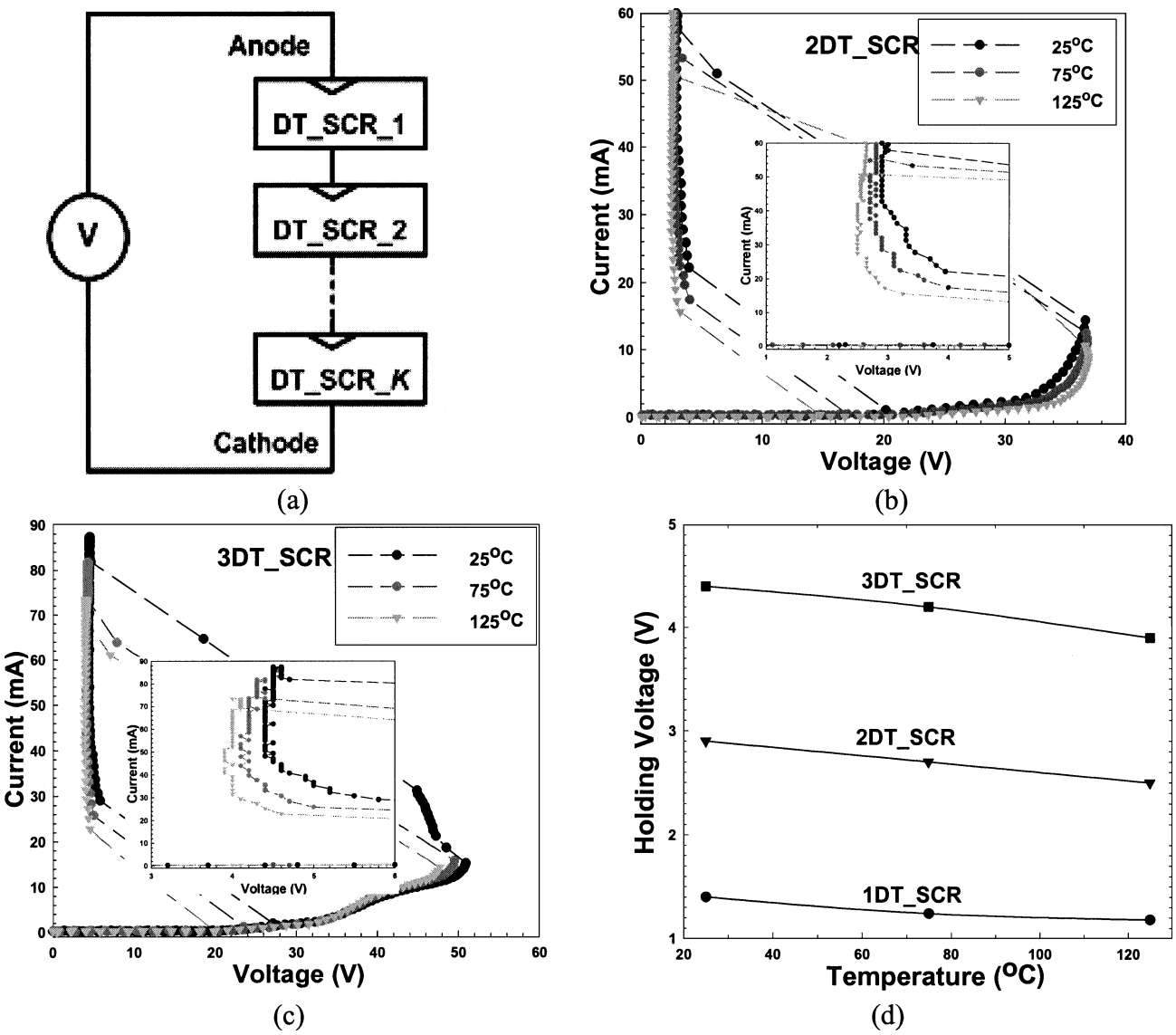

Fig. 5. Temperature dependence on the total holding voltage of stacked DT_SCR devices with different stacked numbers. (a) Experimental measurement setup. (b) Measured I–V curves of two DT_SCR devices in stacked configuration (2DT_SCR). (c) Measured I–V curves of three DT_SCR devices in stacked configuration (3DT_SCR). (d) Relation between holding voltage and temperature under different numbers of stacked DT_SCR devices.

C. Turn-On Speed

From the measured dc I–V curves of the DT_SCR, it has been verified that the $V_{\rm t1}$ of DT_SCR can be significantly reduced by the substrate and n-well triggered currents. The turn-on time of the DT_SCR, which is defined as the time for the DT_SCR to enter into its latching state, will be verified in this section. Fig. 6(a) shows the measurement setup to find the turn-on time of DT_SCR devices with the double-triggered technique. The measured results in the time domain for the DT_SCR are shown in Fig. 6(b)–(h), where $V_{\rm anode}$, $V_{\rm p-trigger}$, and $V_{\rm n-trigger}$ are the voltage waveforms on the anode, p-trigger, and n-trigger nodes, respectively, of the DT_SCR shown in Fig. 6(a). The anode of the DT_SCR device is biased at 5 V through the resistance of 10 Ω, which is used to limit the sudden large transient current from the power supply when the DT_SCR is turned on.

The positive and negative voltage pulses with a fixed rise time (or fall time) of 10 ns, which are generated from pulse generators, are synchronously applied to the p-trigger and n-trigger nodes. The original voltage pulses generated synchronously from pulse generators are shown in Fig. 6(b). The pulse height and pulsewidth are changed in the experimental measurement to verify the required turn-on time of the DT_SCR. However, in order to avoid the loading effect of oscilloscope interfering with the accuracy of the measured waveform, only the $V_{\rm p-trigger}$ will be monitored. When a 0–1.5 V positive voltage pulse with a pulsewidth of 100 ns is applied into the p-trigger node of the DT_SCR and the n-trigger node is floating, the voltage waveform at the $V_{\rm anode}$ of the DT_SCR which is triggered into the latching state is shown in Fig. 6(c). After the triggering of 1.5-V voltage pulse at the p-trigger node, the $V_{\rm anode}$ is latched at a low voltage level of ∼2.5 V and the $V_{\rm p-trigger}$ is kept at a voltage level of 0.8 V. If the pulsewidth of 1.5-V pulse at the p-trigger node is reduced to 30 ns, the DT_SCR device cannot be triggered on by this 1.5-V voltage pulse. So, the $V_{\rm anode}$ is still kept at the same voltage level of 5 V as shown in

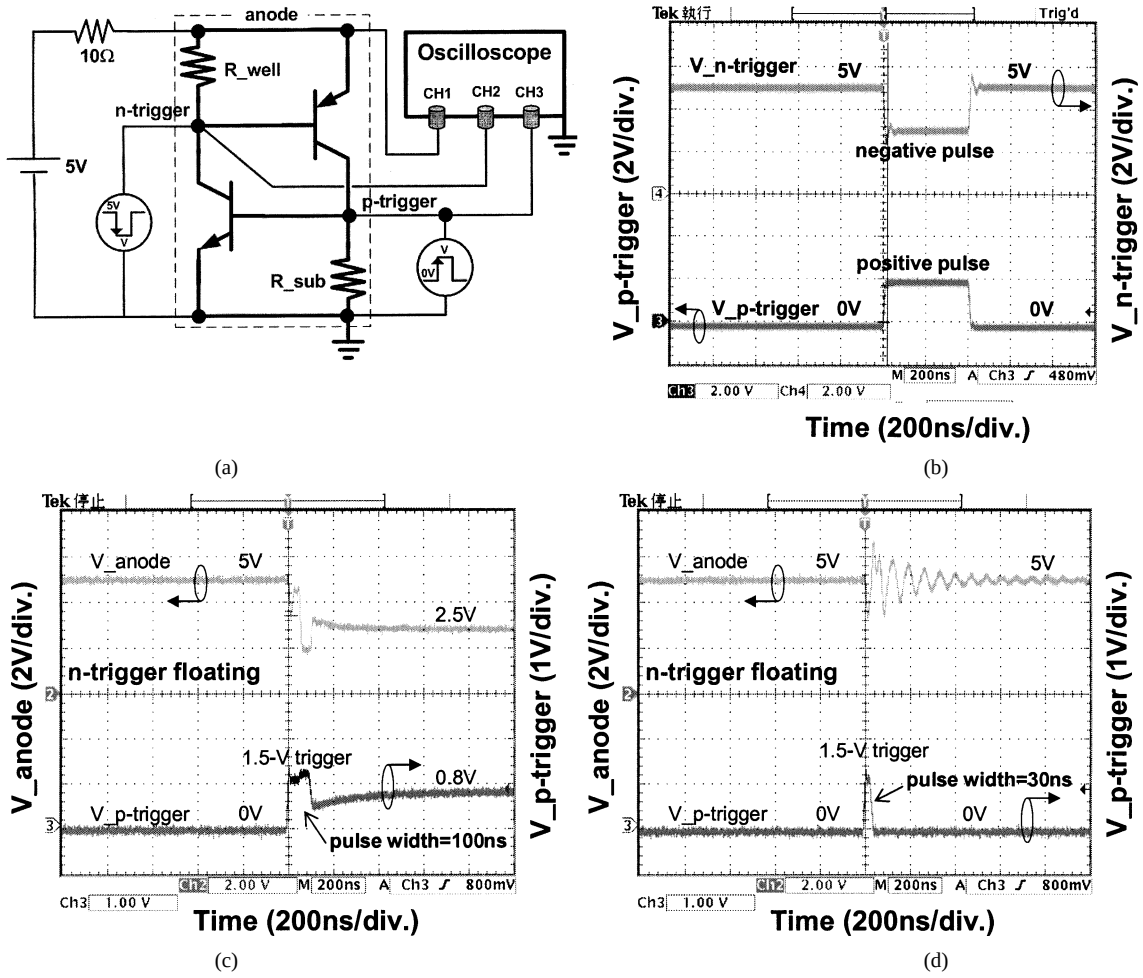

Fig. 6. Turn-on verification of DT_SCR under different voltage pulses. (a) Measurement setup. (b) Synchronous positive and negative voltage pulses. The measured voltage waveforms on the anode and p-trigger nodes of the DT_SCR device under 1.5-V positive voltage pulse with pulsewidth of (c) 100 ns and (d) 30 ns, while the n-trigger is floating.

Fig. 6(d). However, based on the same condition of Fig. 6(d), the DT_SCR device can be triggered into the latching state if an additional 5–0 V negative voltage pulse with pulsewidth of 30 ns is synchronously applied to the n-trigger node of the DT_SCR device, as shown in Fig. 6(e). So, the required pulsewidth for the DT_SCR to trigger into the latching state can be shortened if both positive and negative voltage pulses are synchronously applied to the p-trigger and n-trigger nodes.

The turn-on time for the DT_SCR into its latching state is observed by the closeup view of the $V_{\rm anode}$ voltage waveform at the falling edge. The closeup views of the $V_{\rm anode}$ at the falling edge, while the DT_SCR is synchronously triggered by the positive voltage pulse of 1.5 V at the p-trigger node and the negative voltage pulse of floating, 5–2 V, and 5–0 V at the n-trigger node, are compared in Fig. 6(f)–(h), respectively. The pulsewidths of the positive and negative voltage pulses in the measurements of Fig. 6(f)–(h) are 200 ns. The turn-on time of the DT_SCR is 37.6 ns in Fig. 6(f) if only a 1.5-V positive voltage pulse is applied to the p-trigger node. Hence, the DT_SCR cannot be triggered on if only a 1.5-V voltage pulse with a pulsewidth smaller than 37.6 ns is applied to the p-trigger node alone, which has been verified in Fig. 6(d). Moreover, from Fig. 6(f)–(h), under the positive voltage pulse of 1.5 V at the p-trigger node, the turn-on time can be reduced from 37.6 to 11.8 ns, while the absolute pulse height of the negative voltage pulse applied to the n-trigger node is increased from 0 to 5 V. These results infer that the turn-on speed of the DT_SCR device can be indeed increased by the proposed double-triggered technique. The dependence of the turn-on time of the DT_SCR on the n-well bias under different substrate bias conditions with a fixed rise time of 10 ns is summarized in Fig. 7. The turn-on time of the DT_SCR can be shortened when the substrate and/or the n-well bias voltages are increased. In addition, the dependence of the turn-on time of the DT_SCR on the rise time of the voltage pulse under different substrate bias conditions is measured and shown in Fig. 8. With the reduction of rise time of the applied voltage pulse, the turn-on time of the DT_SCR can be shortened to trace the rise time of the voltage pulse at the p-trigger node, if enough pulse voltage is applied to the trigger nodes of the DT_SCR. To enhance the turn-on speed of the DT_SCR, both the pulse height and rise time must be well designed to trigger on the DT_SCR device more efficiently.

III. Applications for On-Chip ESD Protection

A. ESD Protection Circuit for the Input/Output Pad

Based on above measured results, the ESD protection design for the input/output (I/O) pad, realized with the stacked

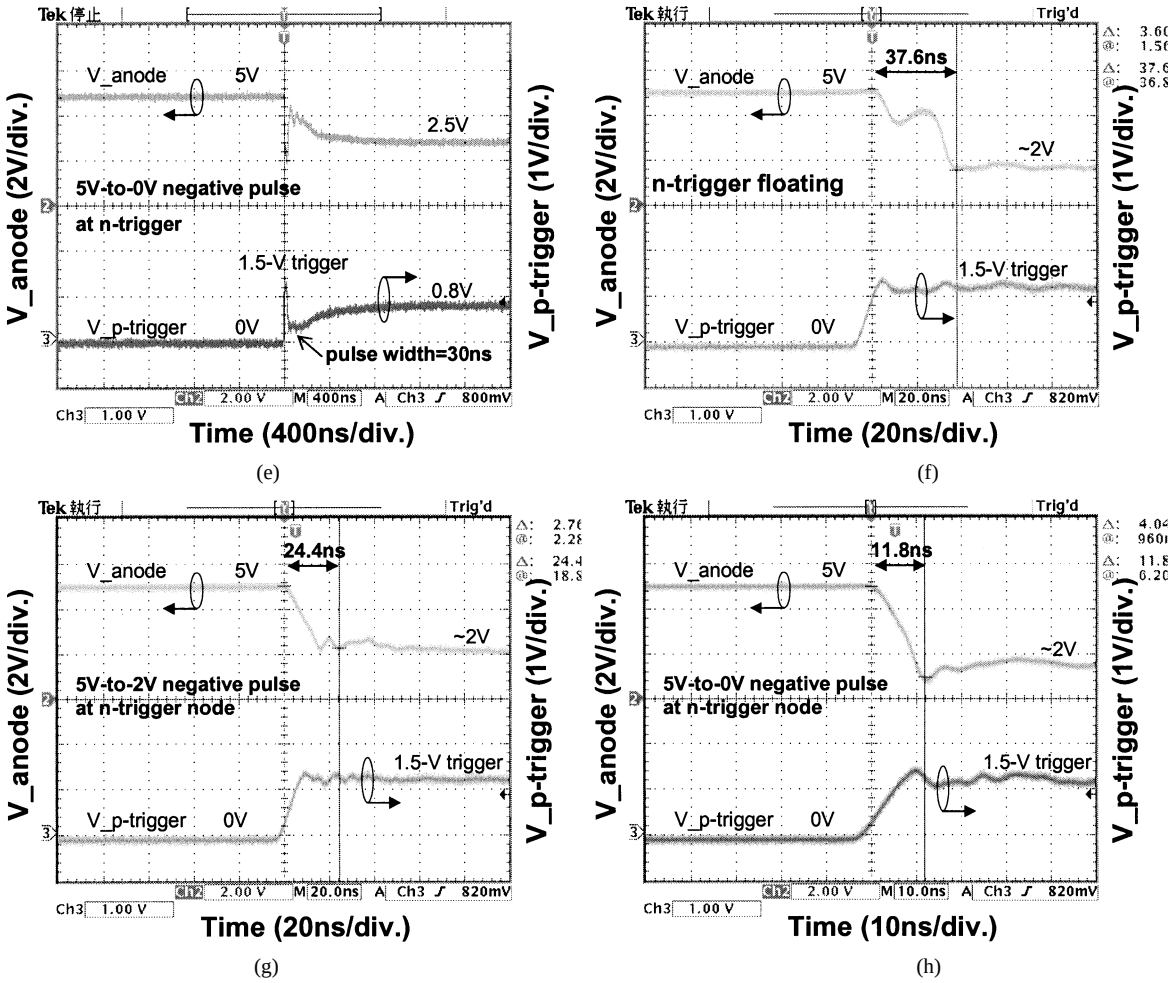

Fig. 6. *(Continued.)* Turn-on verification of DT_SCR under different voltage pulses. The measured voltage waveforms on the anode and p-trigger nodes of the DT_SCR device under 1.5-V positive voltage pulse with pulsewidth of (e) 30 ns while 5–0-V negative voltage pulse is applied to the n-trigger. The closeup views of the $V_{\rm anode}$ at the falling edge while the DT_SCR is synchronously triggering by the 1.5-V positive voltage pulse and under the negative voltage pulse of: (f) floating, (g) 5–2 V, and (h) 5–0 V.

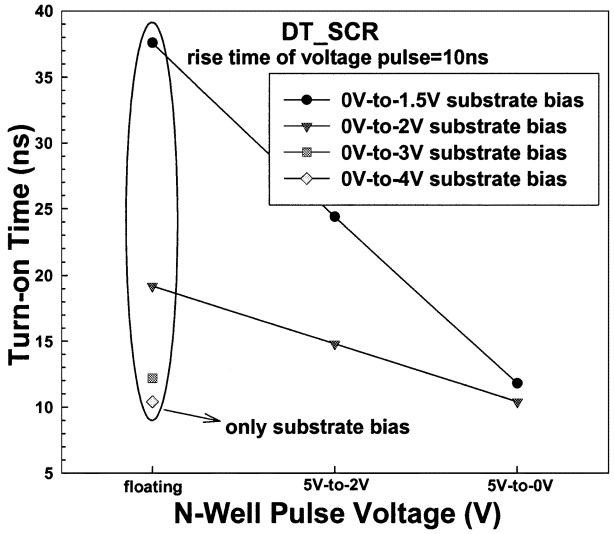

Fig. 7. Dependence of turn-on time of DT_SCR on the n-well biases under different substrate bias conditions with a fixed rise time of 10 ns.

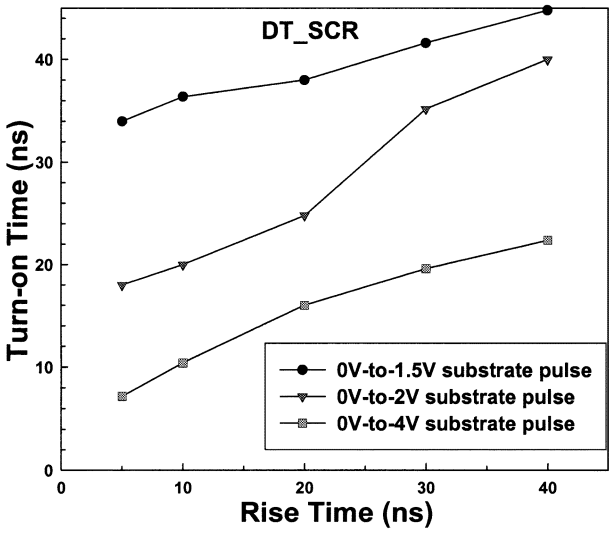

Fig. 8. Dependence of turn-on time of DT_SCR on the rise time of voltage pulse under different substrate bias conditions.

double-triggered SCR devices, is shown in Fig. 9. Two stacked DT_SCR devices are used to avoid the latchup issue during normal circuit operating conditions for 2.5-V circuit applications. The RC-delay circuit technique is used to distinguish the

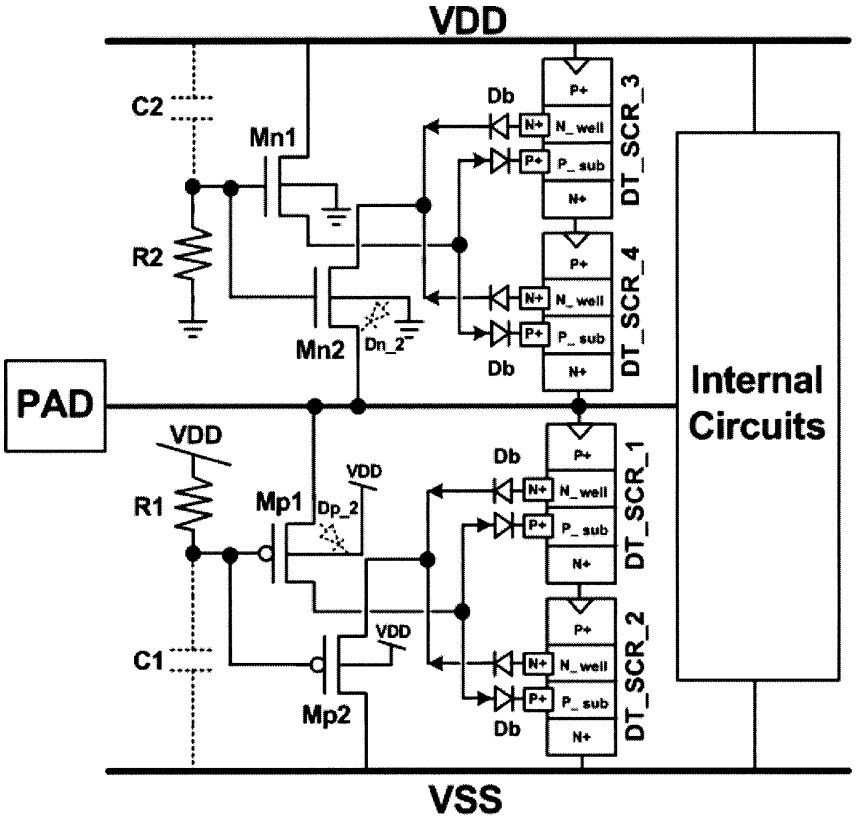

Fig. 9. ESD protection circuit for the I/O pad with the proposed DT_SCR devices in stacked configuration.

ESD-zapping conditions from the normal circuit operating conditions.

In Fig. 9, the p-trigger (n-trigger) nodes of the two stacked DT_SCR devices between the I/O pad and the V_{SS} line are connected to the drain (source) of the pMOS $\mathrm{Mp1}$ ($\mathrm{Mp2}$). The p-trigger (n-trigger) nodes of the two stacked DT_SCR devices between the I/O pad and the V_{DD} line are connected to the source (drain) of the nMOS $\mathrm{Mn1}$ ($\mathrm{Mn2}$). The gates of the pMOS $\mathrm{Mp1}$ and $\mathrm{Mp2}$ (nMOS $\mathrm{Mn1}$ and $\mathrm{Mn2}$) are connected to V_{DD} (V_{SS}) through the resistor $\mathrm{R1}$ ($\mathrm{R2}$), which is better realized by the n+ diffusion resistor for the concern of the antenna effect [11]. The resistors $\mathrm{R1}$ and $\mathrm{R2}$ can be shared by each I/O pad to save layout area in the CMOS IC. A capacitor $\mathrm{C1}$ ($\mathrm{C2}$) is placed between the gates of pMOS (nMOS) and V_{SS} (V_{DD}). These capacitors can be formed by the parasitic capacitors at the gates of the pMOS ($\mathrm{Mp1}$ and $\mathrm{Mp2}$) or nMOS ($\mathrm{Mn1}$ and $\mathrm{Mn2}$). The blocking diodes Db are used to block the current flowing through the metals connected among the trigger nodes of the stacked DT_SCR devices. Without the blocking diodes, the larger ESD current will flow out from the first p-trigger/n-trigger node of the DT_SCR into the metal connection, through the last p-trigger/n-trigger node of the DT_SCR to ground instead of the expected current path. So, without the blocking diodes, the accumulative property in holding voltage for the stacked DT_SCR configuration does not exist. Also, there are two parasitic diodes (Dp_2 and Dn_2) in this ESD protection circuit. The Dp_2 is the source-to-n-well (V_{DD}) parasitic diode in pMOS $\mathrm{Mp1}$. The Dn_2 is the source-to-p-sub (V_{SS}) parasitic diode in nMOS $\mathrm{Mn2}$.

In normal circuit operating conditions with V_{DD} and V_{SS} power supplies, the gates of $\mathrm{Mp1}$ and $\mathrm{Mp2}$ ($\mathrm{Mn1}$ and $\mathrm{Mn2}$) are biased at V_{DD} (V_{SS}). Therefore, the $\mathrm{Mp1}$, $\mathrm{Mp2}$, $\mathrm{Mn1}$, and $\mathrm{Mn2}$ are all in off state, whenever the input signal is logic high (V_{DD}) or logic low (V_{SS}). The p-trigger (n-trigger) nodes of the stacked DT_SCR devices are kept at V_{SS} (V_{DD}) through the parasitic resistors ($\mathrm{R_{well}}$ and $\mathrm{R_{sub}}$), so such stacked DT_SCR devices are guaranteed to be kept off under normal circuit operating conditions.

An ESD event zapping on a pad may have positive or negative voltage with reference to grounded V_{DD} or V_{SS}, so there are four modes of ESD stresses at each I/O pad. The four modes of ESD stresses are positive-to-V_{SS} (PS), negative-to-V_{SS} (NS), positive-to-V_{DD} (PD), and negative-to-V_{DD} (ND) modes [12], [13]. To clearly comprehend the ESD current paths under these ESD stresses, the equivalent circuit of the ESD protection circuit designed with the stacked DT_SCR devices for I/O pads is illustrated in Fig. 10. The Dn_1 is the n-well (under the n+ diffusion at the end of the SCR path) to p-sub (V_{SS}) parasitic diode in DT_SCR_4. The Dp_1 is the p+ to n-well (connected to V_{DD}) parasitic diode in the DT_SCR_1.

Under the PS-mode ESD-zapping condition (with grounded V_{SS} but floating V_{DD}), the gates of $\mathrm{Mp1}$ and $\mathrm{Mp2}$ are initially floating with a zero voltage level, thereby the $\mathrm{Mp1}$ and $\mathrm{Mp2}$ will be turned on due to the positive ESD voltage on the pad. So, the $\mathrm{Mp1}$ will conduct some initial ESD current into the p-trigger nodes of the two stacked DT_SCR devices between the I/O pads and the V_{SS} line. Synchronously, the $\mathrm{Mp2}$ will draw some initial ESD current out from the n-trigger nodes of the stacked DT_SCR devices. The V_{t1} of the two stacked DT_SCR devices will be reduced to a low voltage level, therefore, the two stacked DT_SCR devices can be quickly triggered on. So, the ESD current can be discharged from the I/O pad to the grounded

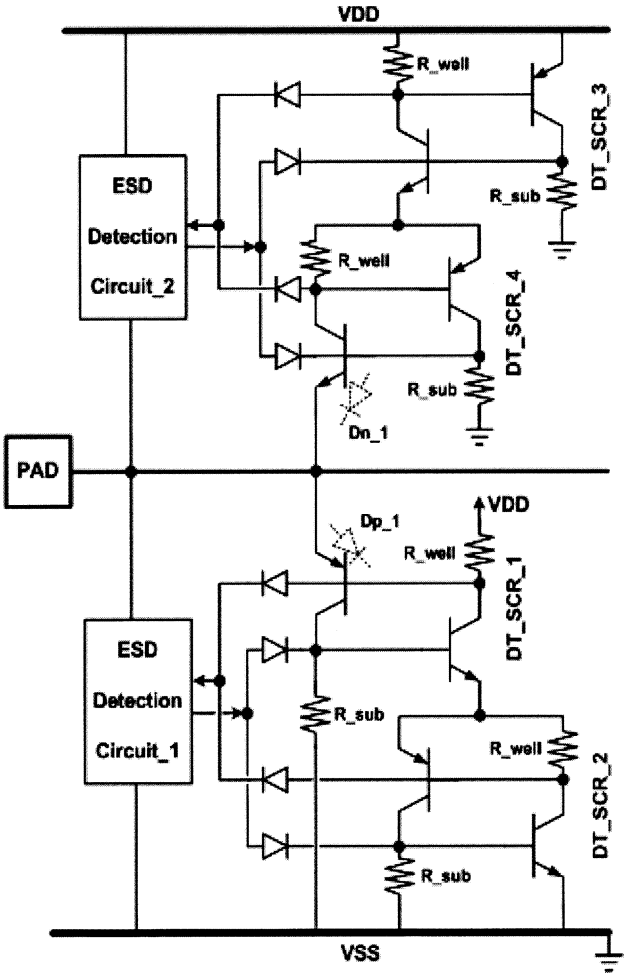

Fig. 10. Equivalent circuit of the stacked DT_SCR devices for the I/O pad.

V_{SS} through the stacked DT_SCR devices. However, the gate voltages of Mp1 and Mp2 may be charged up by the ESD energy through the forward-biased diodes Dp_1 and Dp_2, so the R1C1 time constant is designed to keep the gates of Mp1 and Mp2 at a relatively low voltage level. Then, the voltage pulses can be generated at the p-trigger and n-trigger nodes to successfully trigger on the stacked DT_SCR devices during ESD stress conditions. With the double-triggered technique, the required pulsewidth to trigger the DT_SCR into the latching state can be shortened, as shown in Fig. 6, so the RC time constant can be designed smaller to save layout area.

Under the ND-mode ESD-zapping condition (with grounded V_{DD} but floating V_{SS}), the gates of Mn1 and Mn2 are initially floating with a zero voltage level, thereby the Mn1 and Mn2 will be turned on due to the negative ESD voltage on the pad. So, the Mn1 will conduct some initial ESD current into the p-trigger nodes of the two stacked DT_SCR devices between the I/O pad and the V_{DD} line. Synchronously, the Mn2 will draw some initial ESD current out from the n-trigger nodes of the stacked DT_SCR devices. Therefore, the two stacked DT_SCR devices will be triggered on and the negative ESD current can be discharged from the I/O pad to the grounded V_{DD} through the stacked DT_SCR devices. Furthermore, the R2C2 time constant is designed to avoid the gate voltages of Mn1 and Mn2 being charged up quickly through the parasitic diodes Dn_1 and Dn_2.

Under the NS-mode (PD-mode) ESD-zapping condition, the parasitic diodes Dn_1 and Dn_2 (Dp_1 and Dp_2) will be forward biased and turned on to discharge the ESD current from the I/O pad to the grounded V_{SS} (V_{DD}). The four modes (PS, NS, PD, and ND) of ESD stresses can be clamped to a very low voltage level by the stacked DT_SCR devices or the forward-biased parasitic diodes, so the thinner gate oxide in deep sub-quarter-micron CMOS technologies can be fully protected. The diode in forward-biased condition can often sustain a very high ESD level. The ESD level of an I/O pad is dominated by the weakest ESD current path, so the experimental measurements in the following will be focused on the PS-mode or ND-mode ESD-zapping conditions.

HSPICE is used to verify the functions of ESD-detection circuits on the ESD protection circuit for the I/O pad. The transient simulation of the ESD-detection circuits in Fig. 9 under PS-mode and ND-mode ESD-zapping conditions are shown in Fig. 11(a) and (b), respectively, where R1 = R2 = 100 kΩ, C1 = C2 = 1 pF, and the device dimensions W/L of Mp1, Mp2, Mn1, and Mn2 are 10/0.25 μm, 20/0.25 μm, 10/0.25 μm, and 5/0.25 μm. Because the overdrive voltage V_{sg} of Mp2 is smaller than that of Mp1 under the same pad voltage, the Mp2 in Fig. 9 is designed with a larger channel width than that of Mp1. In Fig. 11(a), when a 0–8-V voltage pulse with a rise time of 10 ns is applied to the I/O pad of Fig. 9, the substrate-triggered and well-triggered currents can be synchronously generated by the ESD-detection circuit, which is formed by R1, C1, Mp1, and Mp2, to trigger on the stacked DT_SCR devices. In Fig. 11(b), the substrate-triggered and well-triggered currents can be also synchronously generated by the ESD-detection circuit, which is formed by R2, C2, Mn1, and Mn2, when a 0–(−8)-V negative voltage pulse with a fall time of 10 ns is applied to the I/O pad of Fig. 9. Because of the difference of the overdrive voltage between Mn1 and Mn2, the Mn1 in Fig. 9 is designed with a larger channel width than that of Mn2. From the simulation results in Fig. 11, the trigger currents at the p-trigger and n-trigger nodes can be generated almost following the voltage pulse on the I/O pad. The delay resulting from the ESD-detection circuit in Fig. 9 can be almost negligible. The triggered currents, which are the function of resistance (R1, R2), capacitance (C1, C2), and device dimensions of pMOS and nMOS devices, can be fine tuned by HSPICE simulation to fit the practical applications of different CMOS processes.

B. ESD Clamp Circuit Between the Power Rails

The stacked DT_SCR devices can also be applied to design the power-rail ESD clamp circuit. The V_{DD}-to-V_{SS} ESD clamp circuit designed with two stacked DT_SCR devices is realized in Fig. 12 for circuit applications of 2.5 V. The function of the ESD-detection circuit, which is formed with a resistor R, capacitor C, and inverters (inv_1 and inv_2), is to distinguish a V_{DD} power-on event (with a rise time in milliseconds) or ESD-stress events (with a rise time in nanoseconds) [14]. During normal V_{DD} power-on transition (from low to high), the input of inv_1 can follow up in time with the power-on V_{DD} waveform, so the output of inv_1 (or the input of inv_2) will be biased at zero. Therefore, the output of inv_2 will be kept at V_{DD}. The p-trigger/n-trigger nodes of stacked DT_SCR devices are biased

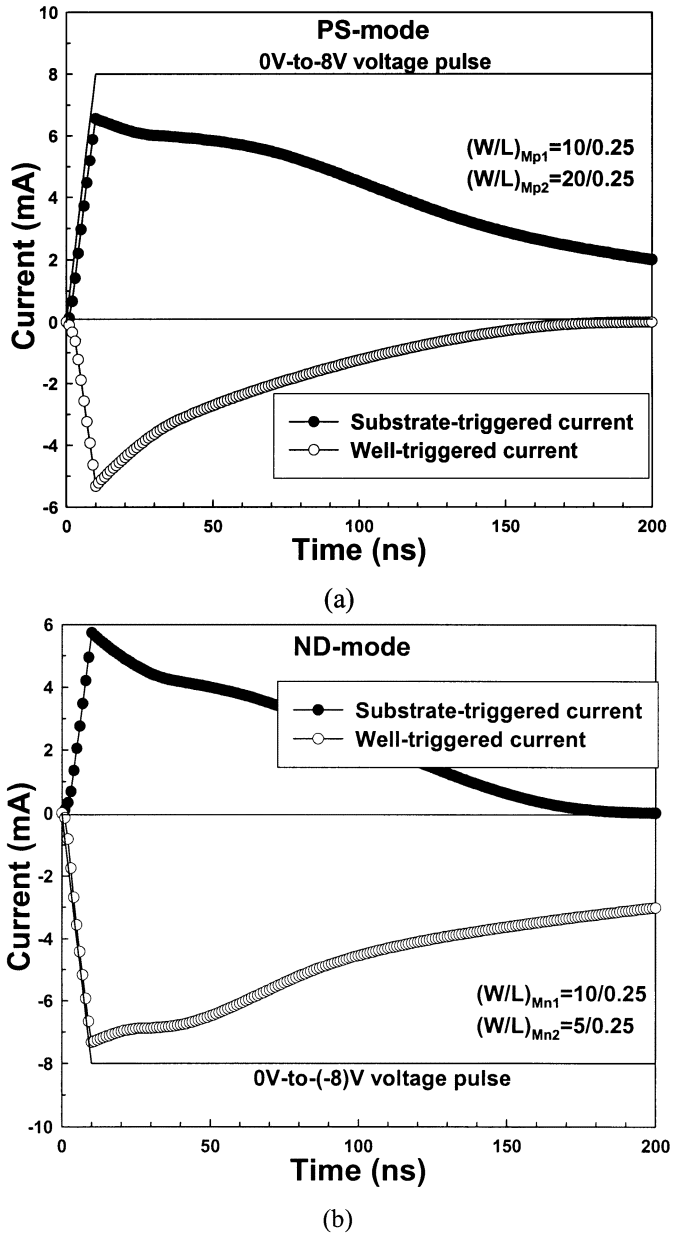

Fig. 11. HSPICE simulation. Transient simulation of the ESD-detection circuit in Fig. 9 under (a) PS-mode and (b) ND-mode ESD-zapping conditions.

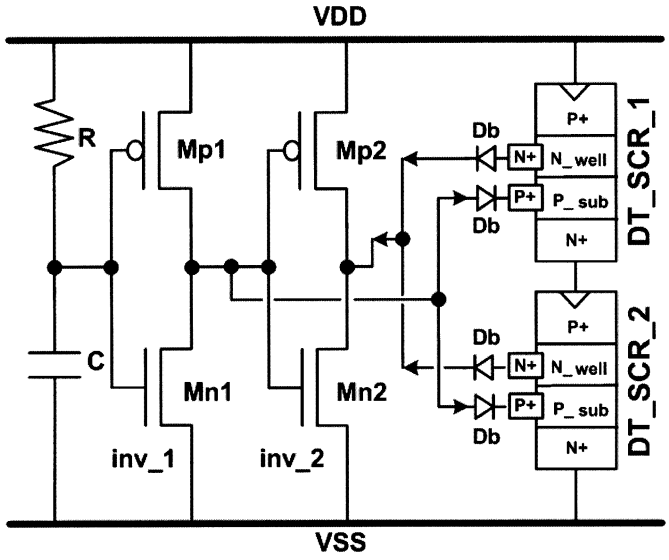

Fig. 12. Power-rail ESD clamp circuit designed with two stacked DT_SCR devices and ESD-detection circuit.

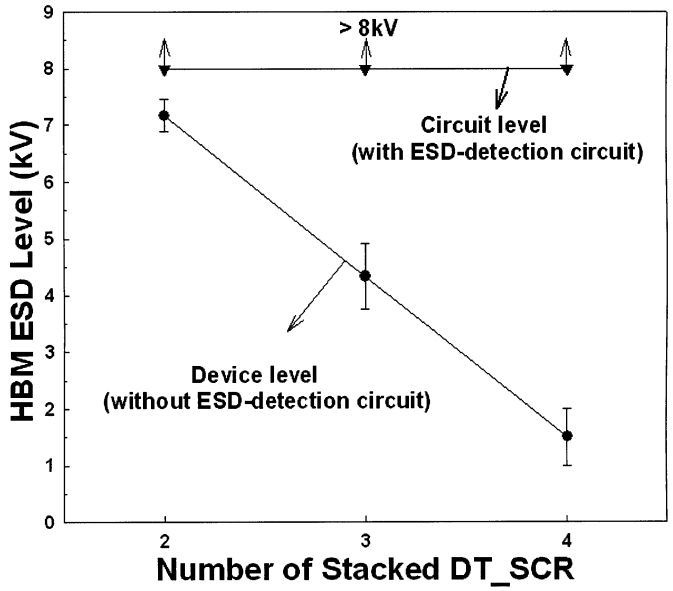

Fig. 13. Dependence of the HBM ESD levels of stacked DT_SCR configuration on the number of the stacked DT_SCR devices. (Failure criterion: $I_{\rm leakage} > 1\ \mu$A at 2.5-V bias.)

at $V_{\rm SS}/V_{\rm DD}$ in this situation, so the two stacked DT_SCR devices are kept off and do not interfere with normal circuit operating functions.

When a positive ESD voltage is applied to $V_{\rm DD}$ with $V_{\rm SS}$ relatively grounded, the RC delay will keep the input of inv_1 at a relatively low voltage level for a long time. Therefore, the output of inv_1 (or the input of inv_2) will become high, and then the output of inv_2 will be kept at a low voltage level. Thus, the p-trigger and n-trigger current voltage pulses can be synchronously generated to trigger on the two stacked DT_SCR devices. ESD current is discharged from $V_{\rm DD}$ to $V_{\rm SS}$ through the stacked DT_SCR devices. When a negative ESD voltage is applied to $V_{\rm DD}$ with $V_{\rm SS}$ relatively grounded, the negative ESD current can be discharged through the forward-biased p-sub ($V_{\rm SS}$)-to-n-well (which is connected to $V_{\rm DD}$) parasitic diode in the ESD protection circuit.

C. ESD Robustness

The human-body-model (HBM) and machine-model (MM) ESD stresses are applied to the ESD protection circuits to verify their ESD robustness. The HBM ESD test results on the stacked DT_SCR devices in the device level (without ESD-detection circuit) and the circuit level (with ESD-detection circuit) are compared in Fig. 13. In these ESD verifications, the failure criterion is defined as the leakage current of the device or circuit after ESD stressed is greater than 1 μA under the voltage bias of 2.5 V. For the device level, the HBM ESD levels of the 2DT_SCR, 3DT_SCR, and 4DT_SCR (without ESD-detection circuit) are 7, 4, and 1.5 kV, respectively. In the layout, each DT_SCR device in the stacked configuration is close to save layout area, so the power (thermal) dissipation

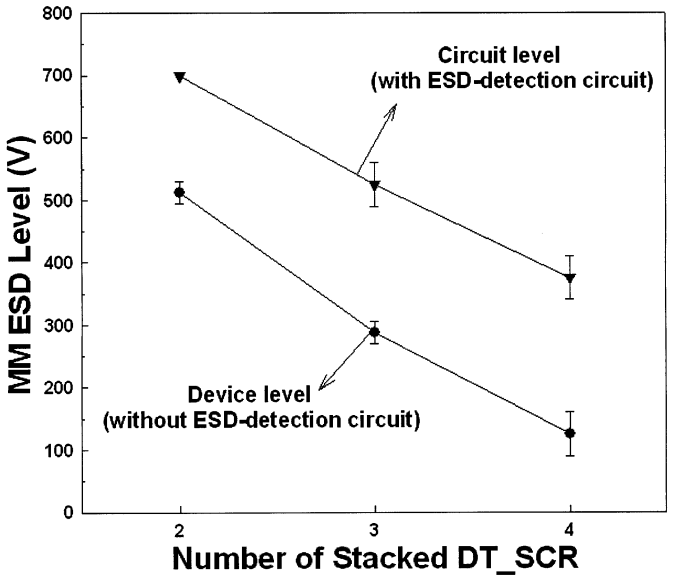

Fig. 14. Dependence of the MM ESD levels of stacked DT_SCR configuration on the number of the stacked DT_SCR devices. (Failure criterion: $I_{\rm leakage} > 1\ \mu$A at 2.5-V bias.)

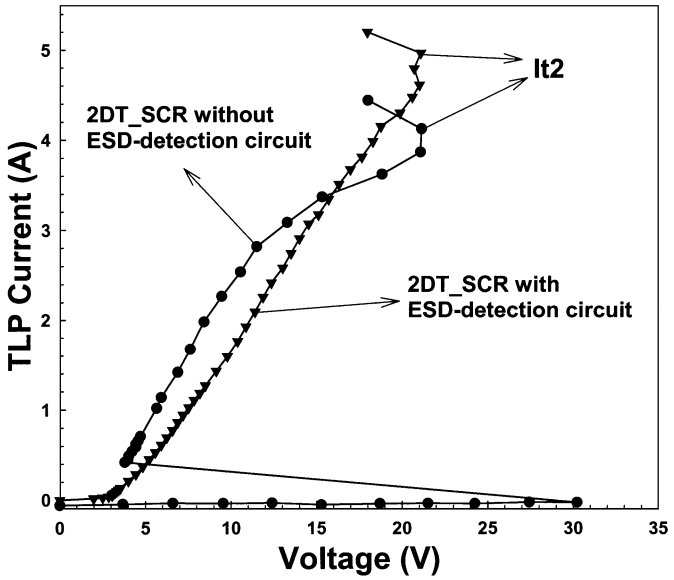

Fig. 15. TLP-measured I–V curves of the two stacked DT_SCR devices with and without ESD-detection circuit. (Failure criterion: $I_{\rm Leakage} > 1\,\mu$A at 2.5 V bias.)

among the stacked DT_SCR devices will interact to reduce the ESD robustness of stacked DT_SCR devices. From another aspect, because the total holding voltage of the stacked DT_SCR configuration is increased with the increase of the number of the stacked DT_SCR devices, the HBM ESD robustness of the stacked DT_SCR devices is decreased due to power $= I_{\rm ESD} \times V_{\rm hold}$. But the ESD levels of the stacked DT_SCR devices can be greatly improved for the 3DT_SCR or 4DT_SCR, if the desired ESD-detection circuit is used to trigger the stacked DT_SCR devices on. From Fig. 13, the ESD levels of the stacked DT_SCR devices with ESD-detection circuit are all boosted up to >8 kV.

The measurement results on the MM ESD levels of the stacked DT_SCR devices with and without the ESD-detection circuit are shown in Fig. 14. The MM ESD level is also decreased when the number of stacked DT_SCR devices is increased. However, the MM ESD levels of the stacked DT_SCR devices can also be improved if the desired ESD-detection circuit is used to trigger the stacked DT_SCR devices on. The MM ESD levels of the 2DT_SCR, 3DT_SCR, and 4DT_SCR (with the ESD-detection circuit) are 700, 525, and 375 V, respectively.

A gate-grounded nMOS (GGNMOS) device with W/L of 200/0.5 μm has also been fabricated in the same CMOS process with an extra silicide-blocking mask for comparison reference. The GGNMOS, which occupies a large active layout area of 25.8 μm × 50 μm, can sustain the HBM ESD level of 3.5 kV. For the ESD protection circuit designed with 2DT_SCR and ESD-detection circuit, the HBM (MM) ESD level per layout area is >10 V/μm^2 (0.88 V/μm^2), but it is only 2.71 V/μm^2 (0.29 V/μm^2) for the GGNMOS. This verifies the excellent area efficiency of the ESD protection circuits realized with the DT_SCR devices.

By using the transmission line pulsing (TLP) measurement [15], [16], the secondary breakdown current $I_{\rm t2}$ of the DT_SCR device can be found. The $I_{\rm t2}$ is another index for the HBM ESD robustness, which is indicated in this work by the sudden increase of the leakage current at the voltage bias of 2.5 V. The relation between second breakdown current $I_{\rm t2}$ and HBM ESD level $V_{\rm ESD}$ can be approximated as

$$V_{\rm ESD} \cong (1500 + R_{\rm on}) \times I_{\rm t2} \tag{1}$$

where $R_{\rm on}$ is the dynamic turn-on resistance of the device under test. The TLP-measured I–V curves of the two stacked DT_SCR devices with and without ESD-detection circuit depicted in Fig. 12 are shown in Fig. 15. The stacked DT_SCR devices with ESD-detection circuit can be triggered on at a lower voltage level of ∼2 V, however, the stacked DT_SCR devices without ESD-detection circuit cannot be triggered on until a higher voltage level of ∼30 V is reached. Moreover, the $I_{\rm t2}$ of the stacked DT_SCR device with ESD-detection circuit can be improved, which is in accordance with the

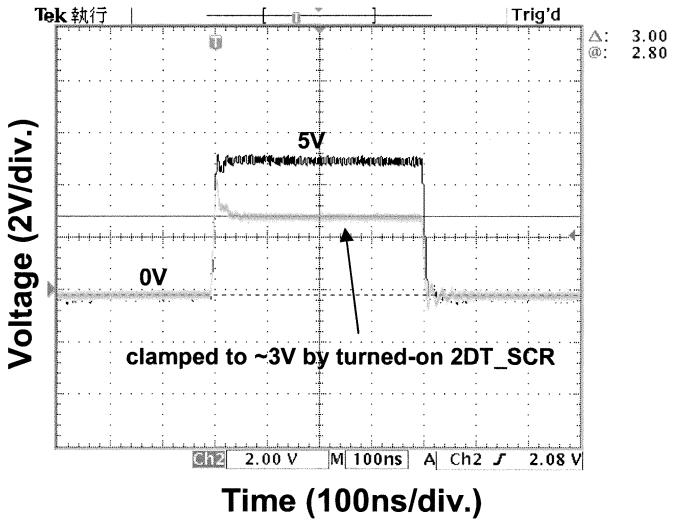

Fig. 16. Measured voltage waveforms to verify the turn-on efficiency of the power-rail ESD clamp circuit with two stacked DT_SCR devices.

results in Fig. 13. This confirms that the ESD-detection circuit proposed in this paper can indeed reduce the switching voltage of DT_SCR and enhance its ESD robustness.

D. Turn-On Verification

In order to verify the function of the ESD protection circuit in Fig. 12, a voltage pulse with a pulsewidth of 400 ns and rise time of 10 ns is applied to $V_{\rm DD}$ of Fig. 12 with grounded $V_{\rm SS}$. In Fig. 16, a 0–5-V voltage pulse applied on the $V_{\rm DD}$ pin is clamped to $\sim$3 V by the turned-on 2DT_SCR. This implies that the ESD-detection circuit realized with the R, C, inv_1, and inv_2 can indeed generate the required double-triggered currents. The stacked DT_SCR devices can be successfully triggered into latching state without involving the junction avalanche breakdown mechanism. The clamped voltage of $\sim$3 V verifies that the proposed ESD protection circuits with two stacked DT_SCR devices are free of the latchup issue under normal operating conditions.

IV. Conclusion

A novel DT_SCR device used for on-chip ESD protection circuits has been successfully investigated in a 0.25-μm salicided CMOS process. With both the substrate and n-well triggered currents, the switching voltage and turn-on time of DT_SCR device can be successfully reduced to only $\sim$1.5 V and $\sim$10 ns, respectively. For IC applications with $V_{\rm DD}$ of 2.5 V, the ESD protection circuits designed with two DT_SCR devices in stacked configuration and ESD-detection circuits have a clamp voltage of $\sim$3 V, which are free of the latchup issue. Such ESD protection circuits can sustain the HBM (MM) ESD level per area of $>$10 V/μm^2 (0.88 V/μm^2) in a 0.25-μm fully salicided CMOS process without using extra process modifications.

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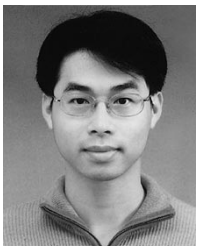

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