Study of Nickel Silicide Contact on Si/Si_{1-x}Ge_x

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Abstract—The properties of nickel silicide formed by depositing nickel on $\mathrm{Si}/P^+ - \mathrm{Si}_{1-x} \mathrm{Ge}_x$ layer are compared with that of nickel germanosilicide on $P^+ - \mathrm{Si}_{1-x} \mathrm{Ge}_x$ layer formed by depositing Ni directly on $P^+ - \mathrm{Si}_{1-x} \mathrm{Ge}_x$ layer without silicon consuming layer. After thermal annealing, nickel silicide on $\mathrm{Si}/P^+ - \mathrm{Si}_{1-x} \mathrm{Ge}_x$ layer shows lower sheet resistance and specific contact resistivity than that of nickel germanosilicide on $P^+ - \mathrm{Si}_{1-x} \mathrm{Ge}_x$ layer. In addition, small junction leakage current is also observed for nickel silicide on $\mathrm{Si}/P^+ - \mathrm{Si}_{1-x} \mathrm{Ge}_x/N - \mathrm{Si}$ diode. In summary, with a Si consuming layer on top of the $\mathrm{Si}_{1-x} \mathrm{Ge}_x$, the nickel silicide contact formed demonstrated improved electrical and materials characteristics as compared with the nickel germanosilicide contact which was formed directly on $\mathrm{Si}_{1-x} \mathrm{Ge}_x$ layer.

Index Terms-Agglomerate, Ni, SiGe, silicide.

I. Introduction

due to its potential applications as the contacts for the SiGe based electronic devices such as the base metal for HBTs [1] and advanced SiGe source/drain for deep submicron CMOS [2]. For the sub-100-nm technology node, the widely used CoSi₂ contact is expected to be replaced by NiSi contact in the future. Except problem of excessive silicide on narrow lines [3], NiSi has several advantages over CoSi₂ when used in the ultrasmall CMOS technology. They are: low temperature silicidation process, no bridging failure property, smaller mechanical stress, low silicon consumption [4], and one step silicidation process [5]. These advantages also apply when NiSi is used as the contact material for $Si_{1-x}Ge_x$. In this letter, we investigated the electrical and material properties of the nickel silicide formed by depositing nickel on $Si/P^+ - Si_{1-x}Ge_x$ and annealed by rapid thermal annealing (RTA) method and compared the properties with that of the nickel germanosilicide formed by direct deposition of nickel on $P^+ - Si_{1-x}Ge_x$ without Si intermediate layer.

II. EXPERIMENTS

N-type 6 in (100) silicon wafers with 10–15 Ωcm sheet resistance were used as the starting substrates. Strained $\mathrm{Si}_{1-x}Ge_x$

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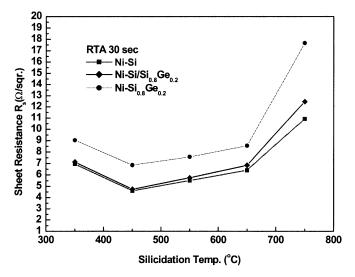


Fig. 1. Sheet resistances comparison of annealed Ni silicide and Ni germano-silicide for P-Si, $\mathrm{Si}/\mathrm{P^+} - \mathrm{Si}_{0.8}\mathrm{Ge}_{0.2}$ and $\mathrm{P^+} - \mathrm{Si}_{0.8}\mathrm{Ge}_{0.2}$ samples.

thin films with x = 0.09, 0.14, 0.2, and 0.3 were grown on these wafers by an ultrahigh vacuum chemical molecular epitaxy (UHVCME) system [6]. Wafers were precleaned, loaded, and transferred into the growth chamber and heated to 850 °C for 500 s for further cleaning of the Si surface. For the growth of the in situ boron-doped $Si_{1-x}Ge_x$ layers, pure GeH_4 , Si_2H_6 , and 1% B_2H_6 diluted with H_2 were used to achieve a boron concentration of 2×10^{19} cm⁻³ in all cases. For the P⁺ – Si_{1-x}Ge_x layer samples, the thickness of the $Si_{1-x}Ge_x$ epitaxial layer was $100\,\text{nm}.$ For the $Si/P^+-Si_{1-x}Ge_x$ layer samples, the thickness of the $Si_{1-x}Ge_x$ epitaxial layer was also 100 nm, and the thickness of the Si cap layers is 25 nm. A 15-nm-thick nickel film was then deposited by the Metal-PVD on these epitaxial wafers and a 5-nm-thick TiN cap layer was deposited on the top to prevent nickel oxidation during the silicidation process. The silicidation reactions were then performed in an RTA system with nitrogen ambient for 30 s with different annealing temperatures. After silicidation process, the TiN-capping layer and the unreacted Ni film were selectively removed by wet etching in 4 H₂SO₄: 1 H₂O₂ (30%) solution. The sheet resistance was measured by four-point probe system. Specific contact resistivity $\rho_{\rm C}$ measurement was performed using the transmission line model (TLM) [7]. Scanning electron microscopy (SEM) and transmission electron microscopy (TEM) in conjunction with energy dispersive spectrometry (EDS) were used for materials study.

III. RESULTS AND DISCUSSION

Fig. 1 compares the sheet resistances (Rs) of the nickel silicide formed on $\mathrm{Si/P^+} - \mathrm{Si_{0.8}Ge_{0.2}}$ and the nickel ger-

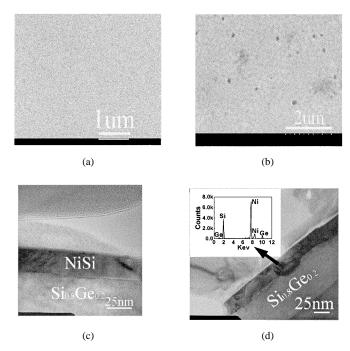


Fig. 2. SEM micrographs of the surface morphology of the (a) $\rm Ni/Si/Si_{0.8}Ge_{0.2}$ sample annealed at 500 $^{\circ}\rm C$ for 30 s and (b) $\rm Ni/Si_{0.8}Ge_{0.2}$ sample annealed at 500 $^{\circ}\rm C$ for 30 s. Cross-section TEM of (c) $\rm Ni/Si_{0.8}Ge_{0.2}$ sample annealed at 500 $^{\circ}\rm C$ for 30 s and (d) $\rm Ni/Si_{0.8}Ge_{0.2}$ sample annealed at 500 $^{\circ}\rm C$ for 30 s and (d) $\rm Ni/Si_{0.8}Ge_{0.2}$ sample annealed at 500 $^{\circ}\rm C$ for 30 s.

manosilicide formed on P^+ – $Si_{0.8}Ge_{0.2}$. The R_S of the nickel silicide on pure P-Si is also shown for comparison. As can be seen in Fig. 1, when the samples were annealed at 450-650 °C for 30 s, the nickel silicide formed on the $Si/P^+ - Si_{0.8}Ge_{0.2}$ sample exhibits superior R_S than that of the nickel germanosilicide formed on the P^+ – $Si_{0.8}Ge_{0.2}$ sample. Its R_S is 4.75–5.75 Ω/\Box , which is similar to that of the nickel silicide formed on P-Si. Additionally, the temperature stability of the silicide degrades as the nickel thickness decreases, because the thinner nickel film can easily be consumed to form NiSi during its silicidation process, and NiSi will convert into NiSi₂ when annealed at elevated temperatures. In our experiments, 15-nm nickel was used; the temperature stability of the silicide formed is lower than that of the silicide film formed with thicker nickel film as reported in [8], [9]. From the SEM [Fig. 2(a), (b)] and cross-sectional TEM images [Fig. 2(c), (d)], we can observe that the nickel silicide formed on the $Si/P^+ - Si_{0.8}Ge_{0.2}$ sample lacks agglomeration, and the layer of nickel silicide is very uniform. However, the nickel germanosilicide formed on the P^+ – $Si_{0.8}Ge_{0.2}$ sample shows severe agglomeration and microvoids, and the layer of nickel germanosilicide is very rough. The EDS/cross-section TEM analysis indicates that the agglomerate is $Ni_2(Si_{1-v}Ge_v)$ as shown in Fig. 2(d). However, the mechanism for the formation of $Ni_2(Si_{1-v}Ge_v)$ agglomeration needs further investigation. This is why the nickel silicide formed on the Si/P^+ – $Si_{0.8}Ge_{0.2}$ sample has a lower R_S than the nickel germanosilicide formed on the $P^+ - Si_{0.8}Ge_{0.2}$ sample. As the silicidation temperature was increased to 750 °C, the formation of Ni(Si_{1-v}Ge_v)₂ phases along with the formation of agglomerates with microvoids cause the increase in the $R_{\rm S}$ value for the P^+ – $\rm Si_{0.2}Ge_{0.8}$

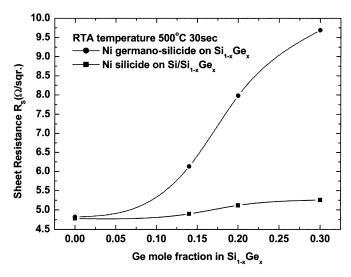


Fig. 3. Sheet resistance as a function of Ge mole fraction for 25 nm Si capping layer and $\rm P^+ - Si_{1-x}Ge_x$ layer after annealing at 500°C for 30 s.

sample as shown in Fig. 1. Fig. 3. shows R_S of the nickel silicide and the nickel germanosilicide as a function of Ge mole fraction in the Si_{1-x}Ge_x layer after RTA process at 500 °C for 30 s. The R_S value of the nickel germanosilicide increases significantly as the Ge mole fraction in the $P^+ - Si_{1-x}Ge_x$ layer increases. This is due to more nickel germanosilicide agglomerate and micro-void formation in the $P^+ - Si_{1-x}Ge_x$ samples as the Ge mole fraction increases as observed by the SEM. These phenomena are attributed to the lower heat formation for metal-Ge than for metal-Si [10]. For the Si/P^+ – $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ samples, the R_S increases slightly as the Ge fraction increases. From our SEM observations, nickel germanosilicide agglomeration starts to occur in theses samples as the Ge fraction increases. This indicates that, for the samples with higher Ge fraction, the thickness of the Si cap layer must be increased to avoid nickel germanosilicide agglomeration. The specific contact resistivity $\rho_{\rm C}$ of these contacts were also measured. A low $\rho_{\rm C}$ value of 0.42 $\mu\Omega-{\rm cm}^2$ is observed for the $\mathrm{Si/P^+}$ – $\mathrm{Si_{0.8}Ge_{0.2}}$ sample. Meanwhile, the ρ_{C} for the $P^+ - Si_{0.8}Ge_{0.2}$ contact is 3.25 $\mu\Omega - cm^2$ which is much high than the $Si/P^+ - Si_{0.8}Ge_{0.2}$ contact. This is believed to be due to rough interface and nickel germanosilicide agglomeration in the surface of the P^+ – $Si_{0.8}Ge_{0.2}$ sample.

The characteristics of the P–N junction diodes with nickel silicide and nickel germanosilicide contacts were also studied. The contacts were formed by annealing at an optimum condition of 500 °C for 30 s. Fig. 4 shows the forward and reverse $\it I-V$ characteristics of the nickel silicided $\rm Si_{1-x}Ge_x$ diodes with different structures (i.e., $\rm Si/P^+ - Si_{0.8}Ge_{0.2}, P^+ - Si_{0.8}Ge_{0.2}, P^+ - Si_{0.7}Ge_{0.3}$). It was observed that the reverse leakage current ($\rm I_{OFF}$) decreases significantly for the sample with a 25-nm Si Cap layer on the $\rm Si_{0.8}Ge_{0.2}$ layer ($\rm I_{OFF} < 3.5 \times 10^{-8}$ A). A larger $\rm I_{OFF}$ for the $\rm Si_{0.7}Ge_{0.3}$ diode is believed to be due to more nickel germanosilicide agglomerate formation on the surface. This again confirms that in order to improve the electrical characteristics of the nickel silicide contact on $\rm Si_{1-x}Ge_x$ layer, a suitable thickness of the Si consuming layer should be grown on top of the $\rm Si_{1-x}Ge_x$ layer for silicide formation.

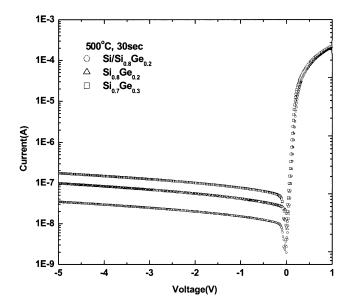


Fig. 4. The forward and reverse characteristics for Si/Si $_{0.8}$ Ge $_{0.2}$, Si $_{0.8}$ Ge $_{0.2}$, Si $_{0.7}$ Ge $_{0.3}$ P⁺ – N junction.

IV. CONCLUSION

We have demonstrated that in order to improve the sheet resistance, specific contact resistivity and junction leakage current of the nickel silicide contact on $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ layer, a Si consuming layer with an appropriate thickness should be grown on the top of the $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ layer for silicide formation. Low sheet resistance of 4.75–5.75 Ω/\square , low specific contact resistivity of 0.42 $\mu\Omega$ – cm^2 and low junction leakage current of 3.5 \times 10^{-8} A were obtained on the $\mathrm{Si/P^+}$ – $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ sample with a 25-nm Si consuming layer in our study. The developed high quality nickel silicide contact technology can be used for the base contact technology of SiGe HBTs and for

the Ohmic contacts for the SiGe raised source/drain technology in deep submicron MOSFETs.

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REFERENCES

- J. Eberhardt and E. Kasper, "Ni/Ag metallization for SiGe HBT's using a Ni silicide contact," *Semicond. Sci. Technol.*, vol. 16, pp. L47–L49, 2001.
- [2] M. C.Mehmet C. Öztürk, J.Jing Liu, H.Hongxiang Mo, and N.Nemanja Pesovic, "Advanced Si_{1-x}Ge_x source/drain and contact technologies for sub-70 nm CMOS," in *IEDM Tech. Dig.*, 2002, pp. 375–378.
- [3] J. P. Lu, D. Miles, J. Zhao, A. Gurba, Y. Xu, C. Lin, M. Hewson, J. Ruan, L. Tsung, R. Kuan, T. Grider, D. Mercer, and C. Montgomery, "A novel nickel SALICIDE process technology for CMOS devices with sub-40 nm physical gate length," in *IEDM Tech. Dig.*, 2002, pp. 371–374.
- [4] H.Hiroshi Iwai, T.Tatsuya Ohguro, and S.-I.Shun-Ichiro Ohmi, "NiSi salicide technology for scaled CMOS," *Microelectron. Eng.*, vol. 60, pp. 157–169, 2002.
- [5] J. P. Gambino and E. G. Colgan, "Silicides and ohmic contacts," *Mater. Chem. Phys.*, vol. 52, pp. 99–146, 1998.
- [6] L. P. Chen, C. T. Chou, G. W. Huang, W. C. Tsai, and C. Y. Chang, "Boron incorporation in $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ films grown by ultrahigh vacuum chemical vapor deposition using $\mathrm{Si}_2\mathrm{H}_6$ and GeH_4 ," *Appl. Phys. Lett.*, vol. 67, pp. 3001–3003, 1995.
- [7] D. K.Dieter K. Schroder, Semiconductor Material and Device Characterization, 2nd ed: Wiley, pp. 149–159.
- [8] D.-X. Xu, S. R. Das, C. J. Peters, and L. E. Erickson, "Material aspects of nickel silicide for ULSI applications," *Thin Solid Films*, vol. 326, pp. 143–150, 1998.
- [9] A. Lauwers, P. Besser, T. Gutt, A. Satta, M. de Potter, R. Lindsay, N. Roelandts, F. Loosen, S. Jin, H. Stucchi, C. Vrancken, B. Deweerdt, and K. Maex, "Comparative study of Ni-silicide and Co-silicide for sub 0.25-μm technologies," *Microelectron. Eng.*, vol. 50, pp. 103–116, 2000
- [10] J. S. Luo, W. T. Lin, C. Y. Chang, and P. S. Shih, "Interfacial reactions of $\rm Ni/Si_{0.76}Ge_{0.24}$ and $\rm Ni/Si_{1-x-y}Ge_xC_y$ by vacuum annealing and pulsed KrF laser annealing," *Nuclear Instrum. Meth. Phys. Res. B*, vol. 169, pp. 124–128, 2000.