High-Performance $Pt/SrBi_2Ta_2O_9/HfO_2/Si$ Structure for Nondestructive Readout Memory

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***Abstract*—Metal-ferroelectric-insulator-semiconductor (MFIS) capacitors with 390-nm-thick $SrBi_2Ta_2O_9$ (SBT) ferroelectric film and 8-nm-thick hafnium oxide (HfO_2) layer on silicon substrate have been fabricated and characterized. It is demonstrated for the first time that the MFIS stack exhibits a large memory window of around 1.08 V at an operation voltage of 3.5 V. Moreover, the MFIS memory structure suffers only 18% degradation in the memory window after 10^9 switching cycles. The excellent performance is attributed to the formation of well-crystallized SBT perovskite thin film on top of the HfO_2 buffer layer, as evidenced by the distinctive sharp peaks in X-ray diffraction (XRD) spectra. In addition to its relatively high κ value, HfO_2 also serves as a good seed layer for SBT crystallization, making the proposed $Pt/SrBi_2Ta_2O_9/HfO_2/Si$ structure ideally suitable for low-voltage and high-performance ferroelectric memories.**

***Index Terms*—Ferroelectric, hafnium oxide, memory window, metal-ferroelectric-insulator-semiconductor (MFIS), $SrBi_2Ta_2O_9$.**

I. Introduction

METAL-ferroelectric-insulator-semiconductor (MFIS) structure has attracted considerable attention as a promising candidate for high-density and high-speed field effect transistor (FET)-type ferroelectric nonvolatile memories (FeMFETs) [1]. FeMFETs have several advantages over 1 transistor/1 capacitor (1T/1C) ferroelectric random access memories (FeRAMs), including smaller cell size, simpler process flow, and in particular, the nondestructive readout operation (NDRO) feature. The purpose of inserting an insulating layer in the structure is to prevent the reaction and interdiffusion between the ferroelectric film and the silicon substrate as well as to improve the retention properties [2], [3]. However, the insertion of the insulating layer results in additional voltage drop across the layer, thus reduces the electric field in the ferroelectric film, leading to unfavorable nonsaturated polarization. Therefore, finding a suitable insulating layer with high thermal stability and relatively high κ value (to reduce undesirable voltage drop) becomes the key issue in pursuing the NDRO low-voltage and high-density FeRAMs [4]–[9].

Manuscript received April 29, 2003; revised June 20, 2003. This work was supported in part by the National Science Council of Taiwan, R.O.C., under Contract NSC-91-2215-E-317-009. The review of this letter was arranged by Editor T.-J. King.

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Digital Object Identifier 10.1109/LED.2003.816582

In this letter, we employ for the first time an HfO_2 thin film as the insulating layer for fabricating MFIS capacitors with $Pt/SrBi_2Ta_2O_9/HfO_2/Si$ structure. HfO_2-based high-κ dielectric is extremely attractive because of its high thermal stability, high interface quality on silicon, and relatively high κ value [10], [11]. It is found that memory window of such stack structure can be as large as 1.08 V at a very low operation bias of 3.5 V. More importantly, it exhibits excellent endurance against switching degradation up to 10^9 cycles (i.e., only $\sim$18% degradation in memory window). Strong peaks indicative of perovskite phase in X-ray diffraction (XRD) spectra confirm that SBT films with superior crystallinity can be obtained on top of the HfO_2 insulating layer.

II. Experimental

The MFIS capacitors were fabricated on 6-in (100) p-type silicon wafers. The 8-nm-thick HfO_2 film was deposited by atomic vapor deposition (AVD) on an AIXTRON Tricent system at a substrate temperature of 400 °C in oxygen ambient, and then annealed at 1000 °C for 30 s in nitrogen atmosphere. Subsequently, the $SrBi_2Ta_2O_9$ film was deposited by metaloganic decomposition (MOD) technique subjected to a baking sequence; the conditions of which were 120, 250, and 400 °C for 10 min in air. After the target film thickness of about 390 nm was achieved through multiple repetitions of the process steps, the film was crystallized at 750 °C for 3 min by rapid thermal annealing (RTA) in O_2 atmosphere. Finally, Pt was deposited to serve as the top electrode by electron beam evaporation through a shadow mask with an area of 2.0×10^{-4} cm^2.

The microstructures and crystallinity of the ferroelectric thin films were analyzed by atomic force microscopy (AFM) and XRD, respectively. The leakage currents were measured using a Keithley 4200 semiconductor characterization system, and the capacitance-voltage (*C–V*) characteristics were extracted using an HP4284A precision LCR meter at a frequency of 100 kHz. Finally, the program/erase endurance tests were performed by a system comprised of HP8110A 150 MHz pulse generator, HPE5250A low leakage switch matrix, and HP 4284A precision LCR meter.

III. Results and Discussion

The XRD profile of the $SrBi_2Ta_2O_9$ thin film annealed at 750 °C for 3 min in oxygen atmosphere is illustrated in Fig. 1. Distinctive peaks which are indicative of well crystallized perovskite phase imply that HfO_2 film acts as a seed layer for SBT crystallization, similar to what Pt does in the MIM structure. The resultant SBT film is polycrystalline with the predominant

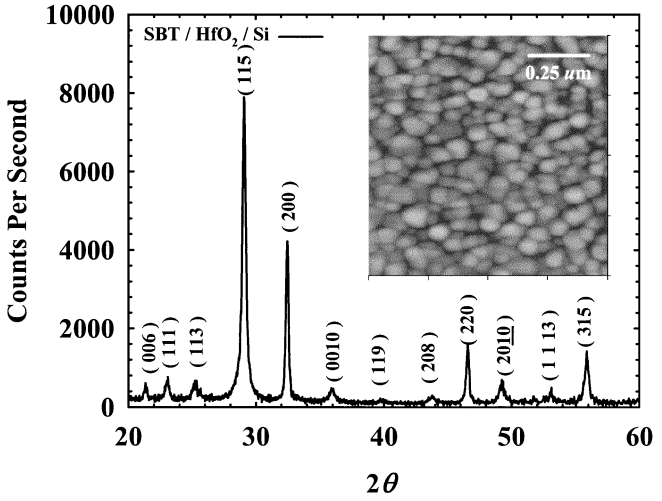


Fig. 1. XRD profile of $SBT/HfO_2/Si$ structure. The inset shows the morphology of the SBT surface.

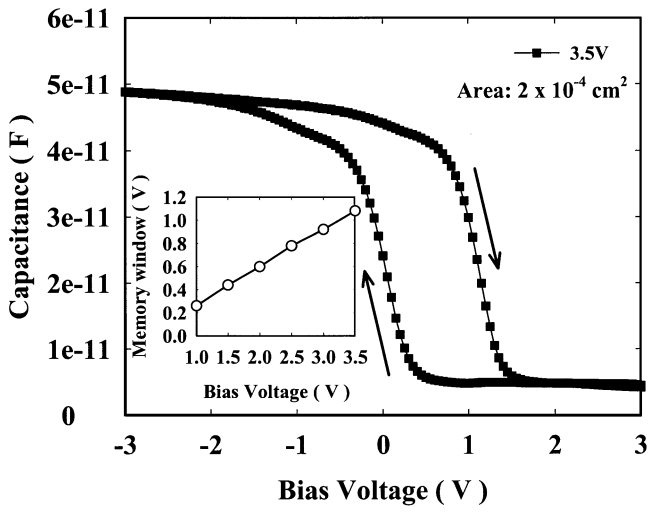
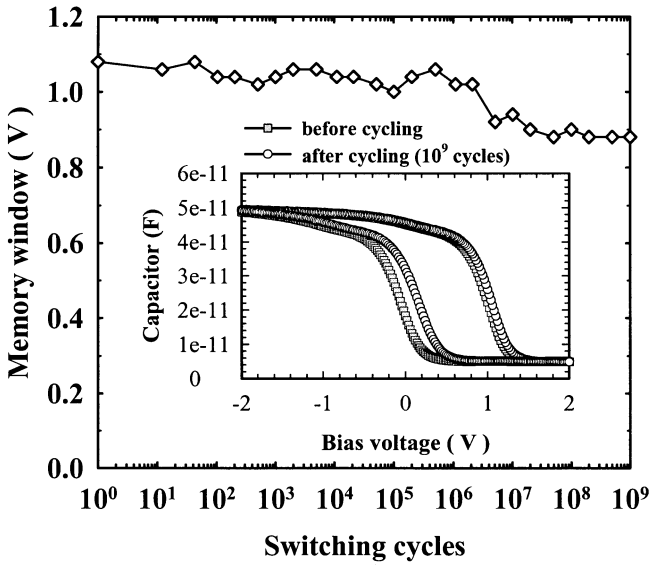
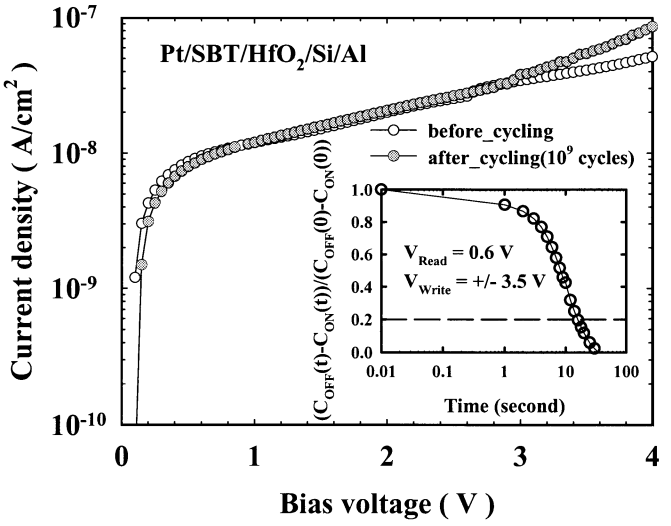


Fig. 2. High-frequency *C–V* characteristics of $Pt/SBT/HfO_2/Si$ structure with different sweeping voltages. Memory window is 1.08 V at a sweeping voltage of 3.5 V. The inset shows that the memory window is a function of sweep voltage.



(a)



(b)

Fig. 3. (a) Memory window as a function of switching cycles for $Pt/SBT/HfO_2/Si$ structure. The inset shows the *C–V* characteristics before and after 10^9 switching cycles. (b) Current density–voltage characteristics before and after 10^9 switching cycles. The inset shows the retention characteristic of this structure.

orientations of (115) and (200). Owing to the fact that the polarization vector most likely lies in the a-b plane, rather than along the c-axis, in bismuth layered perovskite ferroelectrics, the favorable growth along (115) and (200) makes the resultant SBT film more easily polarized. This distinctive feature, we believe, is the key to the low voltage operation. The crystalline microstructure of the SBT film is also analyzed by AFM. As shown in the inset of Fig. 1, the film depicts surface morphology with uniformly distributed and considerably large grains ($\sim$80 nm).

Fig. 2 shows the high-frequency *C–V* characteristics of the $Pt/SrBi_2Ta_2O_9/HfO_2/Si$ structure. The equivalent oxide thickness (EOT) is about 14 nm as calculated from the accumulation capacitance. A memory window of 1.08 V is clearly demonstrated in a back-and-forth voltage sweep between -3.5 and 3.5 V. The estimated ratio of the memory window to the applied voltage, as shown in the inset of Fig. 2, is 26.4%. In addition to the well-crystallized perovskite structure of the SBT film, we attribute such excellent performance to the large capacitance and high quality of the underneath HfO_2 thin film. The EOT of the accompanying $Pt/HfO_2/Si$ test structure, as calculated from the *C–V* measurement, is only about 2.8 nm. According to the voltage divider principle for in-series capacitors, most of the applied voltage will drop across the SBT film, which in turn leads to a well-saturated polarization behavior for the ferroelectric SBT film. Moreover, only negligible hysteresis coming from traps in the bulk has appeared in the back-and-forth *C–V* sweeping. This leaves the hysteresis originating from polarization unaffected because these two types of hystereses always act in opposite direction.

A bipolar pulse train with 3.5 V in amplitude and a pulse width of 2 μs was employed for testing the switching characteristics of the $Pt/SBT/HfO_2/Si$ structure. The endurance results are shown in Fig. 3(a). After switching over 10^9 times, the degradation of the memory window is found to be only

about 18%, shown in the inset of Fig. 3(a). To further examine the degradation after stress, the leakage current characteristics of the $Pt/SBT/HfO_2/Si$ structure before and after cycling are shown in Fig. 3(b). It can be seen that up to 10^9 program/erase switching cycles cause almost no leakage current degradation below 3 V gate bias, and only slight increase above 3 V gate bias. The increase of the leakage current at higher gate bias is believed to be due to the stress-induced leakage current (SILC) of the SBT film, since the SBT film is known to be more vulnerable to current stress. Furthermore, the retention characteristic of this structure is illustrated in the inset of Fig. 3(b). Contrast to the excellent switching property, poor retention is observed with this stack configuration. It is speculated coming from the inherent large leakage of the MOD-prepared SBT thin film. To improve the retention characteristic, an SBT thin film deposited with sputtering technique is currently under our investigation.

IV. Conclusion

In summary, we have demonstrated for the first time the feasibility of fabricating MFIS capacitors with 390-nm-thick $SrBi_2Ta_2O_9$ ferroelectric film and 8-nm-thick HfO_2 dielectric film on silicon substrate. It is shown that the $Pt/SrBi_2Ta_2O_9/HfO_2/Si$ (MFIS) structure can provide a memory window as large as 1.08 V at an operation voltage of 3.5 V. In addition, it also exhibits excellent switching characteristics with only 18% degradation in memory window after 10^9 switching cycles. These results indicate that HfO_2 is suitable for the low-voltage and high-density NDRO FeMFET applications.

Acknowledgment

The authors would like to thank Dr. H.-Y. Lee at SRRC, Taiwan, R.O.C., for providing the X-ray diffraction analyzer, and Dr. H.-T. Chiu of the Department of Applied Chemistry, National Chiao-Tung University, Taiwan, for providing atomic force microscopy.

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