A One-Step Single-Cleaning Solution for CMOS Processes

T. S. Chao,[a,b,z] C. H. Yeh,[c] T. M. Pan,[d,*] T. F. Lei,[d] and Y. H. Li[e]

[a]*Department of Electrophysics and* [d]*Department of Electrical Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan*
[b]*National Nano Device Laboratories, Hsinchu, Taiwan*
[c]*Department of Engineering of Systems and Science, National Tsing Hua University, Hsinchu, Taiwan*
[e]*Merck-Kanto Advanced Chemistry, Limited, Taoyuan, Taiwan*

In this paper, we demonstrate a one-step single-cleaning solution to replace the conventional RCA two-step cleaning method for complementary metal oxide semiconductor (CMOS) processes. We found the performance of devices fabricated using this new recipe is comparable or even better than that of devices fabricated using the conventional RCA method. The benefits of this method are more efficient removal of contaminants, improved driving current of devices, simpler processing, fewer steps in cleaning, time savings, reduction of cost and of chemical waste, and reduced impact on the environment.
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The RCA cleaning processes has been used for more than 30 years in silicon cleaning processes.[1] It is still used in advanced complementary metal oxide semiconductor (CMOS) production lines. There are two steps in the RCA cleaning process. The first step is using an $NH_4OH:H_2O_2:H_2O$ mixture (namely, standard clean 1, SC-1) to remove particles and some trace metallic contamination. The second step is using an $HCl:H_2O_2:H_2O$ mixture (namely, standard clean 2, SC-2) to remove metallic contaminants. The temperature of both steps are ~70°C, and the exposure time is 10 min. Generally, if wafers undergo patterning and stripping processes involving the photoresist (PR) before the standard RCA cleaning process, an additional step including $H_2SO_4:H_2O_2$ (SPM) should be added to remove the residual PR. In standard CMOS processes, many different cleaning processes must be used to maintain cleanliness on the wafer surface during the whole process. Figure 1 shows a typical cleaning process in a deep subquarter micrometer CMOS fabrication. It can be seen that before silicidation, generally referred as the front-end processes, there are 19 cleaning steps. It is noted that four different cleaning methods are used. Clean A consists of SPM followed by RCA. Clean B consists of the RCA. Clean C consists of SPM only. Clean D consists of SPM followed by diluted HF solution (pregate oxide cleaning). Obviously, the number of cleaning steps in a typical CMOS fabrication process is large and cleaning methods are complex at the same time. Recently, many modifications of the conventional RCA two-step cleaning process have been proposed for improving cleaning efficiency and to reduce process cost and cycle time.[2-5] However, these reports focus only on the pregate oxide cleaning (clean D). The purpose of this paper is to present a one-step single-solution cleaning process to replace all cleaning methods mentioned above and listed in Fig. 1. The cleaning efficiency and the performance of the final devices is shown to be comparable to RCA counterparts.

In our previous reports,[6,7] such a one-step single-cleaning solution has been successfully employed in post-CMP cleaning after poly-Si polishing,[6] and in pregate oxide cleaning.[7] This cleaning solution is based on the conventional SC-1 solution with the addition of tetramethyl ammonium hydroxide (TMAH, $NH_4OH = 1:50$ moles) that acts as a surfactant to enhance the removal efficiency of particles, and ethylenediamine tetraacetic acid (EDTA, 100 ppm) to reduce metallic contaminations. We have reported elsewhere[8] that the recipe was optimized for pregate oxide cleaning by a robust design method. The optimum condition was found to be 60°C for 5 min. Compared to the conventional RCA

cleaning process, the temperature is lower (*c.f.*, 60-70°C) and time is shorter (*c.f.*, 5 to 10 min). We have demonstrated that the removal efficiency of particles, metallic and organic contamination, by using this optimum solution was improved over the two-step RCA cleaning process, resulting in comparable, or even better performance. However, in the previous report we only demonstrated its efficacy on one individual step (*e.g.*, pregate oxide cleaning or post-CMP cleaning). In this paper, we extend this cleaning solution to the complete MOS fabrication process. Only one single cleaning solution, in contrast to the two-step RCA cleaning method, was used from wafer start to the silicidation step. We found that this one-step single recipe shows very significant improvements and advantages.

Device Fabrication

Two split lots of n-metal oxide semiconductor field effect transistors (n-MOSFETs) were processed in this study. The control split wafers were cleaned by the conventional RCA cleaning processes as shown in detail in Fig. 1, while the one-step split wafers were cleaned by the proposed one-step single-cleaning solution for every cleaning steps listed in Fig. 1. The rest of the process parameters were kept identical for these two splits, including ion implantation, thermal cycles, and film depositions. So the only difference between the two splits is the cleaning recipe, *i.e.*, clean A to clean D, which were used in the control split (as shown in Fig. 1), were replaced by the one-step single-cleaning solution. It is worth noting that since there is only one cleaning step in the new recipe, it requires only a single DI water rinse in each cleaning step. In our experiments, n-MOSFETs were fabricated on a 6 in. (100)-oriented p-type wafers with a resistivity of 14-21 Ω cm. After p-well implantation with BF_2 (at 70 keV, 1.2×10^{13} cm^{-2}), all wafers underwent a drive-in step at 1100°C for 9 h. The active region was then defined. Local oxidation of silicon (LOCOS) was used to grow a 550 nm field oxide at 980°C. Afterward, BF_2 channel implant (at 90 keV, 1×10^{13} cm^{-2}) and boron antipunch through implant (at 45 keV, 4×10^{12} cm^{-2}) were performed. The gate oxide (3.2 nm) was then thermally grown in furnace, followed by the deposition of a 200 nm poly-Si gate layer at 620°C by low-pressure chemical vapor deposition (LPCVD). The gate oxide thickness was determined by the spectroscopic ellipsometry. The poly-Si film was doped with P^+ ion implantation at 50 keV to a dosage of 5×10^{15} cm^{-2}. After gate patterning, source and drain regions were formed by As^+ implantation (20 keV, 5×10^{15} cm^{-2}). Next, wafers were annealed by rapid thermal processing (RTP) at 1050°C for 20 s, followed by the deposition of a 550 nm oxide for isolation. After contact alignment and etching, Ti/TiN/Al/TiN films were sputtered by physical vapor deposition (PVD) and patterned. Finally, all wafers were sintered at 400°C for 30 min in a N_2 ambient to form good ohmic contacts.

* Electrochemical Society Student Member.
z E-mail: tschao@mail.nctu.edu.tw

1. Initial clean **[Clean A]**
   H_2SO_4/H_2O_2 (10-min) + H_2O (10-min)
   SC-1 ($NH_4OH/H_2O_2/H_2O$) (10-min) +　　H_2O (10-min)
   SC-2 ($HCl/H_2O_2/H_2O$) (10-min)+ H_2O (10-min)
2. Zero-layer: **[Clean B]**
   SC-1(10-min) + H_2O (10-min)
   SC-2 (10-min) + H_2O (10-min)
3. N-well I/I: **[Clean A]**
4. P-well I/I: **[Clean A]**
5. Define PBLOCOS: **[Clean A]**
6. N-field I/I: **[Clean A]**
7. Oxidation: **[Clean B]**
8. Strip (pad oxide): **[Clean B]**
9. Strip oxide: **[Clean B]**
10. P-anti and V_{th} I/I: **[Clean C]**
11. N-anti and V_{th} I/I: **[Clean C]**
12. Pre-gate oxide: H_2SO_4, O_3, Vapor HF/H_2O: **[Clean D]**
13. Poly-Si etching: **[Clean A]**
14. N-LDD: **[Clean C]**
15. P-LDD: **[Clean C]**
16. Spacer: **[Clean A]**
17. N^+ S/D, I/I: **[Clean C]**
18. P^+ S/D, I/I: **[Clean C]**
19. Pre-silicide: **[Clean A]**

Total:　　**[Clean A]**: 8
　　　　　[Clean B]: 4
　　　　　[Clean C]: 6
　　　　　[Clean D]: 1

Figure 1. The cleaning steps in a typical CMOS process before silicidation step. There are four different cleaning methods.

Particle numbers on the wafer surface were measured by a Tencor surface model 4500 system. The surface roughness was measured by atomic force microscopy (AFM), while metallic contaminants were analyzed by total reflection X-ray fluorescence spectrometer (TXRF, Rigaku model 3700). Electrical measurements
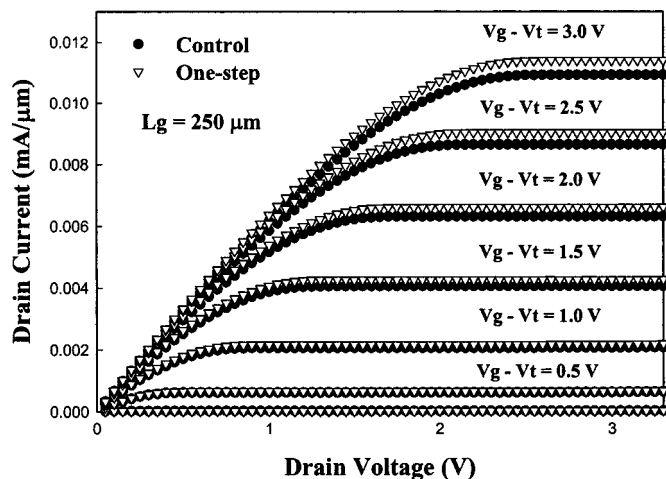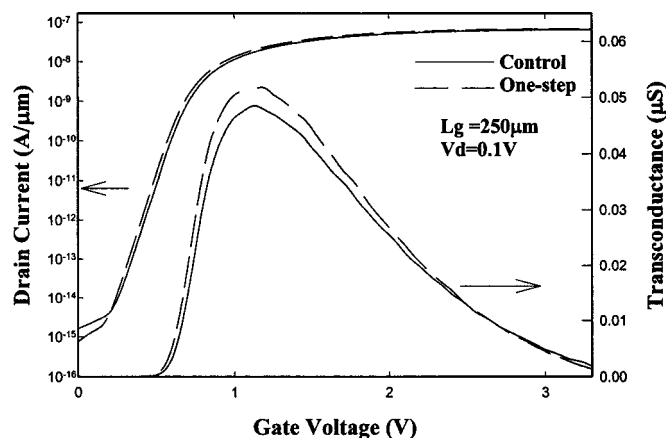

Figure 3. Transconductance for n-MOSFETs with 250 μm channel length at linear region (*i.e.*, $V_d = 0.1$ V).

on n-MOSFETs were measured by a Hewlett-Packard (HP) 4156 semiconductor parameter analyzer. The flatband voltage and interface trap density were obtained by Keithley C-V system.

Results and Discussion

n-MOSFETs with two channel lengths (*i.e.*, 1 and 250 μm for short and long channels, respectively) were characterized in this study. Figure 2 shows $I_d - V_d$ curves for the long-channel (250 μm) devices. Devices from both splits (*i.e.*, one-step and conventional two-step RCA control) exhibit comparable I_{off} that is less than 10 nA/μm, and almost identical threshold voltage (V_t) ~0.70 V. Moreover, the device that underwent a one-step single-cleaning solution (*i.e.*, one-step split) exhibits 4.6% higher driving current than that of RCA counterparts (*i.e.*, the control split), both measured at $V_g - V_t = 3$ V and $V_d = 3$ V. Transconductance at both linear ($V_d = 0.1$ V) and saturation ($V_d = 3$ V) regions for devices with $L = 250$ μm are shown in Fig. 3 and 4, respectively. Again the one-step device shows an improvement in maximum transconductance of 6.8 and 4.0% at the linear and saturation regions, respectively. Figure 5 shows $I_d - V_d$ curves for a channel length of 1 μm. The one-step device exhibits 7.7% higher driving current than the control device, both measured at $V_g - V_t = 3$ V and $V_d = 3$ V. It is noted that the I_d improvement was found in both linear and saturation regions. This is an indication that both the interfacial defect
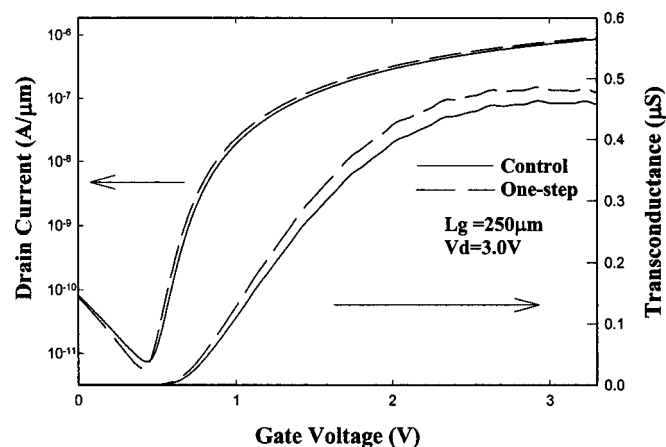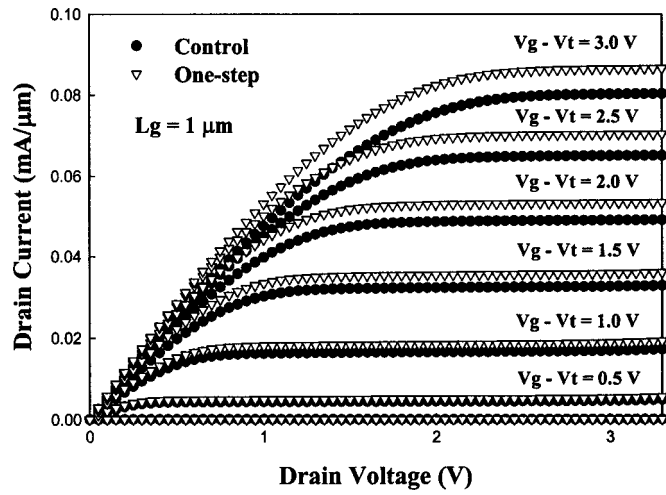

Figure 2. I_d-V_d curves for n-MOSFETs cleaned by standard RCA cleaning processes (control) and the one-step method. Channel length = 250 μm.

Figure 4. Transconductance for n-MOSFETs with 250 μm channel length at saturation region (*i.e.*, $V_d = 3$ V).

Figure 5. I_d-V_d curves for n-MOSFETs cleaned by standard RCA cleaning processes (control) and one-step method. Channel length = 1 μm.
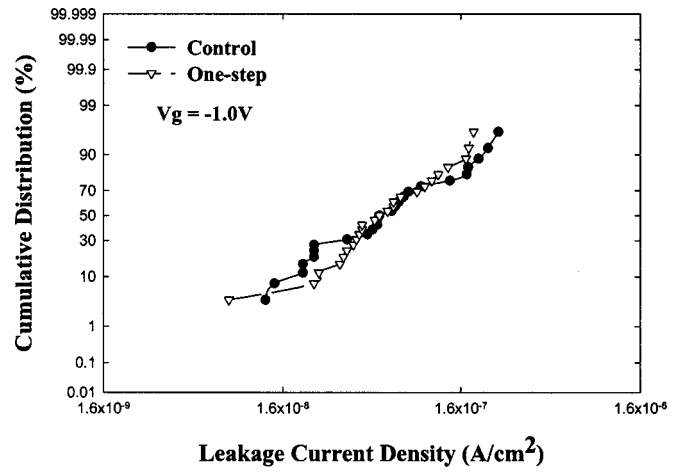

Figure 8. Gate leakage distribution of 25 MOS capacitors. The area is 9×10^{-4} cm^2.

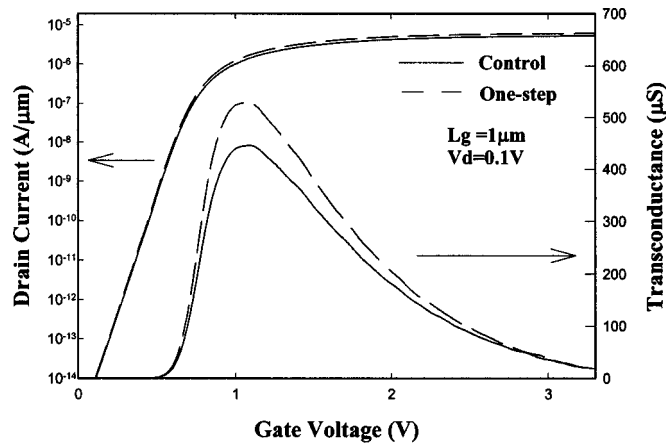**Figure 6.** Transconductance for n-MOSFETs with 1 μm channel length at linear region ($V_d = 0.1$ V).
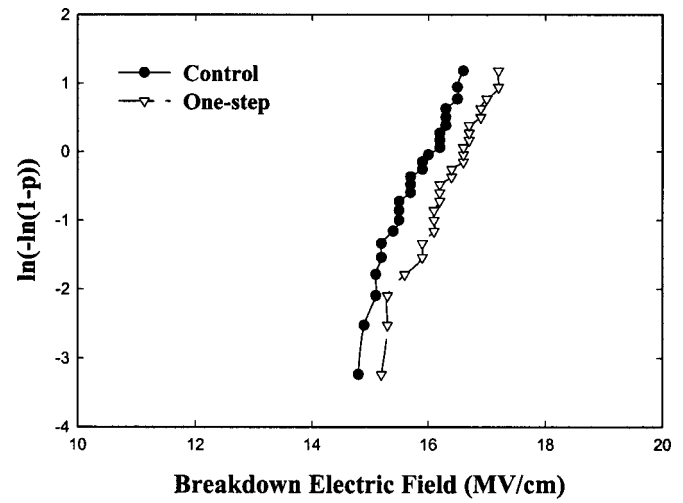

Figure 9. Breakdown filled distribution of 25 MOS capacitors.

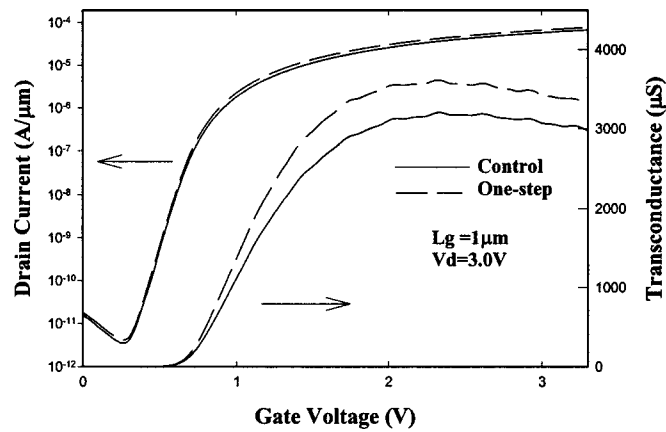**Figure 7.** Transconductance for n-MOSFETs with 1 μm channel length at saturation region ($V_d = 3$ V).
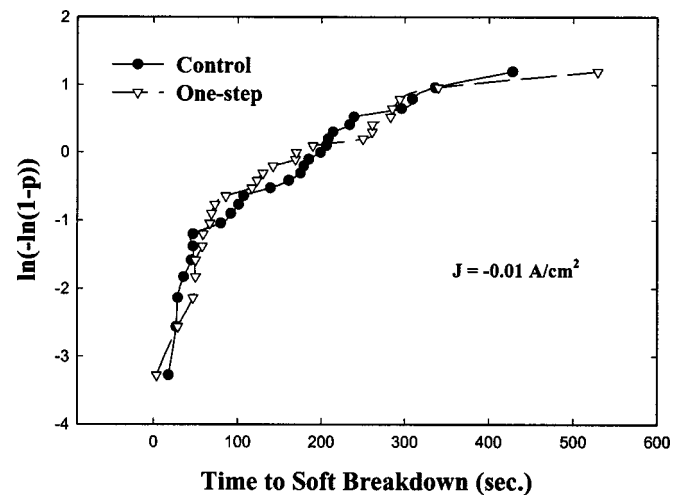

Figure 10. Time-to-soft-breakdown distribution of 25 MOS capacitors.

Figure 11. I_d-V_d curves for n-MOSFETs cleaned by standard RCA cleaning processes (control) and one-step methods in a repeat run. Channel length = 1 μm.

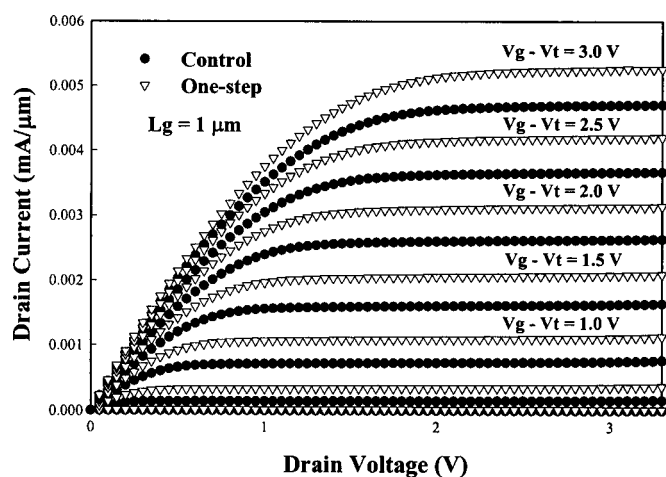**Figure 12.** I_d-V_d curves for n-MOSFETs cleaned by standard RCA cleaning processes (control) and one-step methods in a repeat run. Channel length = 250 μm.

densities (which are strongly related to transconductance in the linear region operation) and the interfacial properties, such as roughness (strongly related to transconductance in the saturation region) both improved. Figure 6 and 7 show the transconductance for the 1 μm devices at linear and saturation regions, respectively. Similar trends are observed. Compared to the 250 μm devices, an even larger improvement (~18.4%) at G_{mmax} is found in the linear region at $V_d = 0.1$, as shown in Fig. 6. The increase in G_m is across the entire gate voltage range. This is due to the cleaner and smoother interface obtained by the new one-step cleaning solution, as we have reported before.[6-8] To confirm this, the surface roughness before gate oxide growth was measured again by AFM. The root-mean-square (rms) value for the control sample is 1.60 Å, while that for the one-step sample is 1.56 Å. The interfacial defect densities (D_{it}), for both samples were measured from 25 MOS capacitors. Samples cleaned by the one-step solution exhibit a lower interfacial defect density (i.e., 2.22×10^{10} cm^{-2} eV^{-1}), compared to that of the control counterparts (i.e., 5.07×10^{10} cm^{-2} eV^{-1}). Subthreshold swing (S.S.), which is strongly related to the interfacial properties,[9] was also measured from the n-MOSFETs, and found to be 80.2 and 81.7 mV/dec for the one-step and control samples, respectively. The smaller S.S. value for the one-step device implies a lower interfacial defect density. From the above results, it is clear that the silicon surface and interface cleaned by the one-step cleaning solution shows improved properties, including a smoother surface and reduced interfacial defect density. These improvements can increase the I_d and G_m of the resultant devices.

Figure 8 shows the gate leakage current measured at 1.0 V for 25 MOS capacitors. The area of the capacitors is 9×10^{-4} cm^{-2}. From the result, the leakage distribution is almost identical for both samples. Breakdown field distribution for these 25 samples is shown in Fig. 9. The one-step devices show a better performance than the control counterparts due to their cleaner and smoother surfaces.
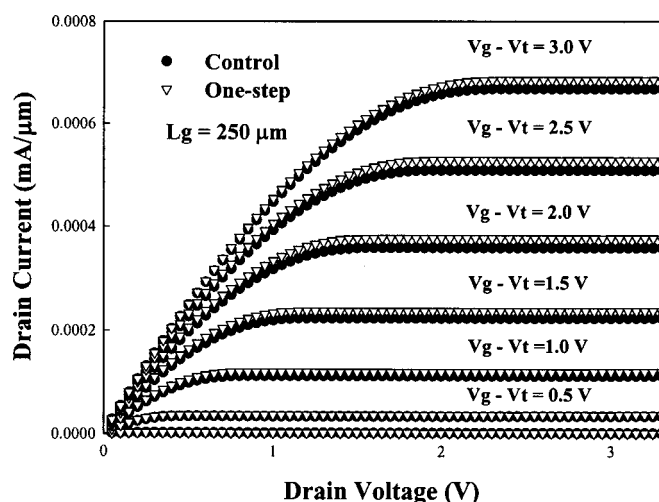
Time-to-soft-breakdown is also measured under constant current stress at $J = -0.01$ A/cm^2, as shown in Fig. 10. Both splits show comparable characteristics. To confirm the above results, a second run was processed and characterized. $I_d - V_d$ curves for devices with short (i.e., 1 μm) and long (i.e., 250 μm) channel in the repeat run are shown in Fig. 11 and 12, respectively. Once again, it is clear that the driving current for the one-step devices is higher than that of their control counterparts.

Another important concern for the interconnect (IC) industry regarding the conventional RCA cleaning process is the required huge amount of DI water consumption. Since two cleaning steps are required in each RCA cleaning process, two DI water rinsing cycles are needed to remove the residual chemicals on the wafer surface. In Table I, we compare the DI water consumption and processing time for both methods. Based on the CMOS logic processes shown in Fig. 1, a CMOS lot requires four different cleaning methods. Each of the four cleaning methods (i.e., clean A, B, C, and D) requires 3, 2, 1, and 1 DI water rinse cycles, respectively, as shown in Fig. 1. In contrast, only one DI water rinsing step is needed when using the one-step cleaning method. A 20 times reduction in DI water rinse cycle is achieved by using the new one-step single-cleaning solution in the CMOS processes. The typical processing time saved for cleaning steps is also estimated and shown in the figure. The total cleaning time required (which includes both cleaning and DI water rinsing times) for clean A, B, C, and D are estimated to be around 60, 40, 20, and 50 min, respectively. The total saving in time is estimated to be around 8.75 h for each lot by adopting the one-step cleaning method.

The overall benefits for this one-step single-cleaning solution method are summarized in Table II. They are (i) reduced equipment cost to one-third as only one bath is required for the one-step cleaning method. (ii) The time for each cleaning step is reduced to one-

Table I. DI water rinsing cycles and processing time for RCA and one-solution cleaning processes.

Rinse cycle by RCA	Rinse cycle by one-step	Rinse cycle difference	Total times in CMOS	Number saved	Processing time by RCA (min)	Processing time by one-step (min)
Clean A: 3	1	2	8	16	60	15
Clean B: 2	1	1	4	4	40	15
Clean C: 1	1	0	6	0	20	15
Clean D: 1	1	0	1	0	50	15

Table II. Advantages of the one-step solution *vs.* the RCA cleaning method.

	RCA	Single-solution	Remarks
Cost of equipment	Expensive foot print	Cheap ($<1/3$), less area, good for minifabrication	Only one bath
Time of cleaning process	Long	Short ($<1/2$)	Average
Cost of H_2O, chemicals, waste handling	High	For 30,000/month (1200 lots), it saves $1200 \times 20 \times 300$ L $= 7.2 \times 10^6$ L/month	20 times H_2O saved in CMOS, 300 L for one cleaning step in 8 in. bath
Processing time of each run	Long	Short	Save 8.75 h for each lot

half to one-third. (*iii*) A huge reduction of the DI water consumption. Take a 30,000 wafer/month process line (which is equivalent to 1200 lot starts per month) for a rough estimation. The DI water saved is as high as $1200 \times 20 \times 300 = 7.2 \times 10^6$ L/month, where 300 L is the typical DI water consumption for an 8 in. lot in one rinsing cycle, and 20 is the reduction number of DI water rinse in each lot as mentioned in Table I. (*iv*) Since the time required for cleaning steps in each run is reduced, the throughput is increased accordingly. More importantly, the chemical waste is also reduced significantly. This is because in the one-step single-cleaning recipe, both HCl and H_2SO_4 are omitted. Since chemical usage is reduced, the IC manufacturing cost is also reduced, which in the long term benefits our environment with reduced chemical use and chemical waste.

Conclusions

In this paper, we have demonstrated a new one-step cleaning recipe for CMOS fabrication. In this method, the one-step single solution is used to replace the conventional RCA two-step cleaning method in the entire CMOS processes. The results of the n-MOSFETs from two split lots show comparable, or even better performance for the new one-step recipe. The potential benefits which are significant for the IC industry include shorter cleaning time, less DI water and chemical usage, and shorter cycle time for CMOS processes. It also benefits our environment by reducing chemical waste.

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