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Analysis and Prevention on NC-ball induced ESD Damages in a 683-Pin BGA Packaged Chipset IC

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Abstract

An abnormal failure mechanism due to ESD zapping on the Non-Connected (NC) balls of a 683-pin BGA packaged chipset IC is presented. Failure analyses, including Scanning Electronic Microscopy (SEM) photographs and the measurement of current waveforms during ESD zapping, had been performed with a new proposed equivalent circuit to give clear explanation on this unusual phenomenon. Several methods to prevent such failure mechanism are also discussed.

1. Introduction

The trend of IC technology is toward smaller device dimension and higher integrated density. The IC packages also make rapid progress toward high pin counts with the increasing numbers of the input/output signals by the trend of more functions integrated in a chip. With the increasing of IC pin counts, the IC product has higher possibility to be damaged by electrostatic discharge (ESD) stresses. In order to improve the whole-chip ESD immunity of IC products, many attentions had been paid on the design and failure analyses of the on-chip ESD protection circuits. But, the relation between ESD damages and the IC packages was seldom discussed. A few reports had shown the package-related ESD issues caused by zapping the Non-Connected (NC) pins [1], [2]. However, there are still no clear analyses or well understanding for this kind of failure mechanism.

In this paper, the event of the adjacent signal balls been damaged when the HBM ESD zapping on NC balls in a 683-pin BGA packaged IC is presented. With a new proposed equivalent circuit, the measurement of ESD current waveforms, and the failure points found by Scanning Electronic Microscopy (SEM), a high correlation between the Small Capacitance Method (SCM) [3] and this failure mechanism can be found. Therefore, clear interpretations of the abnormal failure mechanism have been given with protection solutions to successfully prevent such damages.

2. ESD Damages Induced by NC Balls

2.1. NC Balls in BGA Packaged ICs

The 683-pin BGA packaged chipset IC was fabricated with 0.18μm logic CMOS technology. The cross-sectional view and the top-/bottom-side photographs of the 683-pin BGA packaged IC are shown Figs. 1(a) and 1(b), respectively. The signal or power/ground pads on silicon dice are connected to the solder balls through the Au wires and the traces in the package substrate. NC balls are reserved in the BGA package for further function extension of the next generation products. These NC balls exist only solder balls and short traces in the package

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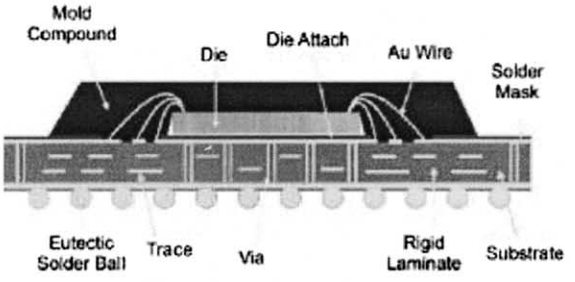
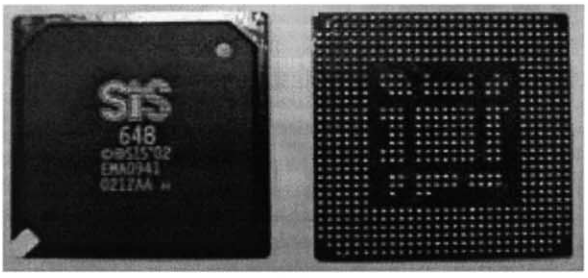
substrate, without bond wires connecting to the dice.



(a)



(b)

Fig.1. (a) The cross-sectional view, and (b) the top-side/bottom-side photographs, of the 683-pin BGA packaged chipset IC product.

2.2. ESD Tests with regards to NC Balls

According to the ESD test standards [4] and [5], these NC balls are currently not necessary to be stressed. But, in real world conditions, the NC balls can be possibly touched by ESD zaps. Thus, these NC balls are treated as signal balls in our ESD qualification procedures. The ESD test results of the BGA packaged IC had been found below HBM 2kV, but above MM 300V. The failure criteria of these IC products are the electrical and function specifications judged by the Auto Test Equipment (ATE). Leakage or short failures had been found in some signal balls of a high-speed data bus. To clarify these failures of signal balls are indeed induced by the NC balls, several sets of ESD test experiments are performed as the following: (1) if only the NC balls are stressed under the ESD test, the leakage or short failures would be found in some of these signal balls that located in the neighbor of the NC balls with HBM level less than 2kV; (2) if ESD stresses been applied on all the balls of the ICs excluding these NC balls, the HBM ESD level of the whole chip can pass 3kV. The results of the MM ESD tests seem not to be influenced by the NC balls. The ESD test results of these ESD test experiments are summarized in Table I. From the results, it has been confirmed that the NC balls really induce the ESD failures of signal balls under HBM ESD stresses.

Table I
The ESD test results of the chipset IC with different stress combinations on the signal or NC balls.

Stress Method	HBM	MM
Stress on all balls	< 2kV	> 300V
Stress only on NC balls	< 2kV	
Stress excluding NC balls	> 3kV	> 300V

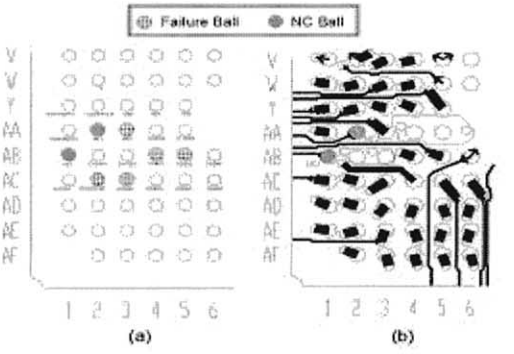


Fig.2. (a) The ball assignment, and (b) the trace layout, of the NC and failure signal balls in the BGA packaged IC.

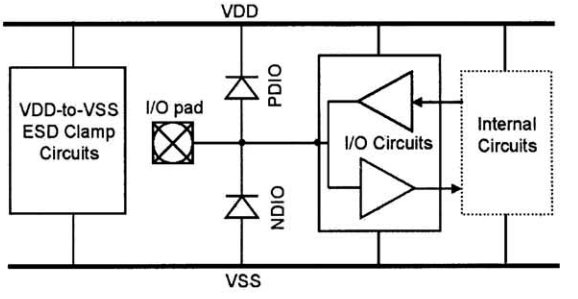


Fig.3. The schematic view of on-chip ESD protection and I/O circuits of the signal balls.

2.3. ESD Failures induced by the NC Balls

The drawing of the ball assignment and the trace layout related to the NC and failure signal balls are shown in Figs. 2(a) and 2(b). As shown in Fig. 2, the failure balls

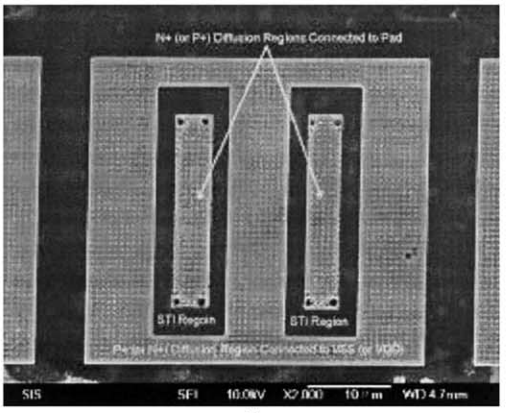
are located around the neighbor of the NC balls, and the minimum space between two adjacent traces is about only 50μm. The schematic view of the ESD protection circuits for these signal balls is shown in Fig. 3. The I/O ESD protection scheme of these signal balls is in the use of the low-capacitance diodes in conjunction with the VDD-to-VSS ESD clamp circuits [6], [7]. The diodes are P+ diffusion in N-well (PDIO) and N+ diffusion in P-well (NDIO) STI-bounded diodes. Figs. 4(a) and 4(b) show the SEM pictures of the failure points of these diodes. Contact destructions of the diodes are found on the boundaries of the diffusion and the STI regions, especially around the corners of the diffusion regions connected to signal pad. Gate ruptures also have been found on the output driving MOS devices, as shown in Fig. 5.

3. Failure Analyses and Protection Solutions

3.1. The Simplified Model and Verification

A simplified equivalent circuit to explain the relationship between the NC and the failure signal balls under HBM ESD stresses is proposed and shown in Fig. 6. The C_{NC}, C_M, and C_S are parasitic capacitors between trace and trace or trace and ground. The capacitor C_{HBM}, resistor R_{HBM}, and the switch S_{HBM} form the equivalent circuit of the HBM ESD tester. For simplicity, only positive voltage polarity applied on the NC ball with respect to the grounded VSS ball is considered in this model. The failure signal ball in this model is floating during the HBM ESD zapping, and the ESD diode is used to stand for the I/O circuits of the signal ball.

During the ESD zapping period, some amount of charges on C_{HBM} will be coupled to C_S through C_M in the way of displacement current. Of course, some of the charges on C_{HBM} will flow through C_{NC} to grounded VSS ball as well. The voltage of C_S will be raised up quickly depending on the value of C_S and C_M. The smaller C_S and the larger C_M will cause the higher voltage on C_S. Moreover, the closer the spacing between the NC and signal traces, the larger capacitance C_M is. The charges stored on C_S will also be discharged by the ESD protection diode through the VSS trace and bonding wire at the same time. The ESD protection diode will be damaged if the energy stored in capacitor C_S exceeds the failure threshold of this kind of mechanism.



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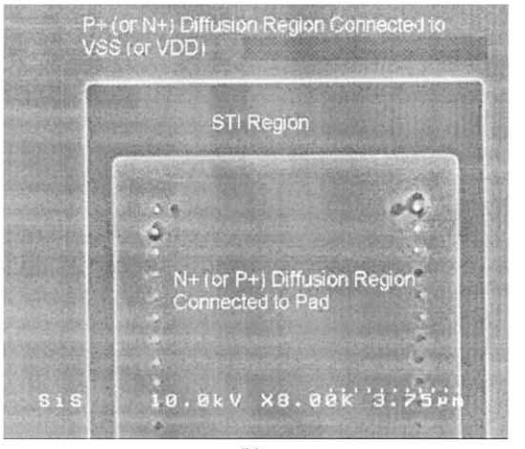


(b)

Fig.4. (a) The SEM picture, and (b) the zoomed-in picture, on the contact destructions of input ESD diodes induced by ESD zapping on the NC balls.

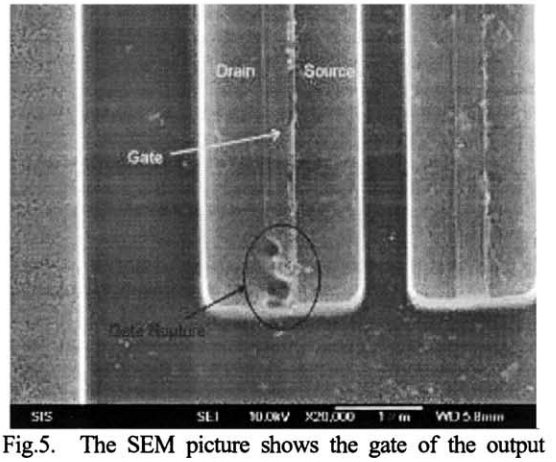


Fig.5. The SEM picture shows the gate of the output driving MOS rupturing due to HBM ESD zapping on the NC balls.

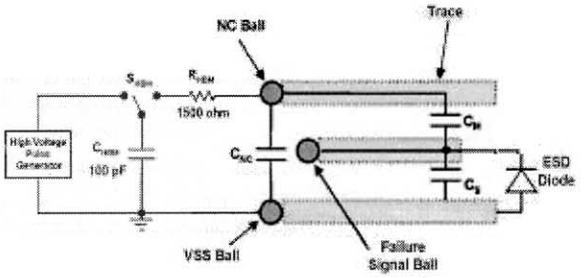
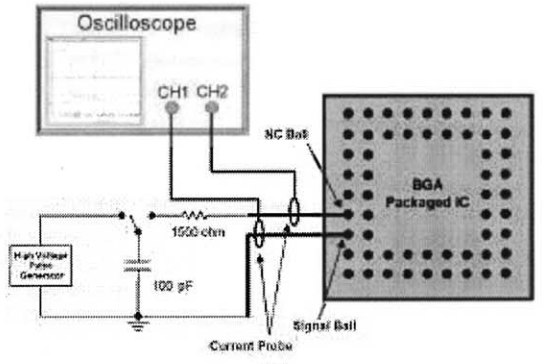


Fig.6. The simplified equivalent circuit proposed to explain the relationship between the NC ball and the failure signal ball under HBM ESD stress.

In order to investigate the possible ESD currents between the NC and signal balls under HBM ESD zaps applied on the NC ball, the experimental setup shown in Fig. 7(a) is performed. To monitor the current waveform of the signal ball, this signal ball is terminated to the ground. The stress voltage applied to the NC ball is +2kV. It was observed that significant current flowing out the grounded signal ball, as that shown in Fig. 7(b). The peak currents measured at the NC ball's input (CH2) and signal ball's output (CH1) were +3.3A and –2.4A, respectively. The negative sign of the current stands for the direction out from the signal ball.



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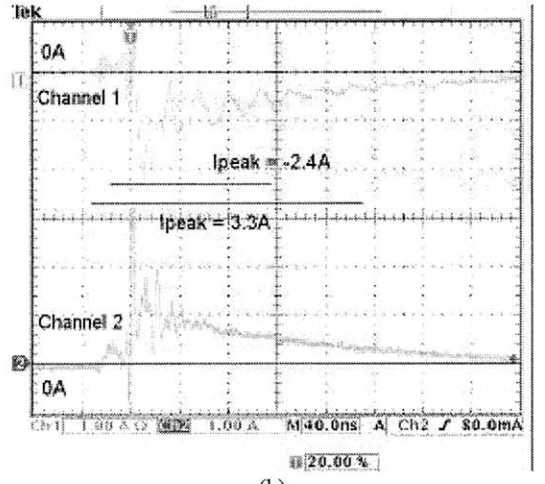
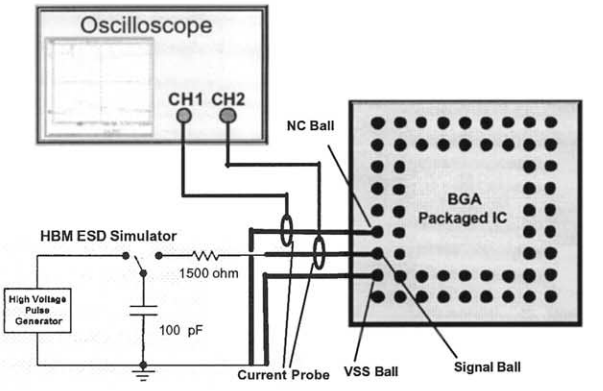
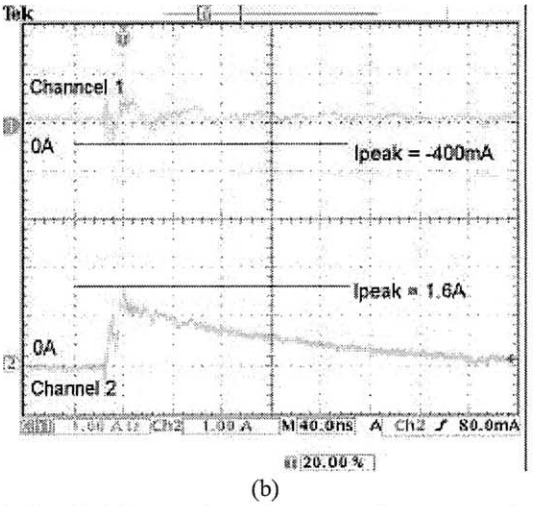


(b)

Fig.7. (a) The experimental setup used to measure the current waveforms between NC and signal balls under HBM ESD zapping on the NC ball with signal ball grounded. (b) The measured current waveforms under HBM 2kV ESD zapping. Channel 1 is the current waveform flowing out the signal ball, and channel 2 is the current waveform flowing in the NC ball.



(a)



(b)

Fig.8. (a) The experimental setup used to measure the current waveforms between NC and signal balls under HBM ESD zapping on the signal ball with VSS and NC balls grounded. (b) The measured current waveforms under HBM 2kV ESD zapping. Channel 1 is the current waveform flowing out the NC ball, and channel 2 is the current waveform flowing in the signal ball.

Another experimental setup provided in Fig. 8(a) is used for comparison with that in Fig. 7(a). The +2kV HBM ESD zap was applied on the signal balls with the VSS ball grounded. The NC ball is connected to the ground for monitoring the current waveform. It was observed that no significant current flowing out the NC ball, as that shown in Fig. 8(b). The peak currents measured at signal ball's input (CH2) and NC ball's output (CH1) were +1.6A and –400mA, respectively.

From the results of above two experiments, it can be proved that a current path exists between the NC and signal balls due to the voltage transient occurring between the parasitic capacitor C_M. In the case of ESD zapping on the NC ball, due to no any other devices can clamp the ESD transient voltage, the current flowing out the signal ball is with a significant high peak current (-2.4A) and a short duration (< 40nsec) in the high current range. In contrast, the small current (-400mA) flowing out the NC ball is observed during the ESD zaps applied on the signal ball, due to the ESD transient voltage been clamped by the I/O ESD protection circuit.

3.2. Correlation with Small Capacitance Method (SCM)

It has been found that the processes of transient ESD current, which charging C_S through C_M and then the charges stored on C_S discharging to the ESD diode under ESD zapping on NC ball, is similar to that of the Small Capacitance Method (SCM) proposed in [3]. The SCM is an ESD evaluation method for the Charged Device Model (CDM). The equivalent circuit of the SCM method is shown in Fig. 9. A 10-pF capacitor is charged by a high voltage supply to such as 1000V, and then discharge to the Device Under Test (DUT) through a very low impedance path. The current waveform and failure modes of DUT due to the SCM are found similar to that of CDM [3]. Both the current waveform of SCM and CDM are with high peak current, fast rise time, and short discharging duration. The failure modes induced by SCM reported in [3] are mainly junction destructions (energy destruction) around the contacts, or the ruptures of the gate oxide (electric-field destruction), due to localized heat dissipation or high transient voltage caused by its discharging current waveform. Although the parasitic capacitor C_S may not be 10pF as that in the SCM method, the comparison of failure points induced by the NC ball and SCM between Figs. 10(a) and 10(b) shows a high similarity.

3.3. Protection Solutions

From the many ESD test results and failure analyses, two directions to prevent ESD damages induced by NC ball are list as below. According to these two directions, several methods are proposed to solve this NC-ball induced problem.

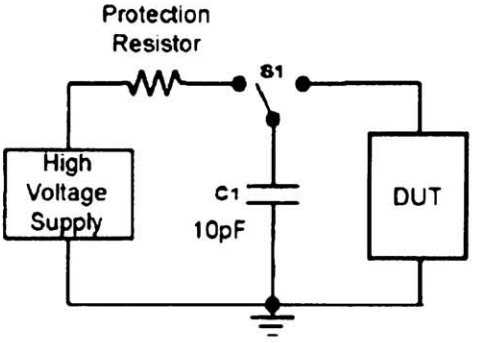


Fig.9. The equivalent circuit of the Small Capacitance Method (SCM) proposed in [3], which is used as an evaluation method for the CDM ESD test.

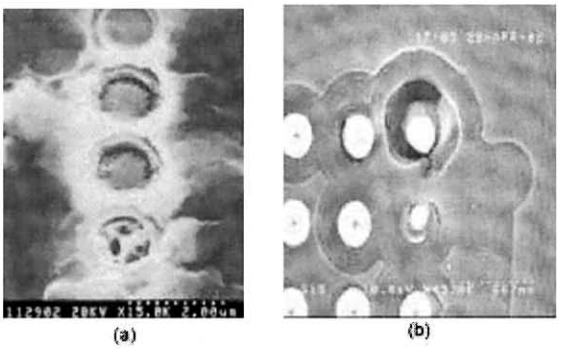


Fig.10 (a) The SEM picture of the junction destruction induced by SCM from [3]. (b) The SEM picture of the junction destruction induced by HBM ESD zapping on the NC ball.

(1). Reducing the Voltage or Charges Coupled to C_S under ESD Zapping Condition: Reducing the voltage or charge coupled to C_S means to reduce the energy stored in C_S that may cause damages on the signal balls. From the simplified equivalent circuit shown in Fig. 6, by increasing the capacitance of C_{NC} or decreasing the capacitance of C_M can reducing the voltage or charge coupled to C_S under the ESD zapping conditions. Inserting the VDD or VSS guard traces around the NC ball and its trace is an efficient way to prevent the ESD damages induced by the NC ball. Separating the NC ball and its trace far away from other signal balls is also a way to increase the failure threshold of the NC ball induced ESD damages. The most efficient way to reduce the voltage or charges coupled C_S is directly

connected the NC ball to VDD or VSS in the package through traces of bond wires, but it is not NC ball anymore. In fact, by using the VDD or VSS guard traces, the ESD immunity of the high-pin-count BGA packaged IC has been improved to above HBM 3kV. This direction also makes it reasonable that the ESD immunity of MM (> 300V) is not affect by the NC balls, because of the stressing voltage of MM is not as high as HBM to give enough energy on C_S to destroy the signal ball.

(2). Improving the Current Conduction Efficiency of ESD Devices under High Peak and Fast Transient Condition: Due to the high peak current and fast transient of the current waveform induced by the ESD zapping on NC ball, most energy will be dissipated in a short duration of time and the current will be crowded in some limited areas of the ESD diodes which with the minimum resistance. As shown in Fig. 4, the contact destructions of the ESD diodes are located on the boundaries of the diffusion and STI regions, especially on the corners. These ESD diodes can sustain above 3kV HBM and above 300V MM ESD stresses, but fails on the NC ball induced event during 2kV HBM ESD stress. Because the discharge durations of the HBM and the MM are much longer than this NC ball induced event, and the ESD diodes in conjunction with the VDD-to-VSS ESD clamp circuit can conduct the ESD current, efficiently.

To make the ESD diodes more efficient to discharge the high-peak and fast-transient current pulse, the layouts of the ESD diodes are suggested in the finger style to obtain the longer perimeters with a lower turn-on resistance.

4. Conclusion

Although according to the ESD test standards, the NC balls are not necessarily stressed, we still treat these NC balls as signal balls under ESD tests for more strict reliability assurance. An abnormal ESD failure mechanism due to HBM ESD zapping on the NC balls of a high-pin-count BGA packaged IC has been presented. The failure modes of this mechanism are junction destructions and gate-oxide ruptures of the signal balls around the neighbor of the NC balls. With the proposed equivalent circuit, the measurements of ESD current waveforms and the failure points found by SEM, high correlation has been found between the NC ball induced ESD damages and the SCM method. This gives a reasonable interpretation for the abnormal failure mechanism. According to the failure analyses, two directions including effective solutions have been provided to prevent such abnormal failures. One of the solutions has been used in the BGA packaged IC product to successfully improve the ESD immunity above 3kV HBM and 300V MM.

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