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Analysis and design of a new SRAM memory cell based on vertical lambda bipolar transistor

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Abstract

A voltage-controlled negative-differential-resistance device using a merged integrated circuit of two n-channel enhancement-mode MOSFETs and a vertical NPN bipolar transistor, called vertical Lambda-bipolar-transistor (VLBT), is presented for memory application. The new VLBT structure has been developed and its characteristics are derived by a simple circuit model and device physics. A novel single-sided SRAM cell based on the proposed VLBT is presented. Due to the characteristics of the VLBT, it offers better static noise margin and larger driving capability as compared with conventional single-side CMOS memory cell.

Keywords: Negative-differential-resistance; Lambda-bipolar-transistor; SRAM

1. Introduction

Over the past years, a variety of semiconductor devices had been reported to exhibit negative-differential-resistance phenomenon. The negative-differential-resistance or the folded $I-V$ characteristics of devices makes it possible to have the multiple stable states with good margins in a simple circuit consisting of just a few devices. This fact was recognized by several researchers and several compact multiple-valued storage functions have been described in the literature [1,2]. Wu and Wu [3] had presented another voltage-controlled negative-differential-resistance device, called Lambda bipolar transistor (LBT), which merges a NMOS with a bipolar transistor. The LBTs, in particular, had shown clear voltage-controlled negative-differential-resistance characteristics, which is advantageous for functional circuit applications [4,5]. Ref. [4] has been shown to have limitations due to the requirement of precharging the bit line to prevent destructive readout and due to slow recovery of the stable state after reading. Moreover, planar-structure LBTs has also been realized to meet the demand for high-level integration.

In this paper, a new LBT, which exhibits λ-type voltage-controlled negative differential-resistance characteristics, will be analyzed. The new LBT has three terminals (emitter, base, collector) which is similar to those of a conventional bipolar transistor except that an additional same carrier type MOSFET should be merged, in order to produce the voltage-controlled differential-negative-resistance. Based on the new device, we propose and demonstrate a single-sided low-power SRAM memory cell. The new cell consists of five MOSFET devices and one parasitic bipolar transistor so that the cell area is smaller than the conventional CMOS static memory cell, which comprises six MOSFET devices. The detailed description of the device operation and the mechanism controlling the negative differential resistance are given in Section 2 of this paper, where the first-order device theory will be developed. In Section 3, a new SRAM memory cell using the new LBT device will be described. Simulation results and comparisons will be made in Section 4. Conclusions is given in Section 5.

2. Device physics and modeling

The basic structure of the new LBT and its electrical equivalent circuit connection are shown in Figs. 1 and 2, respectively. From Fig. 1, the n-channel enhancement-mode MOSFETs are fabricated upon the base region of a vertical

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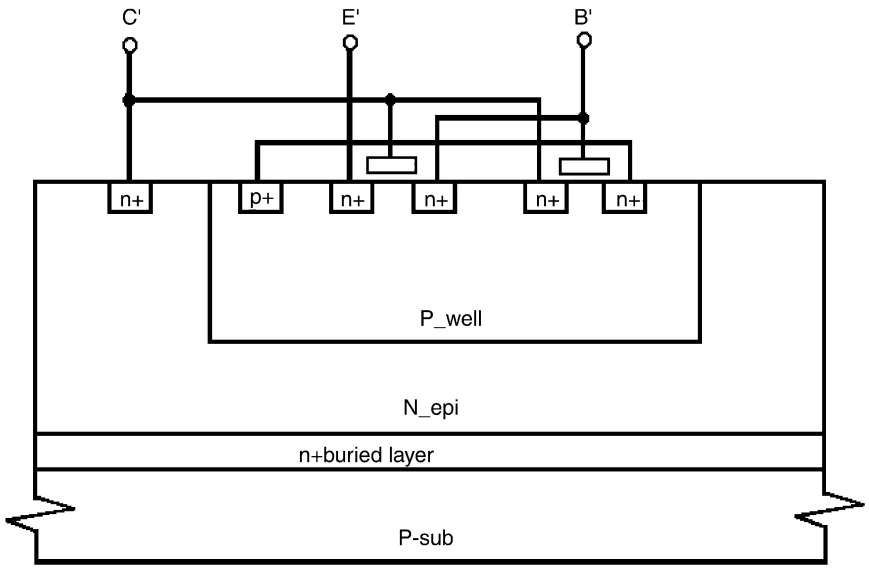

Fig. 1. A VLBT structure.

NPN bipolar transistor, which is called the vertical Lambda bipolar transistor (VLBT). The source of one of the MOSFETs (labeled as E′) is utilized as the emitter of the vertical NPN bipolar transistor, while the p-type diffusion well and the n-type epi-layer act as the base and the collector, respectively.

The VLBT is operated in the same way as the conventional bipolar transistor with a fixed external base current. From the terminal characteristics of the separate devices, the general equations for the proposed VLBT, according to the circuit model of Fig. 2, can be written as

$$I_{B'}=\begin{cases} K_1\left[(V_{C'E'}-V_{T1})V_{B'E'}-\dfrac{V_{B'E'}^2}{2}\right], & \text{if } (V_{C'E'}-V_{T1})>V_{B'E'} \\ \dfrac{K_1}{2}(V_{C'E'}-V_{T1})^2, & \text{if } (V_{C'E'}-V_{T1})<V_{B'E'} \end{cases} \tag{1}$$

where $K_1=C_{ox}\mu_n W_1/L_1$ and V_{T1} is the threshold voltage of M_1.

$$I_{C'}=I_C+I_B \tag{2}$$

$$I_B=\begin{cases} K_2\left[(V_{B'E'}-V_{T'})(V_{C'E'}-V_{BE'})-\dfrac{(V_{C'E'}-V_{BE'})^2}{2}\right], & \text{if } (V_{B'E'}-V_{T2})>V_{C'E'} \\ \dfrac{K_2}{2}(V_{B'E'}-V_{T'})^2, & \text{if } (V_{B'E'}-V_{T2})<V_{C'E'} \end{cases} \tag{3}$$

where $K_2=C_{ox}\mu_n W_2/L_2$, V_{T2} is the threshold voltage of M_2, and $V_{T'}=V_{T2}+V_{BE'}$.

$$I_C=\beta I_B+I_{CO}(1+\beta) \tag{4}$$

where β is the dc common-emitter current gain of the NPN bipolar transistor, and $I_{CEO}=I_{CO}(1+\beta)$ is the common-emitter collector reverse saturation current.

A certain current source load M_3 operated in saturation region is chosen for derivation. The current equation can be written as

$$I_{B'}=\frac{K_3}{2}(V_{GG}-V_{B'E'}-V_{T3})^2 \text{ for } V_{GG}>(V_{B'E'}+V_{T3}) \tag{5}$$

where $K_3=C_{ox}\mu_n W_3/L_3$, V_{T3} is the threshold voltage of M_3 and the V_{GG} is the power supply connected to the drain of the M_3.

In order to get analytical expressions, the body effects are assumed to be negligible. To see the quantitative operational principles of a VLBT shown in Fig. 3, the six-region analyses are given as follows:

Region I. If $V_{C'E'}<V_{BE'(on)}<V_{T1}$, M_1 is off, M_2 is operated in linear region, and Q_1 is off. In this region, $I_B=0$, thus $I_{C'}=I_{CO}(1+\beta)$.

Region II. If $V_{BE'(on)}<V_{C'E'}<V_{T1}$ and $V_{B'E'}=V_{GG}-V_{T3}-K\lfloor\sqrt{2\phi_{fp}+V_{B'E'}}-\sqrt{2\phi_{fp}}\rfloor>V_{T'}$ (where K is the modifying substrate factor), M_1 is off, M_2 is kept in linear region, and Q_1 is operated in forward-active region. By solving $V_{B'E'}$, i.e.

$$V_{B'E'}=\left(V_{GG}-V_T+K\sqrt{2\phi_{fp}}+\frac{K^2}{2}\right)+K\left(V_{GG}-V_T+K\sqrt{2\phi_{fp}}+\frac{K^2}{4}+2\phi_{fp}\right)^{1/2} \tag{6}$$

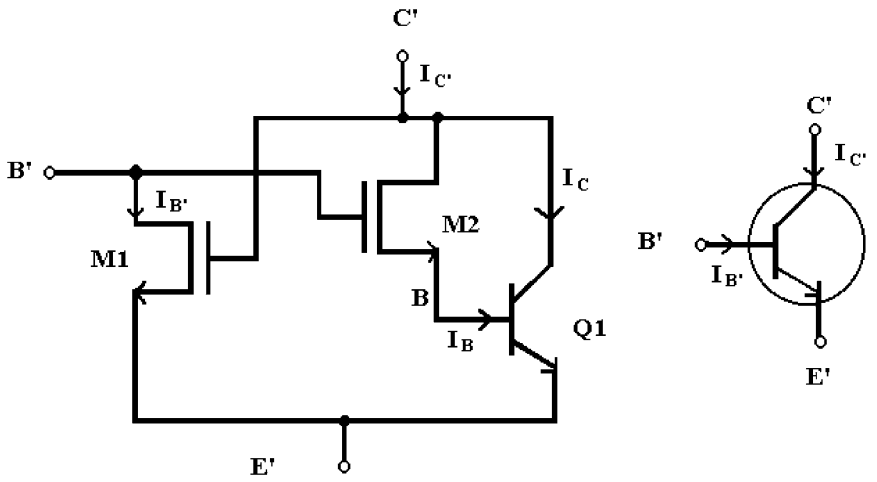

Fig. 2. An equivalent circuit of a VLBT.

we get the output current in this region:

$$I_{C'} = (1+\beta)\left[K_2\left[\left(\left(V_{GG} - V_T + K\sqrt{2\phi_{fp}} + \frac{K^2}{2}\right) \times K\sqrt{\left(V_{GG} - V_T + K\sqrt{2\phi_{fp}} + \frac{K^2}{4} + 2\phi_{fp}\right)} - V_{T'}\right) \times (V_{C'E'} - V_{BE'}) - \frac{(V_{CE'} - V_{BE'})^2}{2}\right] + I_{CO}\right] \quad (7)$$

Region III. If $V_{T1} < V_{C'E'} < V_{B'E'} - V_{T2}$ and assuming that $V_{B'E'} > V_{T'}$, M_1 is operated in saturation region, M_2 is kept in linear region, and Q_1 is still in forward-active region. Solving $V_{B'E'}$ by equating (1) and (5), we obtain

$$V_{B'E'} = V_{GG} - \sqrt{\frac{K_1}{K_3}}(V_{C'E'} - V_{T1}) - V_{T3} \quad (8)$$

and the output current in this region is

$$I_{C'} = (1+\beta)\left[K_2\left[V_{GG} - \sqrt{\frac{K_1}{K_3}}(V_{C'E'} - V_{T1}) - V_{T3} - V_{T'}\right] \times (V_{C'E'} - V_{BE'}) - \frac{(V_{C'E'} - V_{BE'})^2}{2} + I_{CO}\right] \quad (9)$$

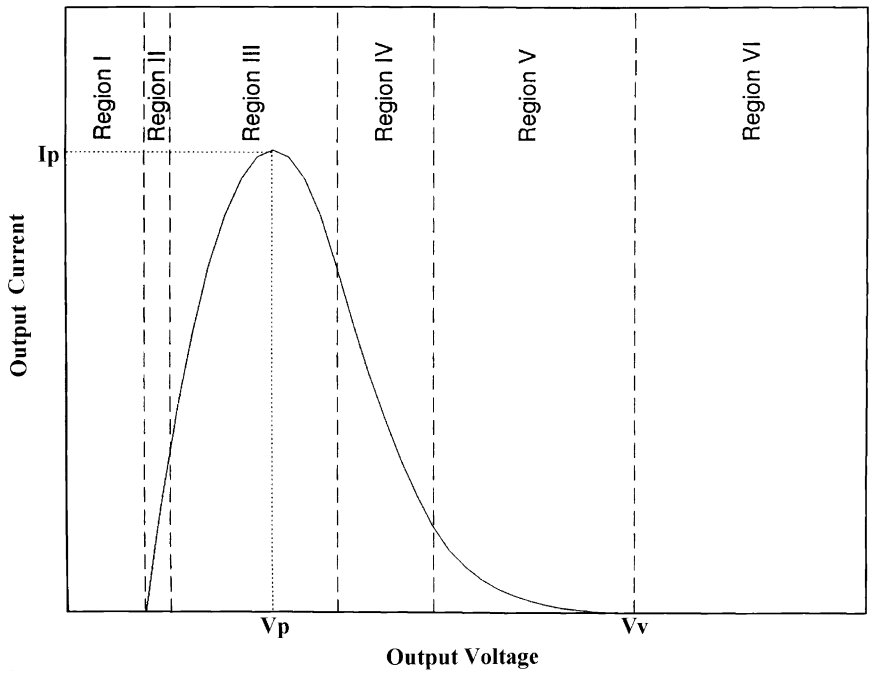

Fig. 3. The $I-V$ characteristics of a VLBT.

The peak current is $I_P = I_{C'|V_{B'E'}=V_P}$, where the peak voltage V_P can be derived by letting $\partial I_{C'}/\partial V_{C'E'} = 0$, i.e.

$$V_P = \frac{K_3(V_{GG} - V_{T2} + V_{T3}) + \sqrt{K_1 K_3}(V_{BE'} + V_{T1})}{K_3 + 2\sqrt{K_1 K_3}} \tag{10}$$

Region IV. If $V_{B'E'} - V_{T2} < V_{C'E'} < V_{B'E'} + V_{T1}$ and $V_{B'E'} > V_{T'}$, M_1 and M_2 are both operated in saturation region, and Q_1 is operated in forward-active region. Using Eqs. (1), (2), (4), and (8), we obtain

$$I_{C'} = (1+\beta)\left[\frac{K^2}{2}\left(V_{GG} - \sqrt{\frac{K_1}{K_3}}(V_{C'E'} - V_{T1}) - V_{T3} - V_{T'}\right)^2 + I_{CO}\right] \tag{11}$$

By differentiating Eq. (9) with respect to $V_{C'E'}$, the output resistance in this region can be written as

$$R_O = \frac{-1}{(1+\beta)K_2\sqrt{\frac{K_1}{K_3}}\left[V_{GG} - \sqrt{\frac{K_3}{K_1}}(V_{C'E'} - V_{T1}) - V_{T3} - V_{T'}\right]} \tag{12}$$

Region V. When $V_{C'E'} > V_{B'E'} + V_{T1}$, M_1 is operated in linear region and M_2 is operated in saturation region. Assuming $V_{B'E'} > V_T$, Q_1 is operated in forward-active region. The output current is

$$I_{C'} = (1+\beta)\left[\frac{K_2}{2}(V_{B'E'} - V_{T'})^2 + I_{CO}\right]$$

Solving Eqs. (1) and (5), gives

$$V_{B'E'} = \frac{K_1(V_{C'E'} - V_{T1}) + K_3(V_{GG} - V_{T3})}{K_1 + K_3} - \frac{[[K_1(V_{C'E'} - V_{T1}) + K_3(V_{GG} - V_{T3})]^2 - K_3(K_1 + K_3)(V_{GG} - V_{T3})^2]^{1/2}}{K_1 + K_3} \tag{13}$$

By a chain rule, we have the output resistance

$$R_O = \frac{1}{\frac{\partial I_{C'}}{\partial V_{B'E'}}\frac{\partial I_{B'E'}}{\partial V_{C'E'}}} = \frac{1}{(1+\beta)K_2(V_{B'E'} - V_{T'})(K_1 + K_3)} \times\left[K_1 - \frac{2K_1[K_1(V_{C'E'} - V_{T1}) + K_3(V_{GG} - V_{T3})]}{2[[K_1(V_{C'E'} - V_{T1}) + K_3(V_{GG} - V_{T3})]^2 - K_3(K_1 + K_3)(V_{GG} - V_{T3})^2]^{1/2}}\right] \tag{14}$$

The valley voltage V_v can be obtained by solving $V_{B'E'}(V_{C'E'}) = V_{T'}$, i.e.

$$V_v = \frac{K_3(V_{GG} - V_{T'} + V_{T3})^2 + K_1(V_{T'}^2 + 2V_{T'}V_{T1})}{2K_1 V_{T'}} \tag{15}$$

Region VI. When $V_{C'E'} > V_v$, M_1 is still operated in linear region, M_2 and Q_1 are both off. Thus, $I_B = 0$ and $I_{C'} = I_{CO}(1+\beta)$.

3. A new memory cell

The general configuration of the proposed static random access memory cell is shown in Fig. 4, which consists of a VLBT, a load element, a current source device, and an access transistor. Owing to the negative-differential resistance of VLBT, the storage node SN has two dc static points (Fig. 5). Two kinds of load elements, current-source-like and resistance-like, can be selected for different applications. For a current-source-like load, the current flow at the static points S_{C1} and S_{C2} can be both small if the circuit is well-configured. On the contrary, a resistance-like load memory cell generally suffers dc current flow at the lower static state S_{R2}. However, it occupies a relative smaller area as compared with a current-source-like load one.

The new memory cell based on the proposed VLBT is presented in Fig. 6. In memory cell configuration, M_1, M_2 and Q_1 operate as a VLBT storage element, M_3 acts as a current source, M_4 acts as the load element, and M_5 is the access transistor. When V_X is in the low stable-state S_{C1}, any positive noise causes V_X to increase slightly. At this moment, $I_{C'}$ is larger than I_{DS4} so that V_X discharges to S_{C1}. If any negative noise causes V_X to reduce a little, the fact that I_{DS4} is larger than $I_{C'}$ will cause V_X to be charged to S_{C1}. Previous description demonstrates why this state is stable. The same argument can apply to the state S_{C2} to verify this state to be stable.

If any positive noise is introduced as V_X in the switching state S_W, the positive differential current $I_{DS4} - I_{C'}$ will charge the node X to the high stable state S_{C2}. The memory cell no longer stays in the state S_W. On the other hand, if negative noise is introduced as the memory cell is in the state S_W, a negative differential current $I_{DS4} - I_{C'}$ makes the node X to be discharged to S_{C1}. Both types of noise (positive and negative) cause a transition from the state S_W to either the stable state S_{C1} or S_{C2}. The stored voltage levels are CMOS like, i.e. full swing between ground and supply voltage is obtained.

Fig. 7 shows the static noise margin (SNM) comparison between our new memory cell and the proposed [5], which is referred to as LBT configuration. The voltage of storage

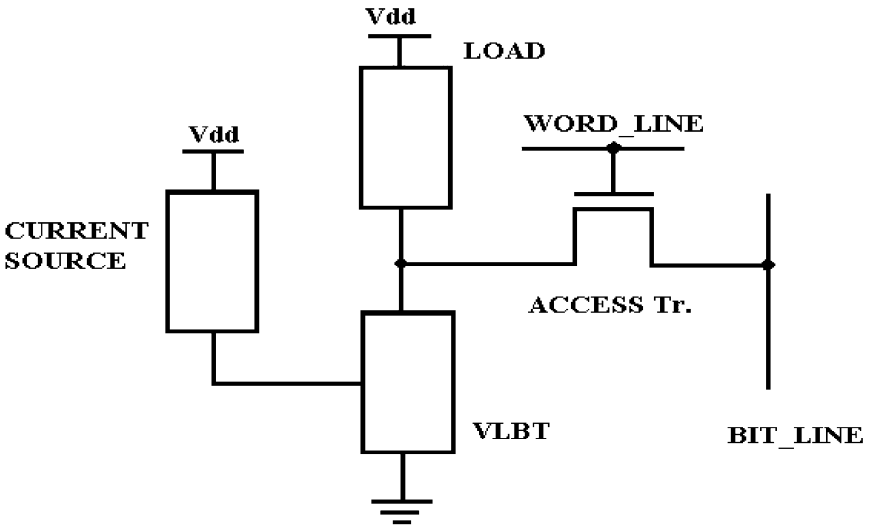

Fig. 4. General configuration of a new memory cell.

node at any instant is the base–emitter voltage in LBT configuration, hence is always less than 1 V. The SNM of the new memory cell (VLBT) and the LBT configuration are about 1.2 and 0.4 V, respectively. The new memory cell has the larger SNM than LBT configuration. It also shows that LBT configuration requires adequate circuit to sense the state of the cell, because the switch point of the LBT configuration is less than 1 V.

4. Simulation results and comparisons

Extensive circuit simulations have been carried out to verify the circuit operation and the characteristics of performance. The performance of the proposed circuit is evaluated based on 5 V 0.5 μm BiCMOS technology. The simulation results are based on 1 ns rise and fall time.

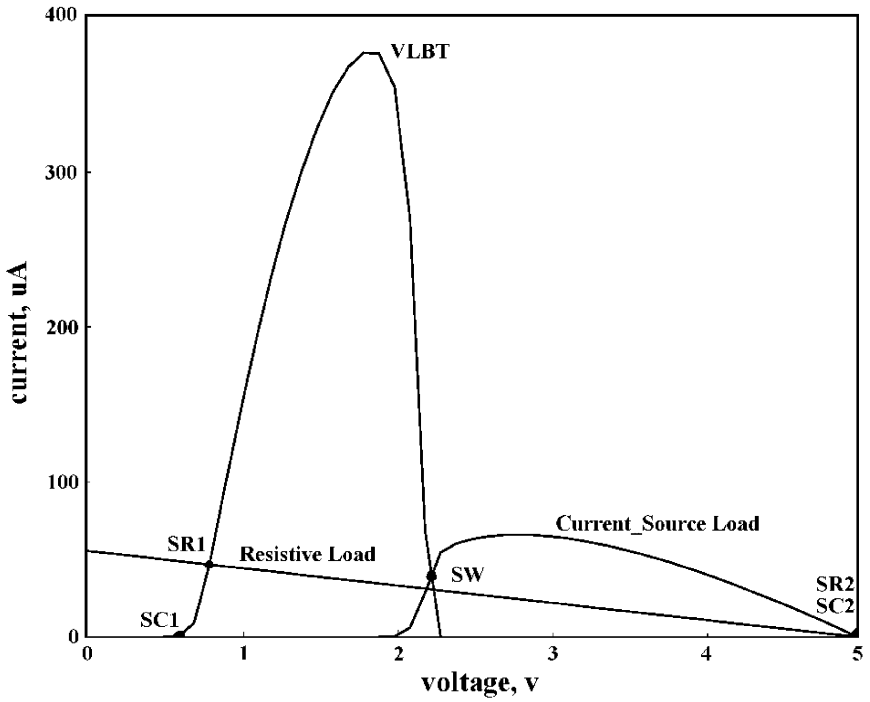

Fig. 5. The $I-V$ characteristics of a new memory cell with current and resistive load.

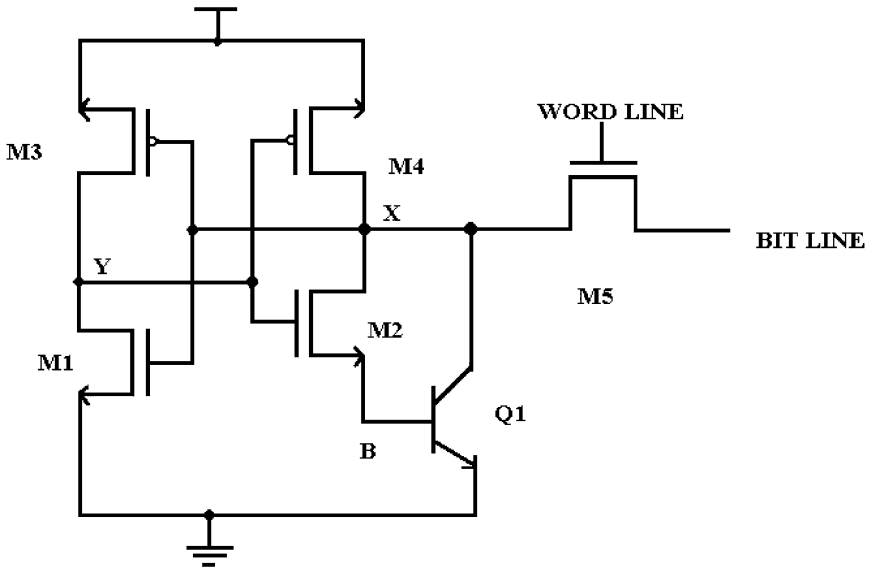

Fig. 6. A new SRAM memory cell circuit.

4.1. Write operation

In the static memory cell, the write operation is performed by forcing high and low voltage to the bit-line. The operation cycles start at 3 ns, turning on the access transistor M_5 by a word-line pulse with 1 ns rise time.

When changing the binary state of the memory circuit from 1 to 0, the voltage level of node X rapidly decreases. Because the transistor M_1 is turned off and the transistor M_2 and Q_1 are turned on, the internal capacitor of node Y is charged very fast via the transistor M_3. The simulation result is shown in Fig. 8. Changing the binary state from 1 to 0 just takes about 0.5 ns.

When changing the binary state from 0 to 1, the voltage level of node X increases very fast due to the fact that the current through the transistor M_4 is increased. But with increasing the node voltage V_x,

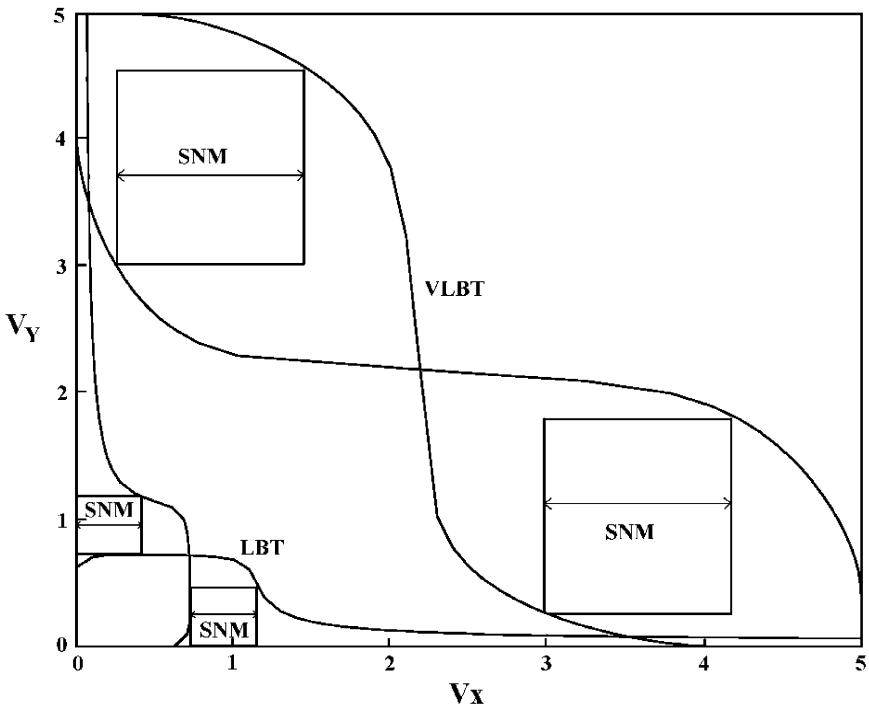

Fig. 7. The static transfer characteristics of the memory cells.

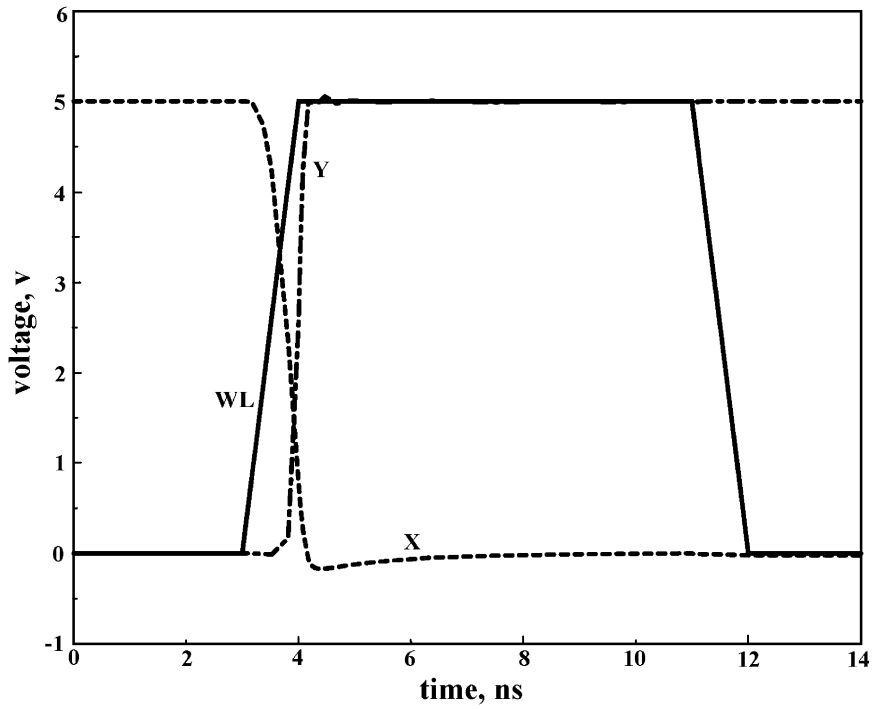

Fig. 8. Write '0' operation.

the access transistor as well as the transistor M_3 are turned off. Now, the internal capacitor of node X is charged more slowly via the load transistor M_4. The simulation result is shown in Fig. 9. Changing the binary state from 1 to 0 just takes about 1.5 ns.

4.2. Read operation

The stored data of a memory cell selected by the word-line and the column decoder has to be read non-destructively. For the read operation, the bit-line capacitor

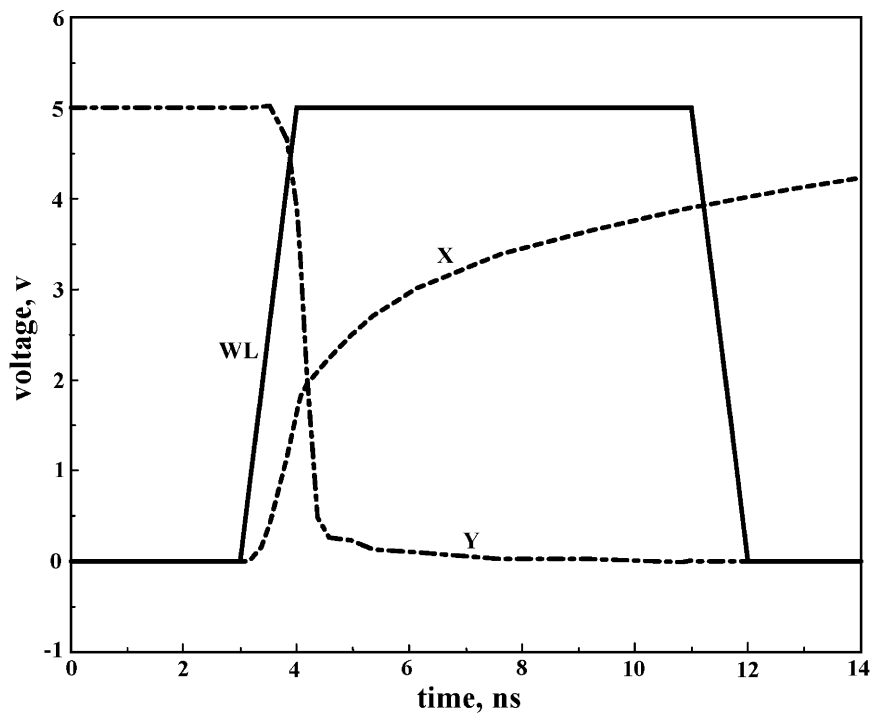

Fig. 9. Write '1' operation.

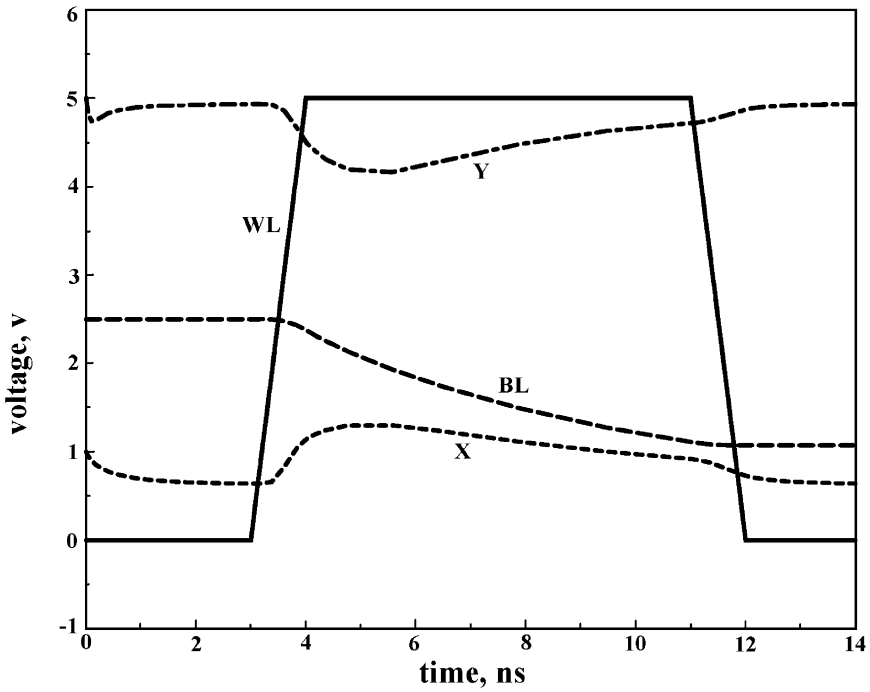

Fig. 10. Read '0' operation.

C_{BL} is precharged to the reference voltage level V_{ref} and then is left floating. The bit-line voltage versus time during the reading cycle is calculated by assuming that the memory cell has to charge a bit-line capacitor C_{BL} of 1 pF.

Reading a binary 0, the bit-line capacitor has to be discharged via the transistor Q_1. The current flowing from the bit-line into the circuit should be low enough so that the voltage level of node X does not cross the switching point S_W. This current will increase with an increasing precharge voltage level on the bit-line. It means that the precharge voltage has an upper limiting voltage. For a precharge voltage level higher than the upper limiting voltage, the circuit becomes unstable and switches into the opposite binary state. The information in the memory cell

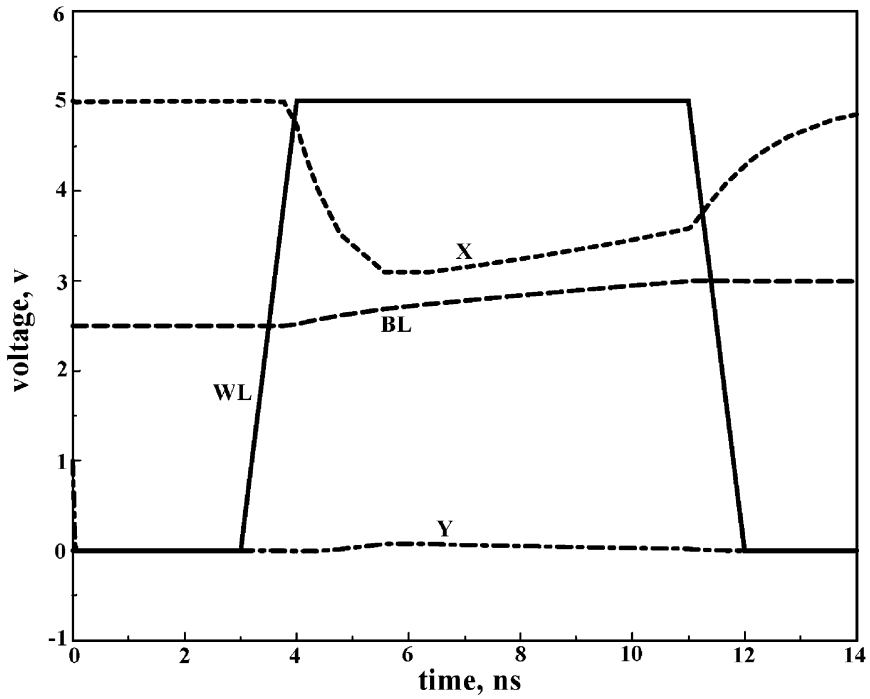

Fig. 11. Read '1' operation.

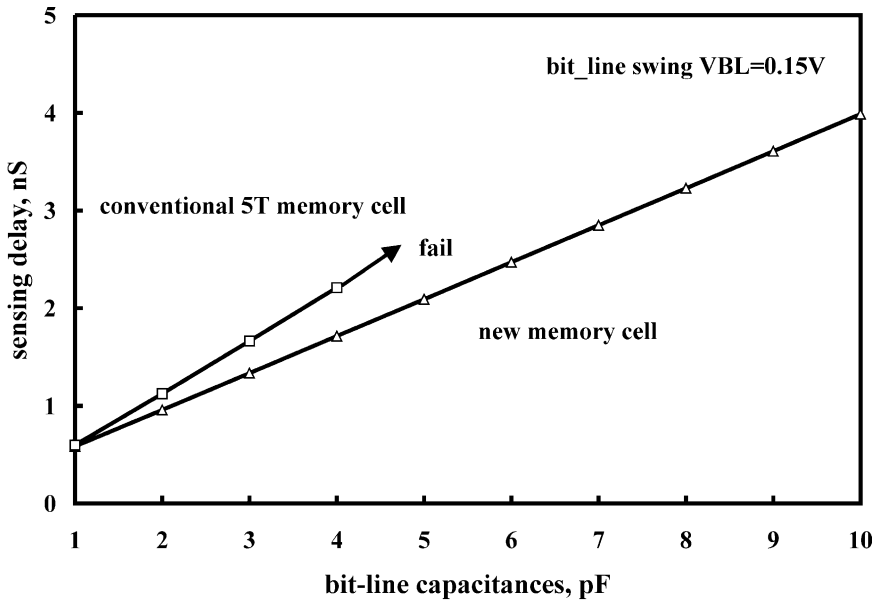

Fig. 12. Sensing delay versus bit-line capacitance.

will then be destroyed during readout. The reading '0' operation is shown in Fig. 10.

Reading a binary 1, the bit-line capacitor is charged via the transistor M_4. The load current will cause the node voltage V_x to full. To avoid the voltage level of node X crossing the switching point S_W, the load current level should be higher. Therefore, during reading a binary 1, the precharge voltage level has a lower limiting voltage. The reading '1' operation is shown in Fig. 11.

4.3. Comparisons

Fig. 12 shows comparisons of the transient analysis of read '0' operation with respect to different load capacitances on the bit-line. Since the bipolar transistor is operated from cut-in to forward-active region, the proposed memory cell does not make too much difference on the delay time from conventional single-side CMOS memory cell for a small bit-line capacitance. However, for a large bit-line capacitance, the proposed memory cell is greatly superior to the conventional one because its large cell current. What can be noted is that for a heavily loaded bit-line, the conventional memory is destructively read, i.e. its storage state is changed from '0' to '1' after read operation. On the contrary, the proposed memory cell maintains its trend on delay time toward a bit-line capacitance. That is, because the charge required for changing the state of the proposed cell from '0' to '1' is relatively large as compared with the conventional one, which is important for non-destructive read operation.

5. Conclusions

In this paper, a new VLBT for low-power memory application has been studied and characterized. It is obtained by merging two n-channel enhancement-mode MOSFETs with a vertical bipolar transistor in a new way. It could be noted that, the n + buried layer is utilized to reduce the collector resistance of the vertical bipolar transistor. Thus, it is an option with respect to various integrated circuit fabrication processes.

A novel single-sided static random access memory cell based on the new VLBT is also studied. Due to the characteristics of the VLBT, it offers better noise margin and larger driving capability as compared with a conventional single-side CMOS memory cell.

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