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DSP implementation of successive interference cancellation (SIC) receiver for 3GPP WCDMA uplink transmission‡

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Summary

The 3GPP WCDMA is a widely accepted third-generation cellular system standard. By using nonorthogonal codes for different users, the multiple access interference (MAI) can be a limiting factor for system performance, as for other CDMA systems. Multiuser detection (MUD) is known to reduce MAI and improve CDMA system performance, but many such techniques have high complexity. Successive interference cancellation (SIC) is an effective MUD technique with relatively low complexity. We consider the software implementation of an SIC receiver for WCDMA uplink transmission on a commercially available general-purpose multi digital signal processor (DSP) platform. This also goes in line with the recent interest in software-defined radio. Issues addressed in this work include job partitioning and signal routing for multiprocessor implementation, design of SIC components (especially the channel estimator and the signal regenerator), determination of the precision of fixed-point computations, consideration of the receiver's error performance and analysis of the implementation's complexity and efficiency. These issues are tightly coupled with the 3GPP WCDMA specifications. Because the employed platform only contains four DSPs, the implementation only considers up to three users. But this is sufficient for us to appreciate various DSP implementation issues of an SIC receiver. Moreover, by the nature of SIC, it is easy to extend the implementation to handle more users with an enlarged platform. Our present implementation achieves real-time speed in the RAKE receiver part of the complete receiver. Due to the complexity in signal regeneration, the overall SIC receiver still falls short of the real-time requirement when interference cancellation is activated. In fact, the platform employed presently cannot support real-time processing when the number of multipaths is four or more, unless either the system architecture or the SIC algorithm is redesigned. Such and other ways of improvement are relegated to potential future work. Copyright © 2003 John Wiley & Sons, Ltd.

KEY WORDS: CDMA; Third-generation partnership project (3GPP); Multiuser detection (MUD); Successive interference cancellation (SIC); Multipath channels; Digital signal processors (DSPs)

1. Introduction

The WCDMA standard developed by 3GPP is a widely accepted third-generation cellular system standard, providing high data rate transmission at a chip rate of 3.84 Mcps. It employs the direct-sequence code division multiple access (DS-CDMA) scheme. DS-CDMA systems assign different codes to different

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users to discriminate their signals. Ideally, interference-free transmission is possible if the codes are orthogonal. In practice, due to multipath propagation and implementation reasons, code orthogonality cannot be attained. This results in interference among user signals, known as multiple access interference (MAI), that constitutes a major limiting factor to CDMA system performance.

The adverse effects of MAI can be mitigated by multiuser detection (MUD) and a variety of MUD techniques have been developed [1]. Among the MUD techniques, one group known as the subtractive interference cancellation detectors has proven to be effective in combatting MAI and yet possesses relatively low complexity. Subtractive interference cancellation detectors are based on a simple heuristic idea: if an interferer's signal has been detected, then the detector can use it to regenerate the interfering signal and subtract it from the received signal for better detection of other user signals. Parallel interference cancellation (PIC) and successive interference cancellation (SIC) are two main types of subtractive interference cancellation techniques. As the names indicate, PIC attempts to cancel the interference from every user to every other user at the same time, while SIC cancels the contributions from different users in a successive way. We consider SIC in this work.

Despite its being of lower complexity among all multiuser detection techniques, SIC at the high chip rate of 3GPP WCDMA still requires a large amount of computation that is beyond the capability of many general-purpose digital signal processor (DSP) chips commercially available today. Hence we consider a multiprocessor implementation. Besides complexity and performance considerations, the successive manner in which user signals are detected in SIC lends it to easier job partitioning and easier signal routing in a multiprocessor implementation. Incidentally, a DSP implementation of PIC is reported in Reference [2].

This paper is organized as follows. Section 2 describes the 3GPP WCDMA uplink transmission system. Section 3 introduces the SIC receiver. Section 4 discusses the DSP implementation and the resulting performance. And finally, Section 5 gives a brief conclusion.

2. The WCDMA Uplink Transmission System

In 3GPP WCDMA, the spectrum spreading procedure consists of two successive multiplications with two different kinds of codes, namely, the channelization codes and a complex scrambling code. The channelization codes are orthogonal and the set of codes are the same for all users. By using more than one channelization code, a user can transmit data on more than one 'channel'. The complex scrambling codes are used to distinguish one user from another. The scrambling codes are not orthogonal. The output chip rate is 3.84 Mcps.

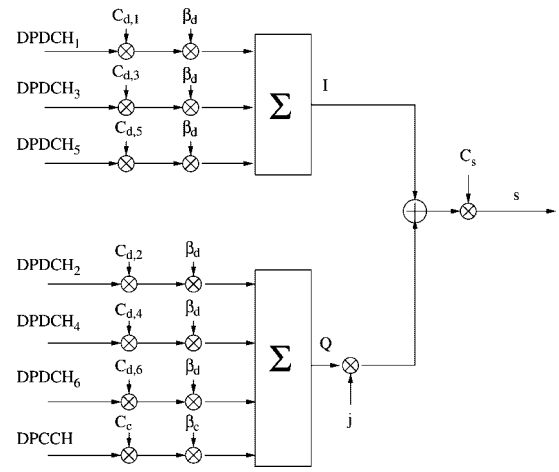

Fig. 1. Spreading for uplink DPCCH and DPDCHs (based on Figure 1 in Reference [3]).

Figure 1 illustrates the principle of the uplink spreading function [3], where the dedicated physical data channels (DPDCHs) carry user data and the dedicated physical control channel (DPCCH) carries pilot bits and some other control information. As shown, the DPCCH is spread to the chip rate by the channelization code C_c, while the mth DPDCH, denoted DPDCH$_m$, is spread to the chip rate by the channelization code $C_{d,m}$. One DPCCH and up to six parallel DPDCHs can be transmitted simultaneously. The spreading factor of the DPCCH is fixed at 256. If there is only one DPDCH, then the spreading factor can vary between 4 and 256. If more than one DPDCH is used, then all use 4 as the spreading factor. After channelization, the spread signals are weighted by the gain factors β_c (for DPCCH) and β_d (for all DPDCHs). The allowed values of β_c and β_d are given in Reference [3] and some example assignments can be found in Reference [4, Annex A]. After the weighting, the I- and Q-branches are summed and treated as a complex-valued stream of chips. This complex-valued signal is scrambled by the complex-valued scrambling code C_s.

Let SF denote the spreading factor for the DPDCHs. Then the kth user's signal after spreading and scrambling is given by

$$s_k[n] = \left\{ \sum_{m=1,3,5} b_m^{(k)}[n] C_{d,m}[n] \beta_d + j \times \left(\sum_{m=2,4,6} b_m^{(k)}[n] C_{d,m}[n] \beta_d + b_p^{(k)}[n] C_c[n] \beta_c \right) \right\} \times C_{s,k}[n] \quad (1)$$

where n is the chip index, $b_m^{(k)}[n]$ is the SF-times repeated user data bit on DPDCH$_m$ and $b_p^{(k)}[n]$ is the 256-times repeated control channel bit. The notations $C_{d,m}[n]$ and $C_c[n]$ should be self-evident, and we have added a second subscript in $C_{s,k}[n]$ to designate the kth user. If one DPDCH is sufficient for the required transmission rate (as is the case considered in our implementation), then the modulation becomes BPSK on both the I- and the Q-branches. (It is not conventional QPSK because the two branches may have different gains.) In this case, Equation (1) reduces to

$$s_k[n] = \left\{ b^{(k)}[n] C_d[n] \beta_d + j \cdot b_p^{(k)}[n] C_c[n] \beta_c \right\} \cdot C_{s,k}[n] \quad (2)$$

For channel transmission, the scrambled chip stream must be filtered by a pulse shaping filter, $g_T(t)$. For this, the 3GPP WCDMA employs a root-raised-cosine (RRC) filter with roll-off factor = 0.22. The receiver front-end employs a similar RRC filter $g_R(t)$. For convenience in simulating the wireless channel, we use the equivalent lowpass representation sampled at four times the chip rate. Also for convenience, we shall distinguish a discrete-time signal at four times the chip rate and its corresponding version at the chip rate by the presence and absence of the superscript $'$. Accordingly, let $s'_k[n]$ denote the four-times upsampled version of $s_k[n]$, and $g'_T[n]$ and $g'_R[n]$ be $g_T(t)$ and $g_R(t)$ sampled at four times the chip rate respectively. Let L_k be the number of resolvable propagation paths of the channel for user k. Then the signal after the receiver filter, sampled at four times the chip rate, is

$$r'_k[n] = \sum_{l=1}^{L_k} \alpha'_{k,l}[n] (g'_T[n] * s'_k[n - \tau_{k,l}] * g'_R[n]) \quad (3)$$

where * denotes convolution, and $\tau_{k,l}$ and $\alpha'_{k,l}$ are respectively, the delay (in units of one-fourth the chip period) and the attenuation of the lth path associated with user k. If there are K users in the system, then the signal after receiver filtering at the base station is

$$r'[n] = \sum_{k=0}^{K-1} r'_k[n] + \eta'[n] * g'_R[n] \quad (4)$$

where $\eta'[n]$ is the additive channel noise sampled at four times the chip rate.

For practical implementation, $g'_T[n]$ and $g'_R[n]$ have to be of finite lengths. We find that the spectrum emission mask of 3GPP WCDMA can be satisfied with $g'_T[n]$ truncated to 33 taps [5]. The receiver filter $g'_R[n]$ may be truncated to the same or a different length depending on complexity and performance considerations.

3. Structure of the SIC Receiver

As mentioned earlier, SIC attempts to eliminate the interference from different users in a successive way. More exactly, it detects a user's signal, regenerates the contribution of this user signal in the received signal and subtracts the regenerated signal from the received signal. It then detects another user's signal and repeats the above process, until all user signals are detected. If the detections are correct, then each iteration through the process reduces the number of interferers by one and thereby improves the performance of later detections. Also as mentioned, the sequential manner in which signal detections are carried out in SIC is beneficial to our DSP implementation employing multiple processors.

In the following subsections, we describe the key features of our SIC receiver.

3.1. Overall Structure

While in principle there can be many users in the system, our hardware platform (described in more detail in Section 4) contains only four DSP chips. We therefore consider three-user SIC. From the perspective of practical system implementation, this should not be severely limiting because the SIC receiver can be modified, replicated and connected to handle the case of more users. On the other hand, consideration of three users is sufficient for us to appreciate various DSP implementation issues.

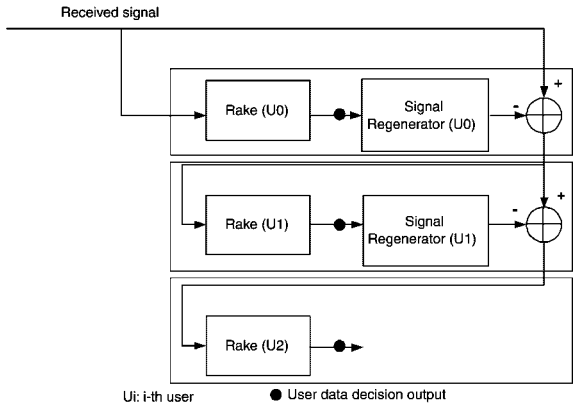

Fig. 2. Block diagram of a three-user SIC receiver.

The block diagram of a three-user SIC receiver is shown in Figure 2. $U0$, $U1$ and $U2$ denote the three users respectively, in the order they are processed. A RAKE receiver is used to detect each user signal, after interference cancellation except for $U0$. The receiver starts with detection of $U0$'s signal. The result is passed through a signal regenerator to reproduce its contribution in the received signal. The regenerator output is subtracted from the received signal to form the input to the next RAKE receiver to detect $U1$'s signal. Mathematically, the subtraction yields

$$r'[n] - \hat{r}'_0[n] = \sum_{k=0}^{K-1} r'_k[n] - \hat{r}'_0[n] + \eta'[n] * g'_R[n] \quad (5)$$

where $K = 3$ in our implementation. If $U0$'s signal is correctly detected, then $\hat{r}'_0[n] = r'_0[n]$ and the residual signal will only contain the contributions of $U1$ and $U2$. The signal detection, regeneration and subtraction process for $U1$ is similar to that for $U0$. Because $U2$ is the last user whose signal is detected, there is no need to regenerate its contribution in the received signal. In fact, for a system with K users, signal regeneration and subtraction may not need to be carried out to the penultimate user. They can be omitted as soon as the interference has been reduced to an acceptable level.

For SIC, it is known that proper power ranking can improve the error performance, so that the user signals are detected in the order of decreasing signal-to-interference-plus-noise ratio (SINR). This is not included in the present implementation for complexity reason.

3.2. The RAKE Receiver

Single-user RAKE receivers have been used widely in today's DS-CDMA systems. Essentially, a RAKE receiver performs maximal-ratio combining (MRC) of the received signal in its span to yield maximum SINR. For illustration, a four-finger RAKE receiver is shown in Figure 3 for an arbitrary user k. The channel estimator employs the pilot symbols in the uplink DPCCH of 3GPP WCDMA and is discussed further in the next subsection.

For each finger, after proper delay as determined by the path searcher-tracker, the received signal is sampled at the chip rate. Techniques for path searching and tracking are not the focus of this work, although we do include a path searcher-tracker in

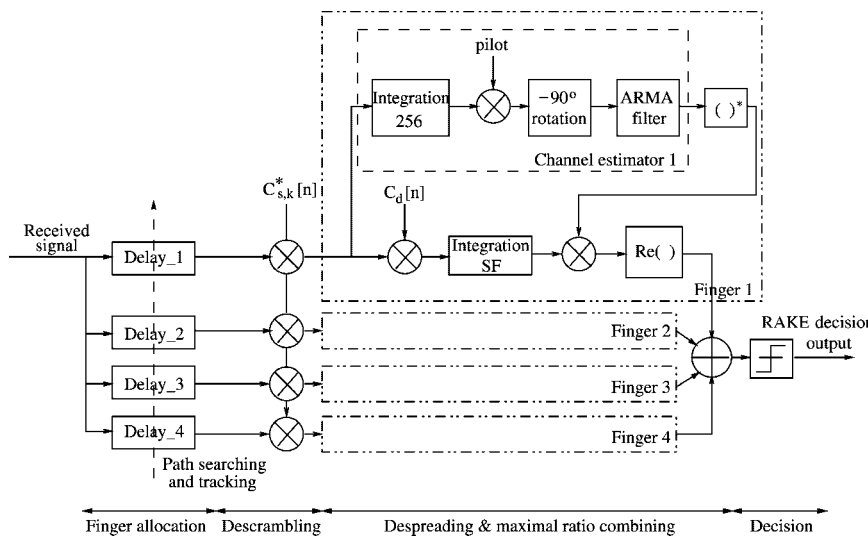

Fig. 3. A four-finger RAKE receiver based on 3GPP WCDMA uplink specifications.

our implementation. Details concerning the searching and tracking method can be found in Reference [6]. The descrambled signal in finger l is given by

$$p_{k,l}[n] = r'[4n + \hat{\tau}_{k,l}]C^*_{s,k}[n] \tag{6}$$

where $\hat{\tau}_{k,l}$ is the estimated path delay. The RAKE receiver then performs despreading in each finger and the despread signal of user k in finger l is, for the ith bit,

$$q_{k,l}[i] = \sum_{n=i\cdot \mathrm{SF}}^{(i+1)\mathrm{SF}-1} p_{k,l}[n] \cdot C_d[n] \tag{7}$$

The despread signal in each finger is weighted by the complex conjugate of the estimated channel coefficient corresponding to that path. The results are summed and thresholded to yield a decision of the ith bit as

$$\hat{b}^{(k)}[i] = \mathrm{sgn}\left\{ \sum_{l=1}^{L_k} \mathcal{R}\ (q_{k,l}[i] \cdot \hat{\alpha}^*_{k,l}[\lfloor i \cdot \mathrm{SF}/256 \rfloor]) \right\} \tag{8}$$

where $\hat{\alpha}_{k,l}[\lfloor i \cdot \mathrm{SF}/256 \rfloor]$ is the estimated channel coefficient of the lth path of user k in the period of bit i. Because the spreading factor for DPCCH is 256, for simplicity the channel coefficients are assumed to remain constant in the period of a pilot bit (a total of 256/SF user data bits) at least. Therefore we have $\lfloor i \cdot \mathrm{SF}/256 \rfloor$ as its time index. The above assumption is also reflected in the channel estimator shown in Figure 3.

3.3. The Channel Estimator

In WCDMA uplink transmission, the DPCCH carries some pilot symbols known to the receiver. We use these symbols to estimate the channel coefficients. Essentially, this estimate is obtained by correlating the locally generated pilot with the received pilot. By using a simple autoregressive moving average (ARMA) filter, as shown in the upper part of Figure 3, the correlator's time constant is made longer than the period of a single pilot bit so that the noise effects may be reduced. The ARMA filter is given by

$$\begin{aligned}\hat{\alpha}_{k,l}[m] = {} & W \cdot \hat{\alpha}_{k,l}[m-2] + (1-W) \\ & \times \left(\tilde{\alpha}_{k,l}[m] + \tilde{\alpha}_{k,l}[m-1]\right)\end{aligned} \tag{9}$$

where $\tilde{\alpha}_{k,l}[m]$ is the filter input and is given by

$$\tilde{\alpha}_{k,l}[m] = -j \cdot b^{(k)}_p[m] \sum_{n=m\cdot 256}^{(m+1)256-1} p_{k,l}[n] \tag{10}$$

The channel estimate is updated once every two pilot bits only. It is also held constant in the period when the DPCCH contains nonpilot symbols. The summation in the right hand side of Equation (10) comes from the fact that $C_c[n]$ in 3GPP contains all 1s. Thus despreading becomes simple accumulation. The weight W is set somewhere between 0 and 1 and may change according to the channel condition. For example, it may be smaller when the channel is fast-changing and larger conversely.

3.4. The Signal Regenerator

The purpose of a signal regenerator is to duplicate the contribution in the received signal of a specific user. The more accurate the duplication, the better performance the SIC can achieve. A signal regenerator that takes finite-precision computation into consideration is shown in Figure 4.

Note that, while in the transmitter the DPCCH and the DPDCH are multiplied by two different gains β_c and β_d, in the signal generator we only multiply the DPDCH by the gain ratio β_d/β_c. This is because the channel estimator, in its computation using the pilot symbols on DPCCH, will supply the factor β_c. For user k therefore, after scrambling we have

$$\hat{s}_k[n] = \left\{ \hat{b}^{(k)}[n] C_d[n] \frac{\beta_d}{\beta_c} + j \cdot \hat{b}^{(k)}_p[n] C_c[n] \right\} \cdot C_{s,k}[n] \tag{11}$$

To regenerate a user signal's contribution in the received signal, the effect of the transmitter and the receiver filters must also be mimicked. We mentioned that a four-times oversampled, 33-tap RRC filter can satisfy the 3GPP WCDMA's spectrum emission mask. If a similar receiver filter is employed for matched filtering, then their combination is a 65-tap filter. To implement such a filter in the signal regenerator is a severe computational burden. Since the cascade of the two filters should approximate a raised cosine (RC) filter, we may use a shorter RC filter to lower the complexity. This may potentially lead to some performance loss compared to perfect reproduction of the transmitter and the receiver filters. But nevertheless it

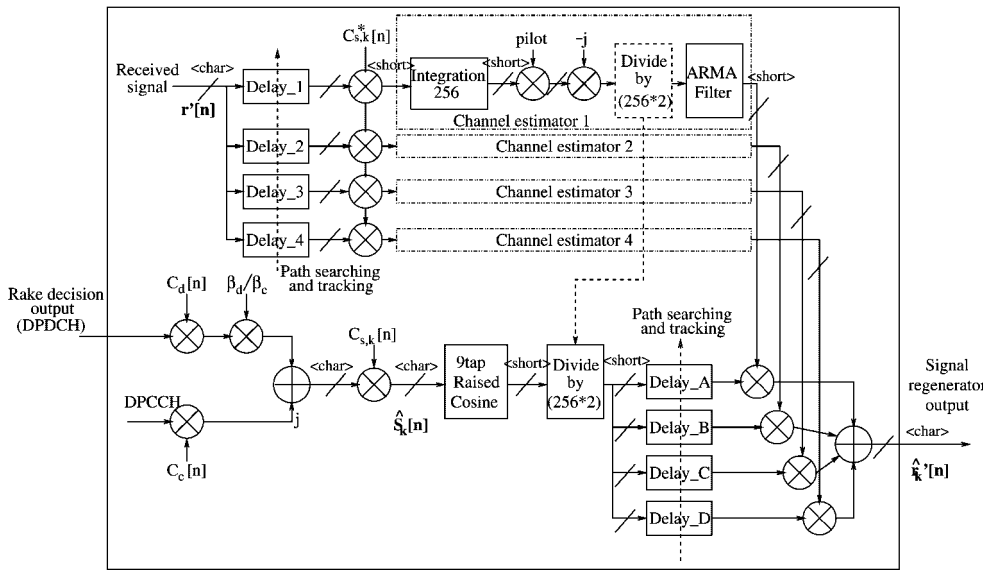

Fig. 4. A signal regenerator in finite-precision arithmetic.

will be able to approximately regenerate the contribution of the given user in the received signal to achieve interference reduction in SIC. In addition, when the transmitter and the receiver are designed and manufactured by two different entities, perfect matching may not be possible anyway. Our analysis shows that a four-times oversampled, 9-tap RC filter contains about 94.5% of the energy in the original 65-tap filter. We thus employ this filter in place of the cascaded RRC and denote it $g'[n]$.

After the RC filtering and the simulated multipath propagation based on the estimated channel response, the signal regenerator output for a specific user k can be expressed as

$$\hat{r}'_k[n] = \sum_{l=1}^{L_k} \hat{\alpha}_{k,l} \left[\left\lfloor \frac{n/4}{256} \right\rfloor \right] \cdot \left(\hat{s}'_k[n - \tau_{k,l}] * g'[n] \right) \quad (12)$$

Equation (12) can be compared with Equation (3) to appreciate and analyze the effects of various inaccuracies on SIC performance.

4. DSP Implementation

4.1. Architecture

Our implementation employs the Quatro6x DSP card made by Innovative Integration (I.I.) [7], with an IBM-compatible PC as the host. The card houses four Texas Instruments' DSP chips, where the DSPs may be the fixed-point TMS320C6201 (200 MHz) or the floating-point TMS320C6701 (166 MHz). The card lays out the four DSPs in a symmetric multiprocessing relationship with high-bandwidth interprocessor communication links, called the FIFO links. The network of FIFO links allows any of the DSPs to transmit to and receive from any other DSP via a high speed 32-bit-wide FIFO buffered interface. The so-called FIFOPorts provide buffered 16-bit interfaces which allow the card to communicate with other I.I. DSP cards or external hardware at high data rates. The PCI interface allows transfer of data to and from the host PC.

We employ Quatro62 (Quatro6x with TMS320-C6201) to implement the three-user SIC receiver. Each SIC stage takes one DSP, as shown in Figure 5. The received signal is first passed to the path searcher-tracker implemented on CPU_4, which finds the path delays and sends the information to CPU_3, CPU_2 and CPU_1 via the FIFO links. As mentioned, we refer to Reference [6] for details of the path searching and tracking method. Besides the path delays, the received signal is also passed to CPU_3. The RAKE receiver on CPU_3 detects $U0$'s data, performs signal regeneration and interference cancellation, and delivers the resulting signal to CPU_2. CPU_2 performs similar operations, except that the user of concern is $U1$. Finally, in CPU_1, the last RAKE is performed for $U2$, completing the entire task. At present, the synchronization between the DSPs is asynchronous, event-driven: a downstream DSP would halt until its upstream FIFO buffer is filled.

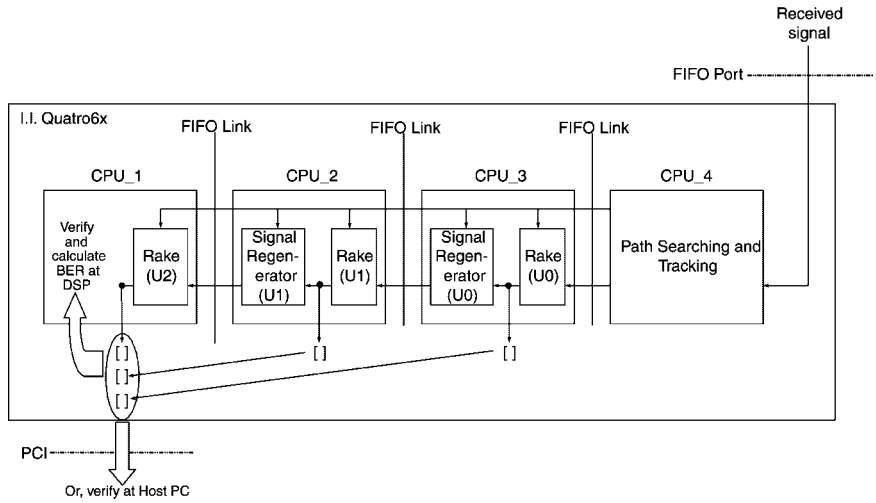

Fig. 5. DSP implementation of three-user SIC receiver.

The receiver performance can be examined and verified in several ways. One is to compare the transmitted and the detected user bits at the host PC and another is to compare them using one DSP. Both ways are illustrated in Figure 5. To do it at the host PC requires routing of the RAKE receiver outputs for $U0$ and $U1$ to CPU_1 because only CPU_1 has access to the PCI. On the other hand, to do it on a DSP requires loading of the transmitted user bits into the DSP card's memory. The latter approach is simpler.

4.2. Error Performance

We examine the bit-error-rate (BER) performance in this subsection. We also compare the BER performance of the DSP implementation with the simulation results.

Although wireless channels are often characterized by multipath fading, for verification purposes we first consider the AWGN condition. Due to considerations outside the scope of the present work, the spreading factor of user data is set to 16 [8]. Figure 6 plots the

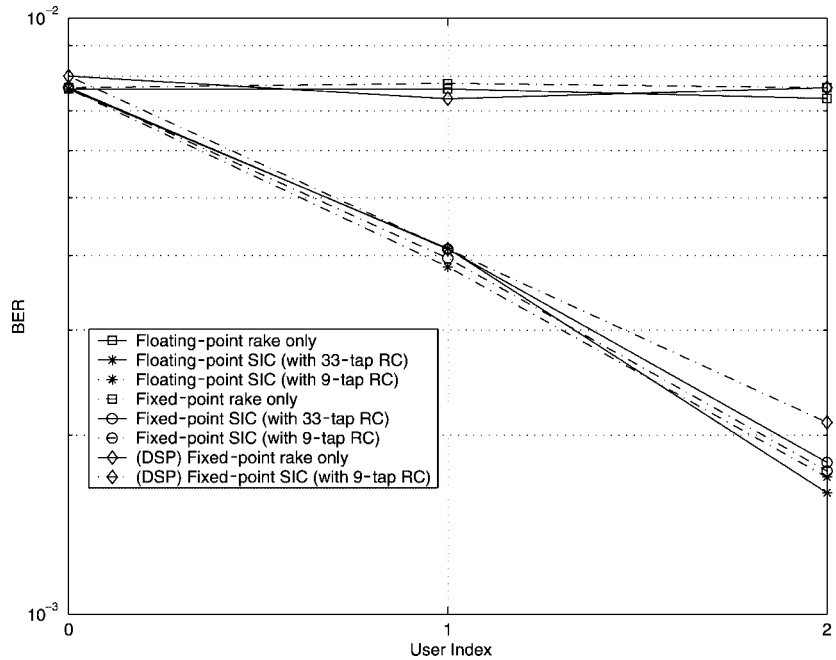

Fig. 6. Receiver performance in AWGN by simulation and with fixed-point DSP implementation at $E_b/N_0 = 7$ dB.

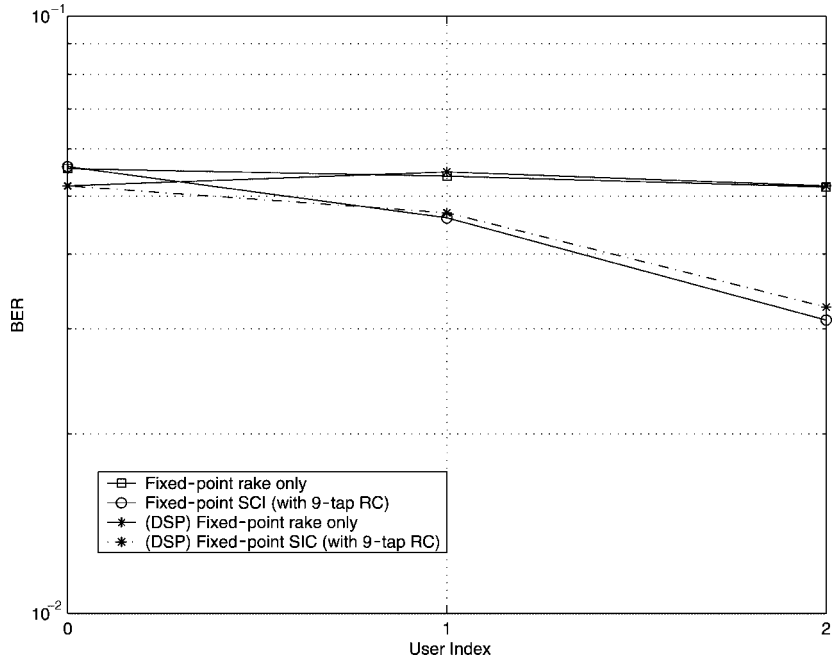

Fig. 7. Comparison of fixed-point simulation and DSP implementation results for signal detection in single-path fading.

performance of the three-user SIC receiver in AWGN at $E_b/N_0 = 7\,\text{dB}$. The user indexes correspond to that in Figure 2. The BERs, both with and without SIC, are given. Theoretically, the single-user BER is $Q(\sqrt{2E_b/N_0})$ for BPSK in AWGN with coherent demodulation. With $E_b/N_0 = 7\,\text{dB}$, it is approximately 10^{-3}. This sets the lower bound of any detection technique.

First, consider the floating-point simulation results. With SIC, the performance of the second and the third users improves significantly. To verify the performance of a 9-tap RC filter in the signal regenerator, we compare it with that of a 33-tap RC filter. The difference is minute, which justifies the use of the 9-tap filter for complexity reason. In both cases with SIC, the BERs for $U2$ are also close to the theoretical minimum of 10^{-3}. The differences should be caused mainly by the residual MAI, signifying that the interference subtractions are not perfect. Next, consider the fixed-point simulation results. A comparison with the floating-point results shows that our design preserves the accuracy well. Finally, consider the results of DSP implementation. The results are obtained using the development tool Code Composer Studio (CCS) from Texas Instruments. We see that the results agree well with that of the simulations.

We now turn to the condition of fading channels. Some results for a single-path fading channel are shown in Figure 7. Here we only compare the result of the DSP implementation with that of fixed-point simulation on a general-purpose computer. Their closeness reaffirms the correctness of the DSP implementation. As a side remark, we note that in comparison to the AWGN channel results, the performance of both the RAKE and the SIC receivers suffers due to fading.

Lastly, we turn to the condition of multipath channels. For this we consider the channel models given in Reference [4], which are shown in Table I. Experimental results again show that a 9-tap RC filter in the signal regenerator performs similarly to a 33-tap RC and that our fixed-point design performs similarly to floating-point simulation.

4.3. Execution Speed and Computational Complexity

Table II lists the measured execution time of SIC components in four multipath conditions for the DSP implementation. Note that the signal regenerator is the most time-consuming component of all. This is due to the RC filtering and the simulation of multipath propagation. Table III shows the measured execution time of different stages of the SIC receiver. Since the scrambling code generation has to be done only once, it is performed offline. The results for $U0$ and $U1$ are exactly the sum of the results for RAKE and signal

Table I. Multipath channel examples (based on Table B.1 of Reference [4]).

Case 1 (3 km/h) Case 5 (50 km/h)		Case 2 (3 km/h)		Case 3 (120 km/h) Case 6 (250 km/h)		Case 4 (3 km/h)	
Relative Delay [ns]	Average Power [dB]	Relative delay [ns]	Average Power [dB]	Relative Delay [ns]	Average Power [dB]	Relative Delay [ns]	Average Power [dB]
0	0	0	0	0	0	0	0
976	−10	976	0	260	−3	976	0
		20000	0	521	−6		
				781	−9		

regenerator in Table II. Therefore, there is imperceptible overhead in combining the SIC components. The results for $U2$ are exactly the same as the RAKE results in Table II, as for this user only the RAKE is performed. The results also show that we fall behind the real-time requirement by about three times in CPU_3 and CPU_2 under the 4-path condition. If only conventional RAKE receiving is needed, then Table II shows that real-time processing is achievable in all conditions.

To see how efficiently we have used the DSP resources in the implementation, we analyze the computational complexity of the SIC receiver. For simplicity, we only calculate the number of multiplications required. This is because in the RAKE receiver and the signal regenerator, multiplications and additions are primary operations. Since the signal flow is quite regular in these components, the amount of multiplications and additions should be indicative of the overall complexity. However, on the TMS320C6201 DSP, there are six adders but only two multipliers [10]. We thus measure the complexity using the number of multiplications.

Table II. Processing time of SIC components for one WCDMA signal frame (10 ms) on DSP, in ms.

Path number	4	3	2	1
One scrambling code generator	7.0	7.0	7.0	7.0
One RAKE	7.8	5.9	3.9	2.0
One signal regenerator	21.0	16.1	11.7	9.9

Table III. Processing time of SIC stages for one WCDMA signal frame (10 ms) on DSP, in ms.

Path number	4	3	2	1
$U0$ on CPU_3	28.8	22.0	15.6	11.9
$U1$ on CPU_2	28.8	22.0	15.6	11.9
$U2$ on CPU_1	7.8	5.9	3.9	2.0

A multiplication on the TMS320C6201 requires two clock cycles. But the multipliers are pipelined, so that, with proper sequencing of data, a throughput of one multiplication per cycle per multiplier is possible. At a 200 MHz clock therefore, the DSP can perform up to 400×10^6 multiplications per second. This will be our base in gauging the efficiency of the implementation.

Consider first the RAKE receiver. The amount of (real-number) multiplications required, per finger, for a 10 ms frame is estimated below.

1. Descrambling:

$$\underbrace{38\,400}_{\#\text{ of chips}} \times \underbrace{4}_{\text{real mult's. per complex mult.}}$$

2. Channel estimation: An upper bound is

$$\underbrace{150}_{\#\text{ of DPCCH bits}} \times \Big(\underbrace{2}_{\text{mult. with pilot}} + \underbrace{\frac{1}{2}}_{\text{freq. of ARMA}} \times \underbrace{4}_{\text{ARMA filtering}} \Big)$$

3. MRC:

$$\overbrace{38\,400 \times \underbrace{2}_{\text{I- and Q-branches}}}^{\text{despreading}} + \overbrace{\underbrace{38\,400/16}_{\#\text{ of data bits}} \times \underbrace{2}_{\text{for real part of complex mult.}}}^{\text{cophased gain}}$$

The total complexity for RAKE receiving is summarized in Table IV. The table also shows the efficiency of our RAKE implementation, where the efficiency is defined as the fraction of multiplier resource used in

Table IV. Computational complexity of RAKE receiver for one WCDMA signal frame and efficiency of DSP implementation.

Path number	4	3	2	1
Mult's. required	943 200	707 400	471 600	235 800
Efficiency (%)	30.2	30.0	30.2	29.5

the time spent for RAKE receiving as given in Table II. For example, in the case of 4 paths the efficiency is calculated as $943\,200/(400 \cdot 10^6 \times 7.8 \cdot 10^{-3}) = 30.2\%$. The efficiency figures are rather consistent over different path numbers, which can also be appreciated from the processing time figures in Table II.

The amount of real multiplications required for the signal regenerator is estimated as follows.

1. Spreading:

$$38\,400 \times (\underbrace{1}_{\text{DPDCH spreading}} + \underbrace{1}_{\text{DPDCH gain}})$$

2. Scrambling:

$$38\,400 \times \underbrace{4}_{\text{real mult's. per complexmult.}}$$

3. Pulse-shaping filtering:

$$38\,400 \times \underbrace{9}_{\text{RC filtering}} \times \underbrace{2}_{\text{I- and Q-branches}}$$

4. Simulated multipath propagation: For each finger,

$$38\,400 \times \underbrace{4}_{\text{oversampling factor}} \times \underbrace{4}_{\text{real mult's. per complex mult.}}$$

The total complexity for signal regeneration and the efficiency of our DSP implementation are summarized in Table V. The efficiency figures for different path numbers vary over a greater range than that of the RAKE receiver. This may be due to uneven overhead in memory accesses.

Table V. Computational complexity of signal regenerator for one WCDMA signal frame and efficiency of DSP implementation.

Path number	4	3	2	1
Mult's. required	3 379 200	2 764 800	2 150 400	1 536 000
Efficiency (%)	40.2	42.9	45.9	38.8

Table VI. Efficiency of DSP processing for three-user SIC receiver. (all data are in percentage)

Path number	4	3	2	1
$U0$ on CPU_3	37.5	39.5	42.0	37.2
$U1$ on CPU_2	37.5	39.5	42.0	37.2
$U2$ on CPU_1	30.2	30.0	30.2	29.5

Taken together, the overall efficiency of the complete SIC receiver, for each user in each multipath condition, is given in Table VI.

Note from Tables IV and V that the required total number of multiplications in the case of four paths is beyond the capability of one TMS320C6201 chip. Therefore, real-time processing cannot be achieved without re-engineering the system architecture (such as distributing the load of one signal regenerator to more than one DSP chip) or the SIC algorithm (to reduce the number of multiplications). Nevertheless, the efficiency figures indicate that there may be room for improvement even under the present system and algorithm structure. These are relegated to potential future work.

4.4. Memory Usage

Table VII gives the memory usage in the three CPUs carrying out the SIC function, where IPRAM and IDRAM respectively, are internal program and data RAMs on the DSP chip, and synchronous DRAM (SDRAM) is external synchronous DRAM on the Quatro62 card. Both the IPRAM and the IDRAM are 64 kbytes in size and the SDRAM contains 64 Mbytes. CPU_2 and CPU_3 have similar usage of the IPRAM and the IDRAM, since both of them implement a RAKE and a signal regenerator. CPU_3 uses a significantly larger amount of the SDRAM because it has to get the received signal samples from CPU_4 and store them for processing use. On the other hand, CPU_1 uses a comparatively smaller amount of the internal memories, especially the IDRAM because it does no signal regeneration.

Table VII. Memory usage of the DSP implementation of three-user SIC receiver, in kbytes.

Processor	CPU_1	CPU_2	CPU_3
IPRAM	28.5	31.5	31.094
IDRAM	30.861	60.188	62.164
SDRAM	1.156	1.188	1173

5. Conclusion

In the area of wireless communication, two subjects of much recent interest are software-defined radio and multiuser detection of CDMA signals. We conducted a study on DSP implementation of SIC receiver for 3GPP WCDMA uplink transmission. The implementation employed a commercially available general-purpose multi-DSP platform. Issues addressed in the work included system-level design for multiprocessor implementation, design of the channel estimator, design of the signal regenerator, determination of the precision of fixed-point computations, consideration of the receiver's error performance and analysis of the implementation's complexity and efficiency. These issues are tightly coupled with the 3GPP WCDMA specifications.

Due to the features of the DSP platform employed, the implementation only considered up to three users. But this has been sufficient for us to appreciate various DSP implementation issues of an SIC receiver. In addition, by the nature of SIC, it is easy to extend the implementation to handle more users with an enlarged platform.

Our present implementation can achieve real-time processing speed if RAKE receivers alone are activated. Due to the complexity in signal regeneration, it still falls short of the real-time requirement when interference cancellation is enacted. Indeed, when the number of multipaths is four or more, either the system architecture or the SIC algorithm needs to be redesigned for real-time processing to be possible with the present platform. These and other ways of improvement are relegated to potential future work.

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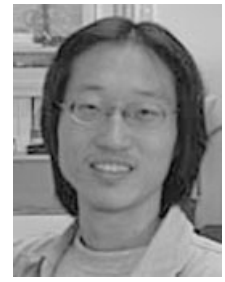
Authors' Biographies



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