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SiC-capped nanotip arrays for field emission with ultralow turn-on field

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Silicon nanotips with tip diameter and height measuring 1 nm and 1 μm, respectively, and density in the range of $10^9-3\times10^{11}$ cm^{-2}, were fabricated monolithically from silicon wafers by electron cyclotron resonance plasma etching technique at a temperature of 200 °C. Field emission current densities of 3.0 mA/cm^2 at an applied field of $\sim$1.0 V/μm was obtained from these silicon nanotips. High-resolution transmission electron microscope and Auger electron spectroscopy analyses concluded that the nanotips are composed of monolithic silicon and nanometer-size SiC cap at the top. A 0.35 V/μm turn-on field to draw a 10 μA/cm^2 current density was demonstrated, which is much lower than other reported materials. The excellent field emission property demonstrated by these nanotips, which were fabricated by a process integrable to the existing silicon device technology at low temperatures, is a step forward in achieving low-power field emission displays and vacuum electronic devices. © *2003 American Institute of Physics*. [DOI: 10.1063/1.1599967]

With the advent of nanotechnologies, microfabricated sharp tips have come up as efficient field emitters than those demonstrated initially by the Spindt-type cathodes.[1] Design and fabrication of field emitter materials and devices have achieved significant progress during recent years[2–6] in pursuit of a new generation of flat panel displays[7] and vacuum microelectronic devices, e.g., microwave power amplifiers.[8,9]

Carbon nanotubes (CNTs) demonstrated remarkable field emission properties. The CNT field emitters can produce high current densities of tens of mA/cm^2 at a low applied electric field of few V/μm.[10–12] However, the adhesion of CNTs to the substrate and the stability of CNT field emitters remain the key issues to be addressed. Recently, CNT-based FEDs have been fabricated by integrated circuit technology and using selective area growth of CNT via microwave plasma enhanced chemical vapor deposition (CVD).[13–15] However, to achieve high structural quality of these CNT and improved field emission performance, the process temperature of CNT growth has to be maintained at above 600 °C. On the other hand, field emitters utilizing lithographically etched silicon tips usually require extremely small tip to gate spacing to achieve the required emission current density because of its high turn-on field of several tens of V/μm.[16,17] A gross reduction in tip diameter and increased packing density of the field emitter tips is required for a major advancement in this field. In this letter, we report the fabrication process of high-density ($10^9-3\times10^{11}$ cm^{-2}) silicon nanotips at low temperatures ($\sim$200 °C) suited for integration into the state-of-the-art silicon technology. Furthermore, high field emission current density has been achieved at ultralow electric field.

Nanomasks hold the key to the formation of high-density nanotips and, hence, the fabrication of nanomasks drives the nanotip technology. Several techniques have been employed to fabricate nanomasks, e.g., electron beam lithography,[18] precoating of substrates before reactive ion etching[19,20] and ion bombardment with a heterogeneous material placing together with the object to be etched,[21] etc. These processes are either too expensive or suffer from the lack of uniformity in terms of geometrical shape and distribution. An femtosecond laser processing of silicon has been reported to produce sharp Si spikes, but of micron sizes.[22] We demonstrate a one-step approach that possesses scale-up capability and maintains excellent uniformity over large area. Formation of nanomasks and development of nanotips by etching of the substrate occurs simultaneously in the same plasma.

The silicon nanotips were fabricated using an electron cyclotron resonance (ECR) plasma reactor, which is comprised of gases such as hydrogen (H_2), argon (Ar), methane (CH_4), and silane (SiH_4) (10% in helium) with a typical flow rates of 8, 5, 1, and 0.2 sccm, respectively. Plasma etching of the Si(100) substrate produced highly aligned uniform silicon nanotip arrays with the tip diameter typically in the nanometer scale ($\sim$1 nm) and the tip length in the micrometer scale ($\sim$1 μm). The tip density can be controlled to range between 10^6 and 10^{11} cm^{-2}, as the typical ones shown in Fig. 1. Each nanotip seems to be protected by a cap at the tip-head. The major physical features of the nanotips, e.g., the aspect ratio and the packing density, could be controlled by adjusting the etching parameters such as substrate temperature, applied microwave power, etc. Typical process temperature was 200 °C, relatively lower than that for the aforementioned CNT growth.

To verify the formation of SiC clusters as the nanomasks, which is suggested by the nanobeam Auger analysis as mentioned earlier, high-resolution transmission electron microscopy (HRTEM) was also employed to acquire the di-

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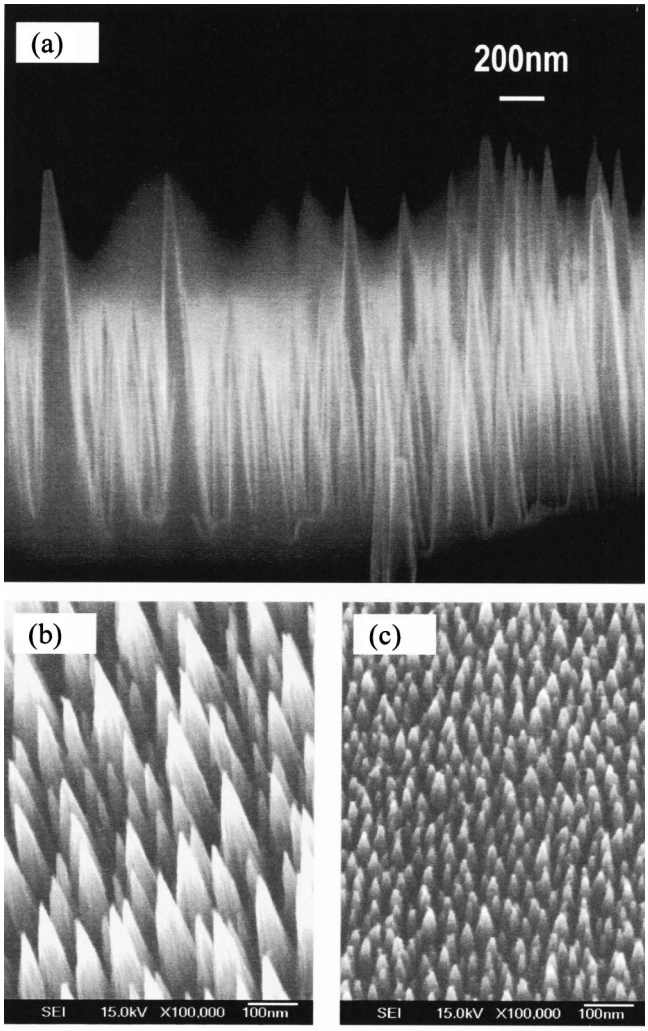

FIG. 1. Typical scanning electron microscopy micrograph of the silicon nanotips. (a) The cross-section view of nanotips of 1 μm height with an aspect ratio of 1000. (b) and (c) show the tilted top views of nanotips demonstrating the high density nature of the arrays of 3×10^{10} and 1×10^{11} cm^{-2}, respectively.

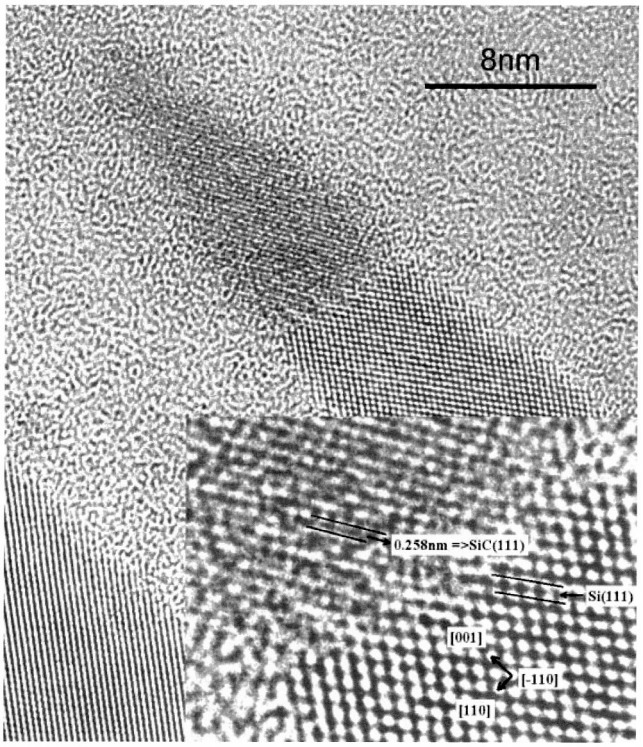

FIG. 2. The cross-section TEM micrograph of a SiC-capped Si nanotip. The inset is a magnified lattice image at the interface between the Si and SiC, which confirms the lattice spacings of the aforementioned materials.

rect evidence of the tip structure. As shown in Fig. 2, the HRTEM image of the nanotip shows clear Si(111) lattice spacing of 3.14 Å, and the cap of the tip with a lattice spacing of 2.58 Å. The cap is confirmed to be SiC since the 2.58 Å lattice spacing is within 97% of the 2.51 Å *d* spacing of a cubic phase SiC(111),[23] and thereby presented a clear evidence for the formation of the SiC nanomasks in the process.

The results discussed so far demonstrate that silicon nanotips are produced by the anisotropic (crystallographic orientation independent) dry etching of the crystalline silicon substrate by the ECR plasma. The SiC clusters produced by the gas phase reactions of SiH_4, CH_4, and H_2 in the plasma could be uniformly and densely distributed on the substrate. These SiC clusters deposited on the silicon substrate then act as nanomasks, during the subsequent etching process, to form the nanotip array. The Ar ion from the plasma plays the dominant role in the formation of nanotips by dry physical etching through selective sputtering process while atomic-H, created in high density by the ECR condition, contributes to the dry chemical etching of the silicon surface. Two competing mechanisms, namely the formation of the SiC nanomask on the surface[24] and the preferential etching of the unmasked silicon,[25] coexist during this process and proceed simultaneously in the plasma, forming the nanotips. Microfabricated pure silicon field emitters are inherently chemically reactive. The contaminants act as tunneling barriers resulting in a larger effective work function leading to emission instabilities. Silicon carbide, being chemically very stable, happens to be attractive as a coating material for silicon emitters. However, the growth of SiC on a nanometer scale Si emitter surface is especially challenging because of the 20% mismatch in lattice parameter between Si and SiC.[26] The one step fabrication technology, under consideration here, eliminates the need for any further encapsulation of the Si emitters. The process was further applied to other substrate materials such as GaAs, GaP, Al, and demonstrated similar nanotip arrays of respective materials capped under a SiC head, which will be reported separately.[27] Figure 3 shows a typical field emission result for SiC capped nanotips on a *p*-type Si substrate. A high current density of 3.0 mA/cm^2 at an applied field as low as $\sim$1.0 V/μm has been achieved. The samples were transferred in air from the ECR processing chamber to the field emission chamber without additional treatment. The field emission chamber is evacuated by a turbo molecular pump to 10^{-7} Torr for the measurement. In the measurement the emission current was limited under 3.0 mA/cm^2 as shown in the figure to avoid damaging the emitter tips. The Fowler–Nordheim (F–N) plot depicted in the inset of Fig. 3 deviates from linear relationship for an ideal field emitter at high electric field. This phenomenon can be attributed to the nonuniformity of the emitter length with fewer discrete long nanotips while the majority of them are shorter ones as shown in Fig. 1. The discrete long nanotips are subjected to less electrical screening effect than the ma-

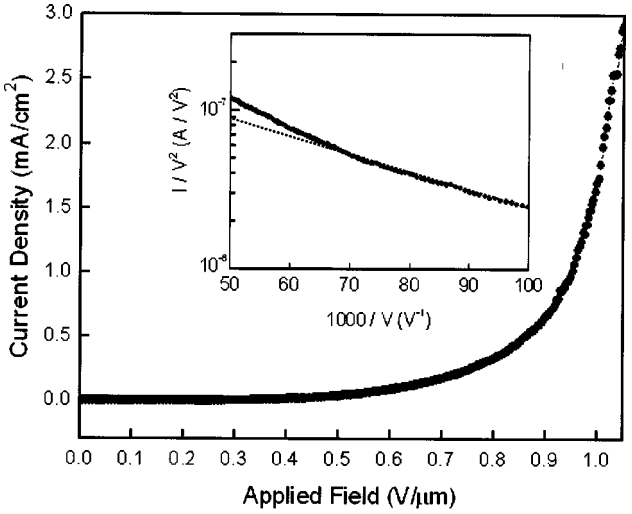

FIG. 3. A typical field emission data obtained from silicon nanotips fabricated monolithically by the ECR dry etching of Si(100) substrate, demonstrating the ultralow turn-on electric fields. The inset presents the emission current data plotted in the Fowler–Nordheim coordinates, wherein the dashed line represents a linear relationship for an ideal field emitter.

jority shorter ones. Therefore, a smaller slope of the F–N fit at low electric field since the emission was mainly contributed from the long nanotips and a larger slope was observed at high electric field as emission was dominated by the large number of the short nanotips. The turn-on field for the nanotips, defined as the electric field required to extract a current density of $10\,\mu\mathrm{A/cm^2}$ from the tip, is found to be $\sim 0.35\ \mathrm{V}/\mu\mathrm{m}$, which is much lower than other reported materials. The low turn-on field in the reported nanotip arrays can be attributed to the extreme sharpness (therefore, large field enhancement factor) of the nanotips as well as negative electron affinity effect from wide band gap materials[28] such as the aforementioned SiC cap. It should be noticed that a *p*-type substrate produced much higher field emission current than an n-type one, which will be reported separately.[29] Silicon based nanotip field emitters operational at ultralow electric fields opens up several possibilities for versatile field emission applications. Field emission displays based entirely on silicon technology, in particular, can thus be realized to produce the next generation displays. Further experiment to fabricate diode- and triode-type emitter is underway to achieve the goal.

Lowering of the operational voltage has multiple effects on the performance of the emitter arrays. The low voltage operation reduces the emitter driving input power and thereby maximizes the power gain and the emission efficiency of the device. In addition, low-voltage operation improves the transconductance of the emitter arrays for any given operating current. The total transconductance of the emitter array again increases effectively with the emitter packing density. Moreover, both smaller tip diameter and larger aspect ratios are advantageous in improving the field enhancement factor at the tip and thereby increasing the transconductance. The lowest possible inter electrode capacitance and the highest possible transconductance maximizes the cutoff frequency at which a field emission electrode could be operational in a miniaturized vacuum device. Ongoing emitter array fabrication technology can successfully extend the limits with respect to emitter tip packing density, sharpness of the nanotips and a low voltage operation (at an ultralow electric field of $\sim 1.0\ \mathrm{V}/\mu\mathrm{m}$).

In conclusion, ultrasharp (~ 1 nm diameter) and high density (up to $10^{11}\ \mathrm{cm}^{-2}$) silicon nanotip arrays has been fabricated using a one-step ECR–CVD technique at low temperatures ($\sim 200\,^{\circ}\mathrm{C}$). Excellent field emission ($3.0\ \mathrm{mA/cm^2}$ at $\sim 1.0\ \mathrm{V}/\mu\mathrm{m}$) from SiC-capped silicon nanotip arrays has been demonstrated, which opens up potentials for feasible field emission displays and vacuum electronic devices.

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