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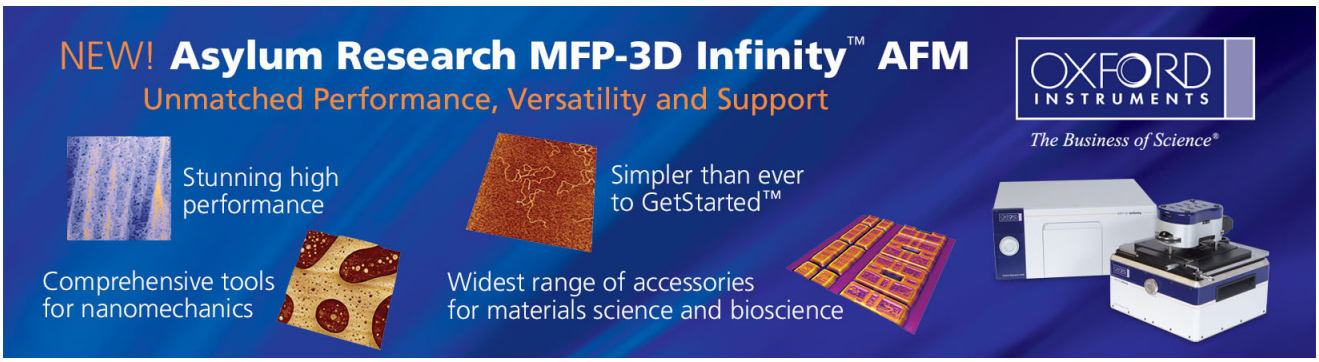

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Improvement in retention time of metal–ferroelectric–metal–insulator–semiconductor structures using MgO doped $Ba_{0.7}Sr_{0.3}TiO_3$ insulator layer

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We report the results of the fabrication and characterization of $Pt/Bi_{3.35}La_{0.85}Ti_3O_{12}$ (BLT)/$LaNiO_3$ (LNO)/$Ba_{0.7}Sr_{0.3}TiO_3$ (BST)/Si metal–ferroelectric–metal–insulator–semiconductor (MFMIS) structures for ferroelectric memory field effect transistor applications. The BLT films were deposited on LNO/BST/Si using the metalorganic decomposition method and annealed by rapid thermal annealing (RTA) process at 600 °C for 3 min. The ratio of remanent polarization to saturation polarization (P_r/P_s) increases with reducing area ratio, A_F/A_I. A large memory window of 3.1 V can be obtained for a small A_F/A_I ratio. By the utilization of 5 mol % MgO doped BST insulator layer, LNO bottom electrode layer for BLT, and small area ratio, $A_F/A_I=1/12$ in the MFMIS structure, large P_r/P_s ratio in BLT film and low leakage current and good capacitance matching of the ferroelectric and the insulator in the MFMIS structures have been achieved and, hence, long data retention time $>10^6$ s has been obtained in this study. Experimental results demonstrate the significant progress in increase of the retention time of these structures, which make them attractive for practical ferroelectric memory field effect transistor applications. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1597412]

Recently, the ferroelectric memory field effect transistors (FeMFETs) have been attracted considerable attention for the applications to nonvolatile ferroelectric random access memories,[1–3] because nondestructive readout is possible and they follow the scaling rule for high density implementation. Good memory window and high switching speed have been reported by some researchers, however, at present, the best data retention time of FeMEFTs was shorter than 10^5 s.[4] Therefore, the difficulty to achieve good data retention characteristics of FeMFETs must be overcome in order to realize its practical applications.[2] On the basis of the results of the theoretical analysis on the electrical characteristics of FeMFETs, the good data retention characteristics at low voltage operation can be obtained through the utilization of larger remanent polarization to saturation polarization ratio (P_r/P_s) ferroelectric film, low leakage current density of insulating layer and small A_F/A_I area ratio of the metal–ferroelectric–metal–insulator–semiconductor (MFMIS) structures.[5–8]

In this letter, we report the electrical properties of MFMIS structures using ferroelectric $Bi_{3.35}La_{0.85}Ti_3O_{12}$ (BLT) film and 5 mol % MgO doped $Ba_{0.7}Sr_{0.3}TiO_3$ (BST) insulating layer. The 5 mol % MgO doped BST has been reported to have a high dielectric constant of 372 and low leakage current of 1×10^{-10} A/cm^2 at an electric field of 100 kV/cm,[9] which is expected to be suitably used as an insulating material for the "*I*" layer. Effects of area ratio, A_F/A_I on the relation capacitance versus applied voltage, memory window, and data retention time are also provided.

The $Pt/BLT/LaNiO_3$(LNO)/BST/Si MFMIS structures were fabricated in this study with *p*-type Si (100) as starting substrate. Subsequent to standard Radio Corporation of America clean, SiON film was grown on silicon substrate in pure N_2O gas in a furnace. After removing the sacrificial SiON layer by dipping the substrate in diluted HF solution, the 16-nm-thick 5 mol % MgO doped BST (Ba/Sr= 70/30) insulator film was deposited on the earlier pretreated substrate by using rf magnetron sputtering. All insulator films were prepared at a fixed power of 100 W, substrate temperature at 450 °C and constant pressure of 20 mTorr, which was maintained by a mixture of argon and oxygen at a mixing ratio of 1:1 with a total flow of 20 sccm. The as-deposited film was annealed at 700 °C by the rapid thermal annealing (RTA) process in pure O_2 ambient for 3 min. The equivalent oxide thickness of BST film is 0.56 nm. The similar steps were employed to deposit the 25-nm-thick LNO oxide electrode on insulator layer. Next, the ferroelectric BLT film with a thickness of 180 nm was formed using a metalorganic decomposition method. The BLT thin film was annealed by the RTA process at 600 °C for 3 min in oxygen ambient. The Pt top electrode was formed and patterned by the lift-off process and finally backelectrode Al was evaporated. The area ratio of MFMIS structures, A_I/A_F varies from 1 to 16.

The capacitance–voltage ($C-V$) characteristics were measured on the MFMIS structures using a Keithley 590 CV analyzer. To measure the $C-V$ characteristics, the voltage was applied from the accumulation to the inversion with a sweep rate of 0.1 V/s at 100 kHz and elapsed time of 30 s. The leakage current density versus voltage measurement was performed using a HP4156C semiconductor parameter analyzer. Ferroelectric hysteresis loops were measured by a Radiant Technologies 66A ferroelectric test system. The thicknesses of thin films were determined from scanning electron microscopy observation and N&K 1200 analyzer.

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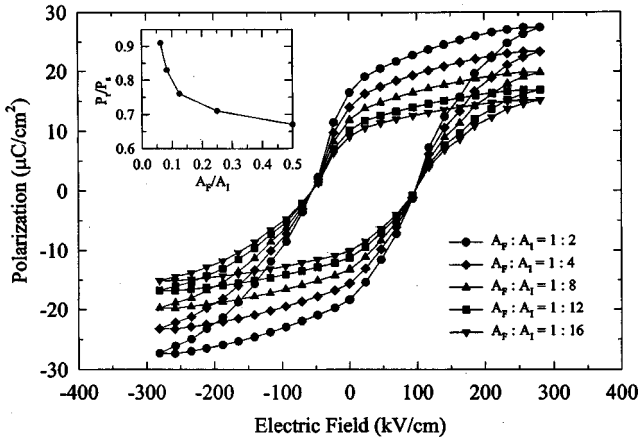

FIG. 1. $P-E$ hysteresis loops of BLT films when the area ratio, A_F/A_I is changed from 1/2 to 1/16. The inset shows the changes of P_r/P_s with the A_F/A_I ratios.

The polarization versus electric field ($P-E$) hysteresis loops of BLT films were measured on Pt/BLT/LNO (MFM) structures among MFMIS frames. The voltage ± 5 V was applied to the BLT films in MFMIS structures with various area ratios, A_F/A_I. It is indicated in Fig. 1 that the P_r/P_s ratio increases from 0.67 to 0.91 with the area ratio A_F/A_I decreasing from 1/2 to 1/16.

Figure 2 depicts the $C-V$ characteristics of Pt/BLT/LNO/BST/Si structures with various A_F/A_I ratios at the voltage sweep rang of ± 5 V. The physical reason for clockwise hysteresis loops has been given in a previous article.[6] In addition, the accumulation capacitance decreases when the area ratio A_F/A_I is decreased, which is attributed to decrease in total capacitance of the MFMIS structure arising from the decrease of MFM area. The theoretical memory window is about 3.1 V, because the memory window is represented by $2V_C$ and the coercive field and thickness of BLT films were approximately 86 kV/cm and 180 nm, respectively. The memory window of Pt/BLT/LNO/BST/Si MFMIS structures increases with the decreasing area ratio A_F/A_I as shown in the inset of Fig. 2. The observed memory window is 1.5 V for $A_F/A_I=1:2$, whereas it becomes 3.1 V for the $A_F/A_I=1:16$.

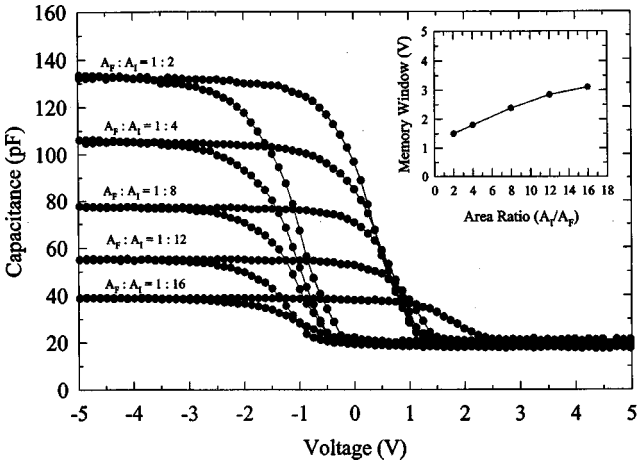

FIG. 2. $C-V$ characteristics of Pt/BLT/LNO/BST/Si MFMIS structures with various area ratios, A_F/A_I indicated. The inset shows the memory window as a function of area ratio.

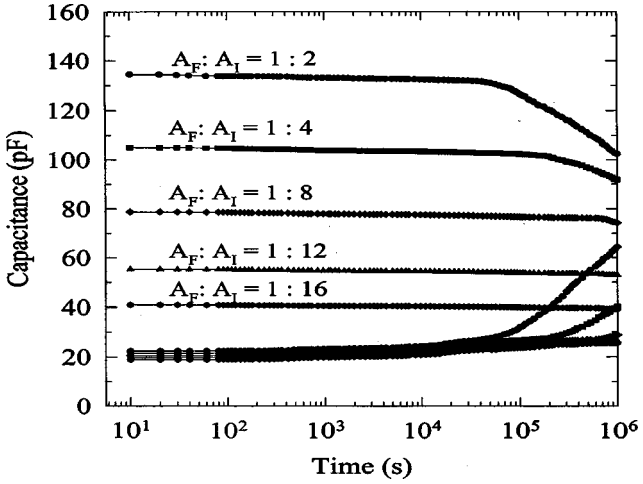

FIG. 3. Data retention time measured for MFMIS structures with various area ratios, A_F/A_I indicated.

The retention characteristics of the MFMIS structures are illustrated in Fig. 3. The writing pulse applied to the MFMIS capacitors were ± 4 V in height and 1 s in duration. The measurement voltage was kept at 0 V. It is indicated in Fig. 3 that the retention time is more than 10^5 s for various area ratios, A_F/A_I and is 10^6 s or more (>11.6 days) for area ratio, $A_F/A_I=1/12$ and 1/16 which is the longest retention time of MFMIS capacitors appeared in the published literature. Figure 4 shows the leakage current density of the MFMIS structure with various area ratios, A_F/A_I, indicated. The leakage current density of the structures has a small value of near 10^{-10} A/cm^2 because of high resistivity MgO doped BST used as I layer[9] and nitridation treatment of silicon wafer.[10] For $A_F/A_I=1/12$ MFMIS capacitors, P_r equals 10 μC/cm^2 and leakage current is about 10^{-10} A/cm^2 (Fig. 4), the expected retention time for our MFMIS structure can be estimated to be 10^4 s for the highest possible trapping probability of $\alpha=1$ and 10^8 s for the very low trapping probability of $\alpha=10^{-4}$ based on a previous study.[8] Our measured retention time, $>10^6$ s is located between these two extreme expected values. However, an acceleration test will have to be employed to verify that is the 10 year retention time achieved. The measurement method used in this study is too tedious.

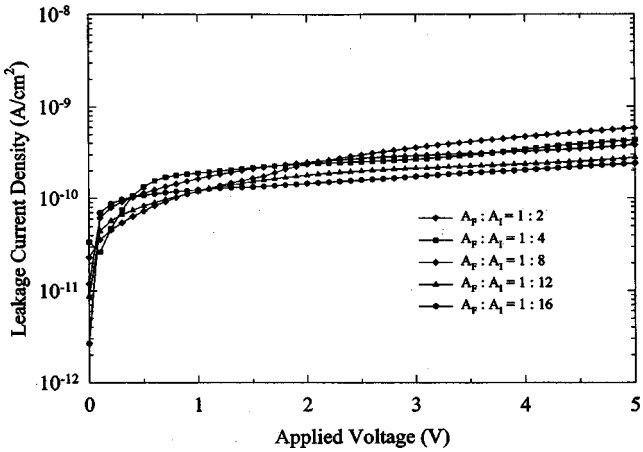

FIG. 4. Plot of leakage current density vs applied voltage for MFMIS structures with various area ratios, A_F/A_I indicated.

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In comparison with the reported results, which are less than a few days of retention time for the best FeMFET, significant improvement in retention time was observed in our MFMIS structures. We attribute such improvement to four major reasons: (1) large P_r/P_s ratio in ferroelectric BLT films. The P_r/P_s ratios corresponding to A_F/A_I ratios 1/12 and 1/16 capacitors which exhibit long retention time are about 0.8 and 0.9, repectively (the inset of Fig. 1); (2) high resistivity MgO doped BST insulator layer and low leakage current MFMIS structures; (3) good interfacial properties of BST/Si due to nitridation treatment;[10] and (4) good matching of the capacitances of MFM and MIS.[7]

In summary, Pt/BLT (180 nm)/LNO (25 nm)/BST (16 nm)/Si MFMIS structures have been fabricated and characterized. The memory window of the MFMIS capacitors depended on the area ratio, A_F/A_I. A large memory window of 3.1 V could be obtained for $A_F/A_I=1/16$. A significant improvement in data retention time, >11.6 days has been achieved for Pt/BLT/LNO/BST/Si MFMIS structures, which enables researchers to be optimistic in reaching the requirement of 10 year retention time for FeMFETs with potential prospects of realizing the practical applications of nonvolatile FeMFET in the future.

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