Electrical Characteristics of Low Temperature Polysilicon TFT With a Novel TEOS/Oxynitride Stack Gate Dielectric

Kow-Ming Chang, Wen-Chih Yang, and Chiu-Pao Tsai

***Abstract*—This investigation is the first to demonstrate a novel tetraethylorthosilicate (TEOS)/oxynitride stack gate dielectric for low-temperature poly-Si (LTPS) thin film transistors (TFTs), composed of a plasma-enhanced chemical vapor deposition (PECVD) thick TEOS oxide/ultrathin oxynitride grown by PECVD N_2O-plasma. The stack oxide shows a very high electrical breakdown field of 8.4 MV/cm, which is approximately 3 MV/cm larger than traditional PECVD TEOS oxide. The field effective mobility of stack oxide LTPS TFTs is over 4 times than that of traditional TEOS oxide LTPS TFTs. These improvements are attributed to the high quality N_2O-plasma grown ultrathin oxynitride forming strong Si $\equiv$ N bonds, as well as to reduce the trap density in the oxynitride/poly-Si interface.**

***Index Terms*—N_2O-plasma oxynitride, stack oxide, thin film transistors (TFTs).**

I. Introduction

LOW-TEMPERATURE poly-Si thin-film transistors have high mobility and driving current, making them highly suitable for realizing peripheral circuits on active matrix liquid crystal displays (AMLCDs) glass substrate [1]. However, the traditional LTPS TFTs, which use PECVD SiO_2 or Si_3N_4 as the gate insulator, suffer from high interface trap states, low electrical breakdown field (< 6 MV/cm) and high gate leakage current [2]. In contrast, PECVD oxynitride has been reported to archive strong Si $\equiv$ N bonds, smooth interface, and excellent charge trapping properties in the oxynitride/poly-Si interfaces [3]. However, although the oxynitride is a good candidate for forming high quality ultrathin oxide, it is not suitable for high-voltage LTPS TFTs peripheral driver integrated circuit (IC) applications. Specifically, the plasma radical oxidation process has difficulty in obtaining a thick and high quality dielectric film at low oxidation temperature ($<= 300\,^{\circ}$C) because of self-limiting effect of thermal oxidation [4] and plasma induced damage [5]. Because of the small breakdown voltage of such thin ($<= 120$ Å) plasma grown oxide, which cannot be applied in making high-voltage TFTs peripheral driving ICs [6], [7]. Consequently, a high quality and durable low-temperature gate dielectric needs to be developed for LTPS TFTs peripheral circuit applications embedded on AMLCDs plates. This study proposes a simple stack gate dielectric structure, based on the continuous stacking of PECVD N_2O plasma grown ultrathin oxynitride (about 3 nm) together with thick-TEOS oxide (37 nm), without breaking the process chamber vacuum. The high quality ultrathin oxynitride formed a strong Si $\equiv$ N bonds and low charge trapping density at the oxynitride/poly-Si interface. The upper 37 nm TEOS oxide layer solves the high-voltage operation problem in the application of LTPS TFTs peripheral circuits.

Manuscript received February 3, 2003; revised May 30, 2003. This work was supported by the National Science Council of Taiwan, R.O.C. under Contract NSC-90-2215-E-009-104. The review of this letter was arranged by Editor J. Sin.

The authors are with the Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: kmchang@cc.nctu.edu.tw).

Digital Object Identifier 10.1109/LED.2003.815155

II. Device Fabrication

Amorphous silicon (a-Si) films with thickness of 100-nm were formed on 4-in thermally oxidized Si wafers by dissociating SiH_4 gas at 550 °C using LPCVD. The a-Si films were then pre-patterned into active islands, and subsequently crystallized at 600 °C furnace annealing in the N_2 ambient for 20 h. Following surface oxide removal, the 40-nm-thick stack gate dielectric (37 nm TEOS/3 nm SiON) film was formed by two step oxidation. First, PECVD N_2O-plasma oxidation was performed at 300 °C substrate heating, a plasma pressure of 100 mtorr, 200 W RF power and 1 min of treatment time to grow a 3 nm thick oxynitride, then a 37 nm thick PECVD TEOS was continuously deposited *in-situ* on the thin-oxynitride without vacuum breakout. For comparison, the control sample was comprised of a 40 nm thick PECVD TEOS oxide without N_2O-plasma treatment. Next, a 200 nm-thick poly-Si was deposited and patterned for the gate electrode. Also, a self-aligned phosphorous implantation was performed at a $5\times10^{15}/\text{cm}^2$ dosage and 40 Kev energy. Moreover dopant activation was performed at 600 °C furnace annealing at N_2 ambient for 12 h following the deposition of a 400 nm TEOS oxide passivation layer and contact hole definition. Finally, 500 nm Al was deposited and patterned to provide an electrode pad. Al sintering was then carried out at 400 °C for 30 min. These LTPS TFTs devices were fabricated without using hydrogenation plasma passivation treatment.

III. Results & Discussion

Fig. 1 illustrates the current density versus electric field characteristics of LTPS TFTs with both TEOS and TEOS/N_2O-plasma oxynitride stack oxide. Obviously, the electrical breakdown field of stack oxide is up to 8.4 MV/cm at a current density of 6 mA/cm^2. Over 40 samples were measured to determine the exact dispersion of breakdown voltage. The dispersion of breakdown voltage of TEOS/oxynitride stack

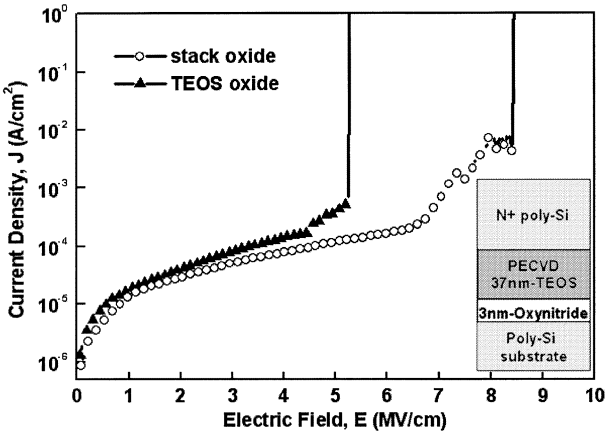

Fig. 1. Current density versus electric field (J–E) characteristics of the gate oxide for the conventional TEOS oxide and proposed stack oxide poly-Si TFTs.

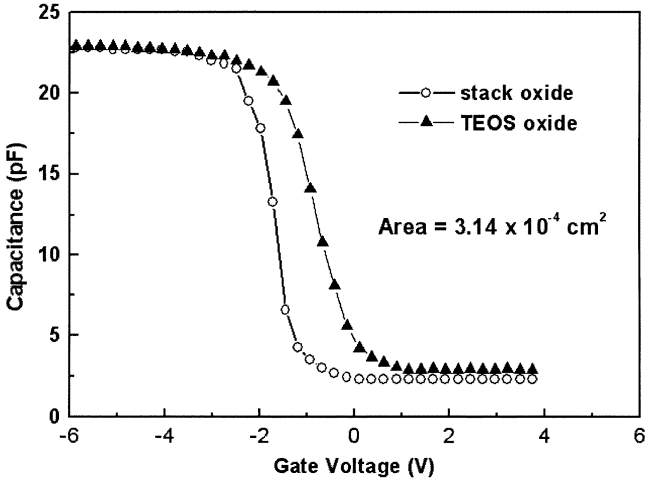

Fig. 2. High-frequency C–V curves of MOS capacitor with TEOS and stack oxide dielectrics films. The frequency was 1 MHz.

oxide is between 33 V and 34 V ($8.25 \sim 8.75$ MV/cm). These breakdown voltages prove that PECVD TEOS/oxynitride stack oxide is superior to conventional TEOS oxide ($20 \sim 24$ V). Fig. 2 shows the capacitance–voltage (C–V) curve of the stack oxide. The C–V curve of stack oxide exhibits a rather sharp transition curve compared with the conventional TEOS oxide. The sharp transition indicates that the interface traps of N_2O-plasma oxynitride is less than conventional TEOS oxide [8]. However, the larger V_T shift of the TEOS/N_2O-plasma oxynitride stack oxide is caused by the damage induced by N_2O-plasma and charging damage from plasma-enhanced TEOS deposition, which results in charge trapping [3], [5]. Even the TEOS/oxynitride stack oxide induced more trapped charge than with TEOS oxide, causing a slightly flatband voltage ($V_{\rm FB}$) shift than with the latter. The TEOS/oxynitride stack gate dielectric still demonstrates good interface property and lower leakage current, which are significantly better than with TEOS oxide.

Fig. 3 displays the I_D–V_G characteristics of the stack oxide LTPS TFTs. The ON current of the stack oxide TFTs was approximately one order larger than that of the TEOS oxide TFTs. Moreover, at high electric field, the leakage current is 1.1 nA and 0.23 nA for TEOS TFTs and TEOS/oxynitride

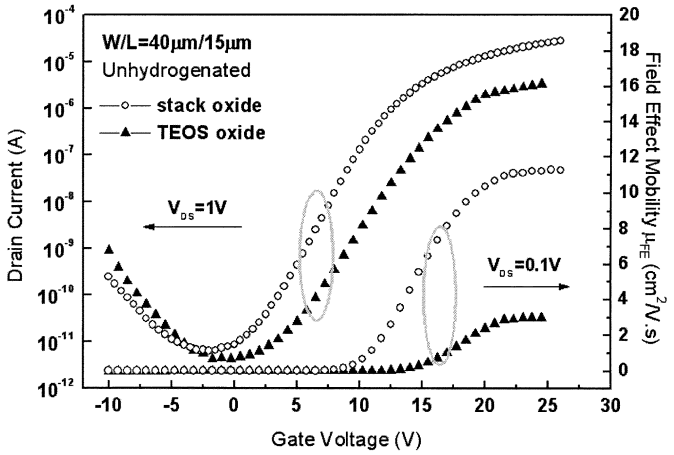

Fig. 3. Transfer characteristic for a 40 μm wide $\times$ 15 μm long stack oxide structure n-channel polysilicon TFT with $V_{DS} = 1$ V for drain current I_D and $V_{DS} = 0.1$ V for field-effect mobility $\mu_{\rm FE}$.

TFTs, respectively. The leakage current of stack oxide TFTs was much lower than that of TEOS oxide TFTs, when the TFTs were biased at larger reverse bias of $V_{GS} = -10$ V. At low electric field, the minimal leakage current was 4.1 pA and 6.34 pA for TEOS TFTs and TEOS/oxynitride TFTs, respectively. The low minimal leakage current of TEOS TFTs is due to a large amount of interfaced states and grain boundary traps in TEOS TFTs. The subthreshold swing (SS) of the stack oxide TFTs was 2 V/dec, compared to 2.67 V/dec for the TEOS oxide TFTs. The subthreshold swing of TFTs is well known to be controlled by the interface trap states, while the small SS value implies the low interface states [9]. Notably, the field effective mobility of stack oxide TFTs is over 4 times than that of TEOS oxide TFTs where both measurements were taken at $V_{DS} = 0.1$ V and $V_{GS} = 23$ V. However, the mobility and subthreshold swing are still rather poor because the growth conditions of LPCVD polysilicon film was not optimized, so our conventional polysilicon thin film transistor with TEOS oxide only has mobility of only about 3 $\rm cm^2/V \cdot s$ poorer than reported elsewhere [1], However, its electrical properties were consistent with data for nonoptimized polysilicon film [9]. To investigate the improvement of device characteristics in stack oxide LTPS TFTs, this study also evaluated the grain boundary trap density using a modified Levinson's model [10]. The density of the grain boundary traps in TEOS/oxynitride TFTs and TEOS TFTs was found to be $1.45 \times 10^{13}/\rm cm^2eV$ and $1.78 \times 10^{13}/\rm cm^2eV$, respectively, indicating that the N_2O-plasma oxynitride film reduces both the interface and grain boundary trap states. However, the grain boundary traps play a more important role than the reduction of interface states, in the mobility and subthreshold swing improvement of LTPS TFTs [11]. We will try to use high-quality novel TEOS/oxynitride on excimer laser crystallized LTPS TFTs to improve further the performance of LTPS TFTs in the future work. Fig. 4 shows the SIMS depth profiles of N and O atom in the N_2O-plasma grown oxynitride and TEOS dielectric films. Structurally, the SIMS samples comprise poly-Si/oxide/poly-Si, and were prepared as the same process as the LTPS TFTs. The N concentration of the oxynitride film is clearly about one order higher than that of the TEOS oxide

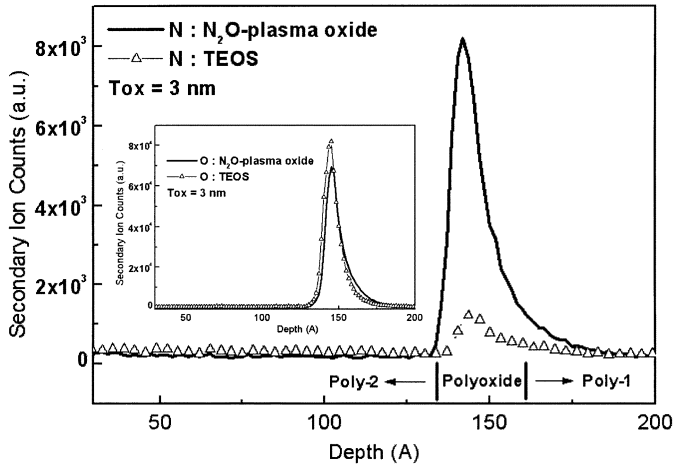

Fig. 4. The SIMS nitrogen profiles of the thin N_2O-plasma oxynitride and TEOS oxide films. The insert is the SIMS oxygen profiles of the thin N_2O-plasma oxynitride and TEOS oxide films.

film. This phenomenon proves that large amounts of nitrogen exist in the oxynitride film and form the strong Si $\equiv$ N bonds in the oxynitride/poly-Si interface.

IV. Conclusion

The LTPS TFTs fabricated with TEOS/Oxynitride stack dielectric exhibit excellent characteristics including electric field up to 8.4 MV/cm, low leakage current, low interface trap density, and low poly-Si grain boundary trap states resulted from the formation of strong Si $\equiv$ N bonds in the oxynitride/poly-Si interface, while the N_2O-plasma passivation effect reduced interface and grain boundary trap density.

References

[1] G. K. Guist and T. W. Sigmon, "High-performance thin-film transistors fabricated using excimer laser processing and grain engineering," *IEEE Trans. Electron Devices*, vol. 45, pp. 925–932, Apr. 1998.

[2] J. K. Lee, J. B. Choi, S. M. Seo, C. W. Han, and H. S. Soh, "The application of tetraethooxysilane(TEOS) oxide to a-Si: H TFT's as the gate insulator," *SID Dig.*, vol. 29, 1998.

[3] E. Ibok, K. Ahmed, M.-Y. Hao, B. Ogle, J. J. Wortman, and J. R. Hauser, "Gate quality ultrathin (2.5 nm) PECVD deposited oxynitride and nitrided oxide dielectrics," *IEEE Electron Device Lett.*, vol. 20, pp. 442–444, Sept. 1999.

[4] J. W. Lee, N. I. Lee, S. H. Hur, and C. H. Han, "Oxidation of silicon using electron cyclotron resonance nitrous oxide plasma and its application to polycrystalline silicon thin film transistors," *J. Electrochem. Soc.*, vol. 144, p. 3228, 1997.

[5] K. P. Cheung and C.-S. Pai, "Charging damage from plasma enhanced TEOS deposition," *IEEE Electron Device Lett.*, vol. 16, pp. 220–222, June 1995.

[6] Y. Z. Xu, F. J. Clough, E. M. S. Narayanana, Y. Chen, and W. I. Milne, "A conductivity modulated high voltage polycrystalline silicon thin film transistor with improved on state and transient performance," in *IEDM Tech. Dig.*, 1998, pp. 273–276.

[7] F. J. Clough, Y. Chen, E. M. S. Narayanan, W. Eccleston, and W. I. Milne, "A novel thin film transistor for high voltage circuitry on glass," *Power Semicond. Devices IC's*, pp. 321–324, 1997.

[8] J.-W. Lee, N.-I. Lee, J.-I. Han, and C.-H. Han, "Characteristics of polysilicon thin-film transistor with thin-gate dielectric grown by electron cyclotron resonance nitrous oxide plasma," *IEEE Electron Device Lett.*, vol. 18, pp. 172–174, May 1997.

[9] C. A. Dimitriadis, P. Coxon, L. Dozsa, L. Papaddimitrious, and N. Economou, "Performance of thin film transistors on polysilicon films grown by LPCVD at various conditions," *IEEE Trans. Electron Devices*, vol. 39, pp. 598–606, Mar. 1992.

[10] J. Levinson, F. R. Shepherd, P. Scanlon, W. D. Westwood, G. Este, and M. Rider, "Conductivity behavior in polycrystalline semiconductor thin film transistors," *J. Appl. Phys.*, vol. 53, no. 2, p. 1193, Feb. 1982.

[11] D. R. Campbell, "Enhanced conductivity in plasma-hydrogenated polysilicon films," *Appl. Phys. Lett.*, vol. 36, p. 604, 1980.