A Fully Integrated Ultra-Low Insertion Loss T/R Switch for 802.11b/g/n Application in 90 nm CMOS Process

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***Abstract*—A 30 dBm ultra-low insertion loss CMOS transmit-receive switch fully integrated with an 802.11b/g/n transceiver front-end is demonstrated. The switch achieves an insertion loss of 0.4 dB in transmit mode and 0.1 dB in receive mode. The entire receiver chain from antenna to baseband output achieves a measured noise figure of 3.6 dB at 2.4 GHz. The switch has a P_{1dB} greater than 30 dBm by employing a substrate isolation technique without using deep n-well technology. The switch employs a 1.2 V supply and occupies 0.02 mm^2 of die area.**

***Index Terms*—CMOS, T/R switch, transceiver, wireless LAN.**

I. Introduction

THE fast growth of wireless local area networks has spurred the need for cost reduction and high levels of integration. The increased integration eliminates many board level components which is the key to low-cost, small area wireless systems. Increased sales have placed wireless radio modems into more products and have driven down the form factor together with the cost. Some of the largest contributors to the cost and overall footprint of the radio modem are the off-chip components including low noise amplifiers (LNAs), power amplifiers (PAs), transmit/receive (T/R) switch, DC-DC converters, etc. Recent publications show a trend of integrating the LNA, PA and T/R switch together on a single die.

Fig. 1 shows the function of the T/R switch in the integrated transceiver. In the RX mode, the T/R switch connects the receiver to the antenna providing high impedance to the TX side. In the TX mode, the switch connects the transmitter to the antenna and provides high impedance to the RX side. To date, no fully integrated CMOS T/R switch has been reported with adequate linearity (1 dB compression point, P_{1dB}) and low insertion loss.

M. Yeh and Z. Tsai [1] demonstrated a floating body technique. However, the reported P_{1dB} is only 20 dBm, which is inadequate to meet WiFi requirements. Also, the insertion loss is more than 1 dB and the switch is stand-alone. N. Talwalkar et.al [2] also showed the need for a high impedance substrate achieving an insertion loss of more than 1.5 dB in RX and TX mode. This switch is stand-alone and not integrated with a transceiver.

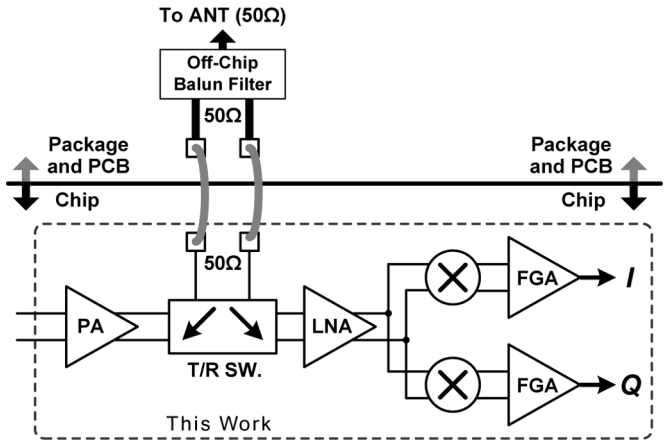

Fig. 1. Integrated transceiver front-end shows the integration of T/R switch.

The solution presented in [3] is promising and the T/R switch has been integrated with the transceiver but the TX mode insertion loss is 1.8 dB, which is undesirable for the efficiency of the transmitter. It also has only 15 dB isolation to the RX in the transmit mode. This may degrade the reliability of the LNA input devices, which are typically low voltage transistors and can break-down in the presence of high voltage swings at their gate. The solution presented in [4] also has the T/R switch integrated in the transceiver. It has better TX mode insertion loss than [3], but the integration of the T/R switch degrades the PA output power by 1 dB because the RX isolation in the TX mode is not sufficient.

The measured insertion loss of the switch architecture described in this paper is approximately 0.1 dB in the receive mode and approximately 0.4 dB in the transmit mode. With our implementation, the LNA NF increased by only 0.1 dB as compared to the LNA without the T/R switch. Typical discrete component T/R switches have an insertion loss of approximately 1 dB and increase the cost of the solution. The integrated switch presented here consumes negligible silicon area (approximately 0.02 mm^2) and therefore has negligible cost.

Our approach introduces a substrate isolation technique through layout which enhances the power handling capability of the transmit side switch and also reduces the insertion loss.

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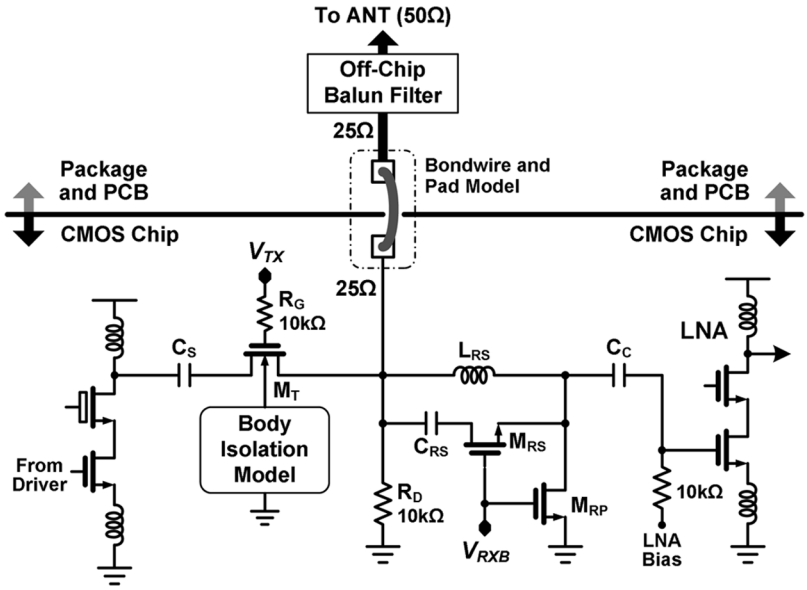


Fig. 2. Schematic of the integrated T/R switch (single ended representation).

The paper is organized as follows. In Section II, the principles and the target specification of T/R switch design are presented. Section III describes the T/R switch design. Section IV explains T/R switch operation while Section V presents measured results. Section VI concludes the paper.

II. Design Consideration

An efficient transmit line-up requires a transmit switch that does not limit the compression in the TX mode. The 1 dB compression point of the switch should be greater than that of the power amplifier. During the transmit mode, high isolation to the receiver is required for the following reasons.

1) High isolation of the receiver during the transmit mode reduces the loss of power from the transmitter to the receiver. This affects transmitter efficiency.
2) High isolation to the receiver protects the LNA input devices from the large voltage swings at the transmitter output.

Transmitter isolation in the receive mode is another important consideration in the T/R switch design. If the isolation of the transmitter is not adequate, a part of input signal will couple to the transmitter and will degrade the noise figure of the receiver. Also, the return loss of the T/R switch in the receive mode should be adequate to limit the reflection of the input signal in the receive mode. Another important factor in T/R switch design is the switching time. The switching time is defined as time from when the control signal changes until the RF signal is stabilized within 0.5 dB of the final value.

III. Design and Implementation

The specifications for the T/R switch design for 2.4 GHz 802.11b/g application are summarized in Table I. Other criterion which should be taken into account during the switch design include:

1) performance degradation at high temperatures;
2) robustness with respect to mismatches and large reflections at the antenna.

TABLE I
Target Specifications for T/R Switch

Specifications	Target Value
Operating frequency	2.4-2.484 GHz (WiFi b/g)
Return loss	> 10 dB
Insertion loss (TX mode)	< 0.5 dB
Insertion loss (RX mode)	< 0.2 dB
Isolation (TX mode)	> 25 dB
Isolation (RX mode)	> 20 dB
Linearity (P_{1dB})	> 30 dBm
Switching time	150 nsec

The full circuit schematic (single ended representation) of the T/R switch is shown in Fig. 2. Different architectures were chosen to implement the transmit/receive functions in the integrated transceiver. This is because the requirements for transmit and receive modes are very different. As can be seen in Fig. 2, the receive switch is merged with the LNA input matching.

A differential output impedance of 50 ohm was chosen to meet the reliability of the power amplifier. Lower output impedance enables the power amplifier to deliver the required power at a lower voltage swing, reducing the reliability issue for the T/R switch devices and the PA output devices. This dictated the LNA input impedance to be 50 ohms differential. The bond-wire inductance and the pad model were absorbed in the T/R switch design. The only off-chip component used in the 802.11b/g/n transceiver solution was an off-chip balun-filter. The DC voltage at the antenna is 0 V and is established by a resistor $\mathrm{R_D}$ as shown in Fig. 2. AC coupling capacitors were employed at both the PA output (Cs) and the LNA input (Cc).

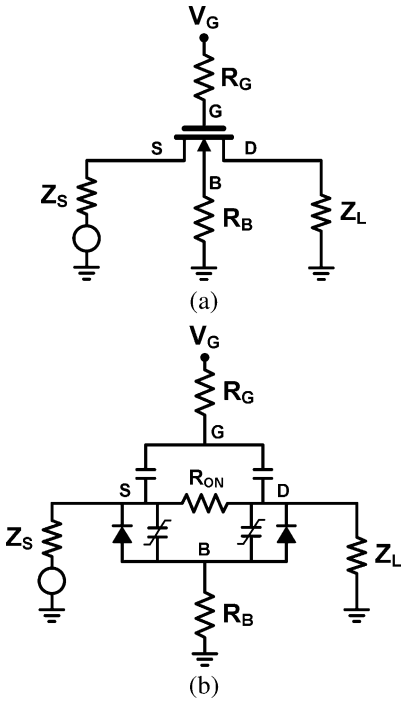


Fig. 3. (a) nMOS transistor switches. (b) Equivalent model.

Details about the switch in the TX mode and the RX mode are described in the following subsections.

A. TX Mode

As shown in Fig. 2, an nMOS transistor was employed in the transmit side of the switch. An equivalent circuit model of a nMOS switch is shown in Fig. 3.

As shown in [5], if the equivalent capacitance associated with all the nodes in a MOS transistor can be neglected and the source and load have the same impedance, the insertion loss of the MOS transistor with ON resistance of $\mathrm{R_{ON}}$ can be given by the following equation [5]:

$$IL = \left(\frac{R_{\mathrm{ON}} + 2Z_0}{2Z_O}\right)^2 \text{ if equivalent capacitance} = 0. \quad (1)$$

Z_O is the characteristic impedance. The dependency of the insertion loss on the transistor width and the associated capacitance at each node in the device can be found in [5]. Equation (1) is true only when the body impedance is infinite.

To achieve a high body impedance and decrease the RF power coupled to the bulk we increased the substrate impedance by blocking the P implants close to the switch devices. The substrate connections were placed far from the nMOS switch. Additionally, the high body impedance prevents the source-body and drain-body diodes from forward biasing, which would degrade power and linearity. The large isolating body resistance allows these junction capacitors to bootstrap the diodes.

Body Isolation Technique: As described above, a high body impedance is required for high linearity and low insertion loss. Fig. 4 shows two differential nMOS transistors whose bodies are remotely biased through a high resistivity P substrate. A 3-D EM simulation was performed to measure the substrate impedance for various distances of substrate connection from the nMOS transistors. The result is shown in Table II. The region between the transistors and substrate biasing contact employs a mask which blocks the P-well implant. This mask is typically used to realize on-chip high-Q inductors. By employing this mask layer, the bias of the body to ground is through the high resistivity P substrate.

TABLE II
THREE-DIMENSIONAL BODY ISOLATION ANALYSIS FOR T/R SWITCH

Transistor Size (μm)	Body Area (μm)	Clearance (μm)	Space (μm)	Switch P_{1dB} (dB)	Switch S_{21} (dB)
10x16	12x17	25	20	28.25	-0.656
10x16	12x17	50	20	28.15	-0.656
10x16	12x17	100	20	27.8	-0.656
10x16	12x17	150	20	27.46	-0.655
10x32	12x34	25	20	33.51	-0.394
10x32	12x34	50	20	33.44	-0.395
10x32	12x34	100	20	33.16	-0.395
10x32	12x34	150	20	32.63	-0.400
10x32	12x50	25	20	32.11	-0.412
10x32	12x50	50	20	31.83	-0.413
10x32	12x50	100	20	31.42	-0.412
10x32	12x50	150	20	30.72	-0.416

As can be seen in Fig. 4, the three design parameters in the analysis to determine the substrate impedance are *body area, clearance,* and *space* between the two bodies. The *body area* is the area of the isolated P-well of the local body of the nMOS switch transistors. The *clearance* is the distance from the isolated local P-wells to the global P-well region. The *space* is the distance between the two transistors. Generally, a larger *clearance* and *space* result in a larger body impedance, whereas a larger *body area* results in a smaller impedance (for a given *clearance*). There is some tradeoff between switch insertion loss and compression point when the transistor body area is increased.

Multiple wide metal lines are required to carry the large signal current for the transmitter. Parasitic fringing capacitive between drain and source nodes from these metal lines, as well as the capacitive coupling through the P-well, needs to be sufficiently small to achieve good isolation in the OFF state. This is accomplished by increasing the space between transistor fingers and minimizing the drain/source diffusion area. With the enlarged spacing, separate drain/source regions of succeeding fingers are separated and do not increase diffusion area. The expansion of transistor fingers results in a larger *body area* which lowers the body impedance. A balance between off isolation and $\mathrm{P_{1dB}}$ was made.

We find through simulation that increasing the *clearance* initially increases the substrate impedance but eventually lowers it when made too large. The exact mechanism is not understood. Table II summarizes a variety of tradeoffs while varying the three dimensions outlined in this section. The gray area is the chosen configuration.

The layout of the nMOS transistor interconnect was chosen to reduce $\mathrm{C_{ds}}$. This effects the isolation provided by the switch in the off-state. Another tradeoff is between insertion loss and the isolation. As can be seen from (1), using a larger switch

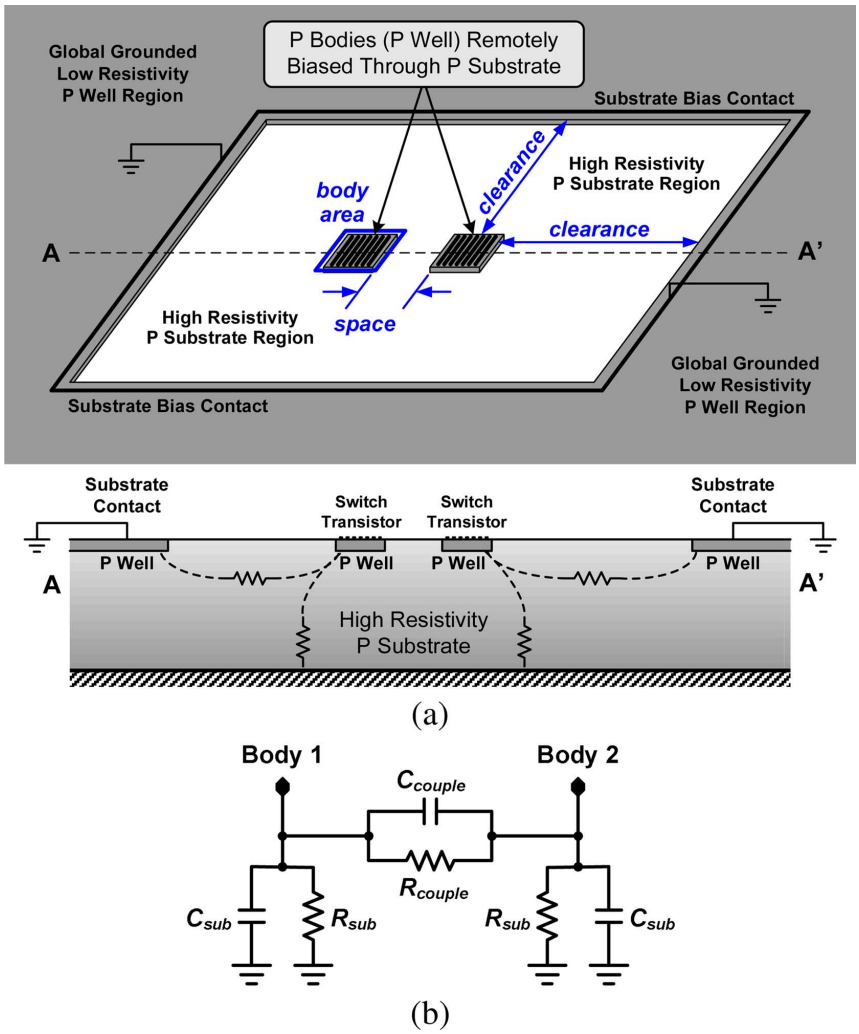


Fig. 4. (a) Body isolation technique. (b) Frequency independent model for parameter extraction.

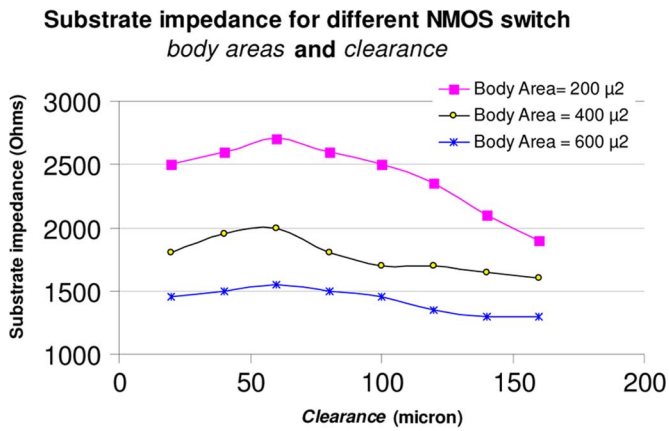


Fig. 5. Substrate impedance for different nMOS switches well areas and distance to the substrate connection.

decreases the insertion loss (less R_{on}) but also decreases the isolation by increasing device capacitance. The final distance to the substrate connection and the well area were chosen as a tradeoff between silicon area and substrate impedance, which affects the insertion loss and isolation as mentioned above. The final chosen parameters were Transistor Size $= 10 \times 32\ \mu$, Body Area $= 400\ \mu^2$, Clearance $= 50\ \mu$, Space $= 20\ \mu$. The final simulated impedance was approximately 1.8 KOhms. Final device sizes were chosen based on simulations results for insertion loss and isolation.

Fig. 6(a) shows the layout of the differential T/R switch. The substrate connection is on the outer ring which is 50 μaway from the devices (clearance in Fig. 4). The entire area was filled with the blocking "mask" layer in order to achieve high resistivity of the substrate as mentioned before. Fig. 6(b) shows the individual switch. The T/R switch does not carry DC current but needs to carry the AC current required to transmit approximately 25 dBm of power. The peak AC current for this power level in a 50 Ω system is 125 mA for each side in the differential switch. In order to carry this current, multiple layers of metals were stacked up in the layout as shown in Fig. 6. However, this introduces a significant amount of fringe capacitance between the source and the drain which in-turn affects the switch isolation. In order to mitigate this problem, we chose a larger body area as mentioned before so that the drain and source of the transistors can be placed far apart in the layout. The complete operation of the T/R switch is described in detail in Section IV.

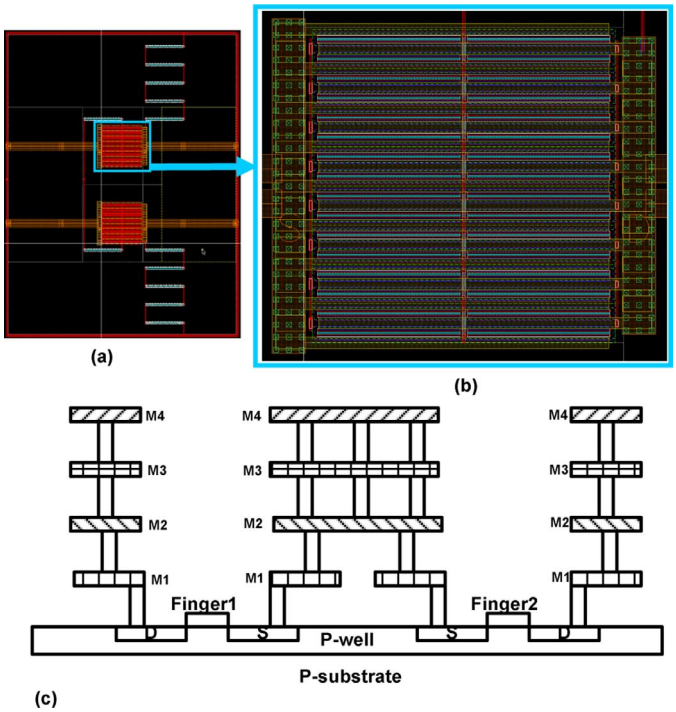


Fig. 6. (a) Differential switch layout. (b) Layout for one switch. (c) Metal stack-up on different fingers to carry the required AC current.

B. RX Mode

A different architecture was designed to implement the receive switch. A source degenerated series matched LNA was employed in the receiver design.

The receive side switch was merged with the LNA matching network. This reduces die area and lowers insertion loss compared to using a series switch. Fig. 2 shows the LNA has an AC coupling capacitor C_c and series matching inductor L_{RS}. The principle is to put the capacitor C_{RS} and switch M_{RS} in parallel with the series matching inductor LRS to form a high impedance parallel resonant network when the switch is in TX mode. Another switch, M_{RP}, is employed after this network to attenuate the TX signal to improve isolation. To reduce area, a differential custom inductor for the LNA was designed. This inductor requires less area than two separate inductors. Fig. 7 shows the layout of this inductor.

The layout of the custom inductor is shown in Fig. 7. Pin is connected to Pout and Nin is connected to Nout. This inductor is the first element in the receive path in the Integrated Transceiver Chip. Any loss in the inductor directly contributes to the receiver noise figure when the transceiver is in the RX mode. A 3-D field simulation was performed in order to accurately determine the value of the series resistance of the inductor. Two metal layers were stacked up in the layout of this inductor to keep the series resistance low. The proximity of the coils produced significant fringing capacitance between the two sides of the inductor, which decreased the self resonance frequency (SRF). Enough distance was maintained between the coils to keep the SRF of the inductor well above the frequency of operation.

Fig. 8 shows the low noise amplifier half circuit. A series matched source degenerated LNA was used in the receiver [6].

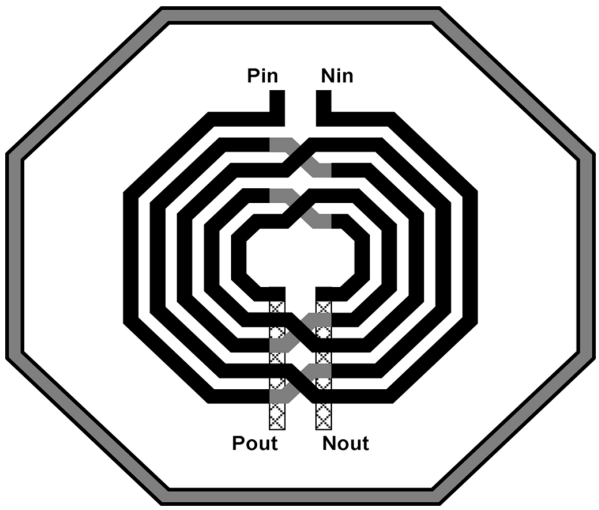


Fig. 7. Custom inductor design for series matching.

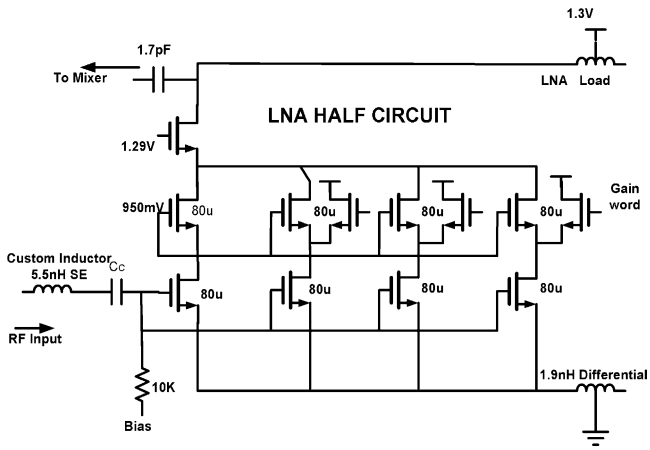


Fig. 8. LNA half circuit.

The custom inductor shown in Fig. 7 was used for the series matching of the LNA shown in Fig. 8. In order to achieve multiple gain steps, current steering was used in the LNA. As shown in Fig. 8, different outputs of the LNA are turned on-off depending upon the gain state of the receiver. One advantage of this current steering method is that S11 of the receiver remains substantially the same for different gain steps. To decrease the impact of the bulk capacitance, resistors of 5 KΩ were used between bulk and the source (not shown in Fig. 8). An 830 fF coupling capacitor was used at the input of the LNA, while a 1.7 pF capacitor was used between the LNA and the mixer. A 1.9 nH differential inductor was used for source degeneration. The input devices of the LNA were optimized for good noise figure and input matching. The LNA cascode device was biased at approximately 950 mV. The LNA draws 9 mA of DC current from a 1.3 V supply.

In order to mitigate ESD issues, a secondary ESD structure was employed at the gate of the LNA input devices (not shown in the picture). The transceiver passes the standard HBM ESD testing and accelerated oven burn-in testing.

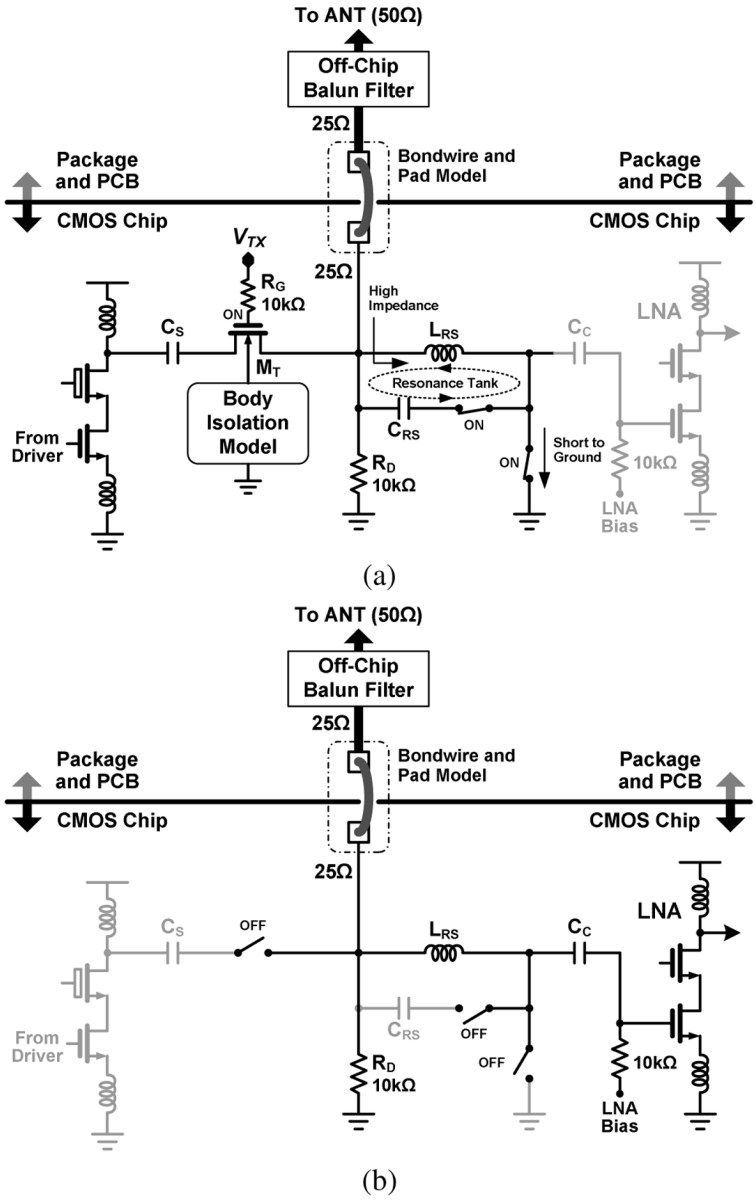


Fig. 9. (a) T/R switch operation in the Transmit mode. (b) T/R switch operation in the Receive mode.

IV. T/R Switch Operation

TX Mode Operation: The TX mode operation of the T/R switch is shown in Fig. 9(a). In the TX mode, $\mathrm{M_T}$ is ON, which connects the power amplifier output to the bond pads. The switches $\mathrm{M_{RS}}$ and $\mathrm{M_{RP}}$ are turned ON. This creates a resonance tank at the input of the receiver. This parallel resonance tank isolates the receiver side from the transmit side. The quality factor of this tank is determined by the Ron of $\mathrm{M_{RS}}$. The series capacitor $\mathrm{C_{RS}}$ was chosen such that the tank formed by $\mathrm{L_{RS}}, \mathrm{M_{RS}}$ and $\mathrm{C_{RS}}$ resonates at the frequency of interest. The quality factor of series inductor $\mathrm{L_{RS}}$ affects the NF of the receiver as well as the isolation in the TX mode. The high quality factor of this inductor improves the NF and the isolation in the TX mode.

However, in this scenario, the bandwidth is limited. In order to get acceptable noise figure in the receive mode, good isolation in the transmit mode and a large bandwidth of operation, a quality factor of 5 was chosen for the series matching inductor. As mentioned earlier, the floating bulk for the series switch in the transmitter ensures low insertion loss and a high compression point of the switch. In order to achieve reliable operation of the series switch, the Vgs and Vgd should always remain less than the breakdown limits of the transistor. This was achieved by putting a large resistor on the gate of the series switch. In this way, the gate/drain/source are bootstrapped together and there are no breakdown issues when the transmitter is ON. This also maintains a large overdrive voltage for RF signals, assuring low on resistance.

RX Mode Operation: The RX mode of operation of the T/R switch has been shown in Fig. 9(b). In the RX mode, the transistors $\mathrm{M_T}$, $\mathrm{M_{RS}}$, and $\mathrm{M_{RP}}$ are turned OFF. Therefore, transistor $\mathrm{M_T}$ provides a high impedance to the transmit side. In the receive side, the capacitor $\mathrm{C_{RS}}$ is disconnected and the resonant

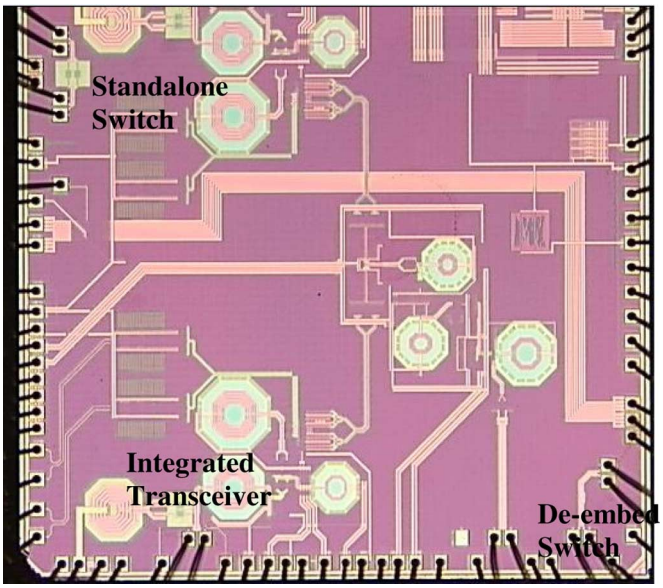


Fig. 10. Chip micrograph.

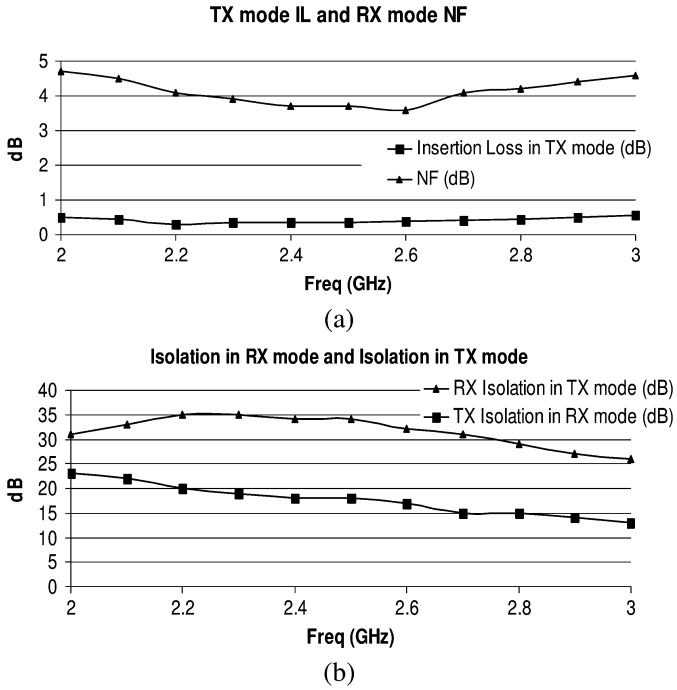


Fig. 11. (a) TX mode insertion loss and RX mode noise figure. (b) RX isolation in TX mode and TX isolation in RX mode.

tank which provided high impedance in the TX mode is non-existent. In this configuration, the LNA works as a series matched LNA as mentioned before.

V. Measurement Results

The integrated transceiver was fabricated in a 90 nm digital CMOS process. In order to measure the insertion loss and isolation of the transmit side switch, a separate de-embed structure was fabricated on the same die (Fig. 10). S-parameter measurements were performed on the switch structure and the de-embed structure and the difference between the S21 is calculated to be the loss through the series switch. The receiver gain of the entire 802.11b/g/n receiver was measured to be approximately 60 dB with a NF of approximately 3.6 dB. The P_{1dB} (in-channel) of the receiver was -29 dBm and the P_{1dB} (50 MHz offset channel) was -14 dBm. In the transmit mode, the total saturated power was approximately 24 dBm (with on-chip PA and T/R switch), which is close to simulations.

The stand alone T/R switch switching time was simulated to be <20 ns. Measured switching time is approximately 90 ns. Further simulations suggested that the increase in switching time is caused by the PA bias circuit.

No latch up issues were observed during various phases of testing. The ESD devices were placed far away from the transmit side high impedance substrate structure to avoid latch up.

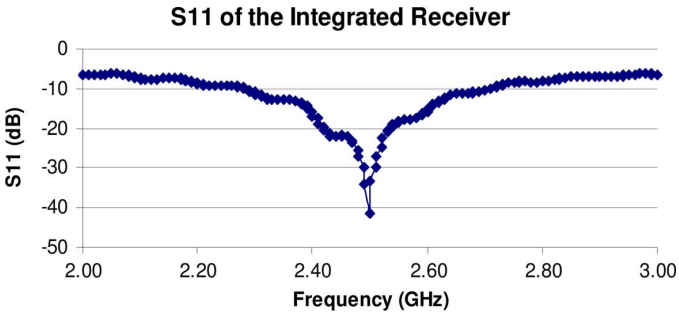
Fig. 10 shows the chip micrograph of the integrated transceiver. A separate transmit side switch and a de-embed structure were taped out in order to measure the insertion loss/isolation of the transmit side switch.

Fig. 11(a) shows the insertion loss of the switch in TX mode. The insertion loss was measured using the calibrated loss of the de-embed structure shown in Fig. 10. The loss is broadband and less than 0.5 dB across the band of interest. This insertion loss is that of the T/R switch stand-alone. A comparison between the measured output power of the Power Amplifier with and without (not described in this paper) the T/R switch suggests that the loss of the stand-alone T/R switch is in close agreement with the difference between the above mentioned measurements. Fig. 11(a) shows the noise figure of the receiver including the T/R switch, loading of the PA, low noise amplifier, passive mixers and base-band amplifiers. Fig. 11(b) shows the RX isolation in the TX mode. Isolation was measured by taking the difference between the receiver gain when the RX side of the T/R switch was ON/OFF. As can be seen in Fig. 11(b), isolation is broadband. Fig. 11(b) shows the TX isolation in the receive mode. This isolation was measured on the separate switch shown in Fig. 10. As mentioned earlier, if the isolation of the TX is low, receive power is lost to the TX side, increasing NF. Isolation in TX mode was lower than simulated because CDS was higher than expected. This is evident from the frequency response of the TX isolation which decreases as frequency increases. Fig. 12(a) shows S11 of the integrated receiver. Measured S11 is less than -10 dB from 2.3 GHz to 2.7 GHz.

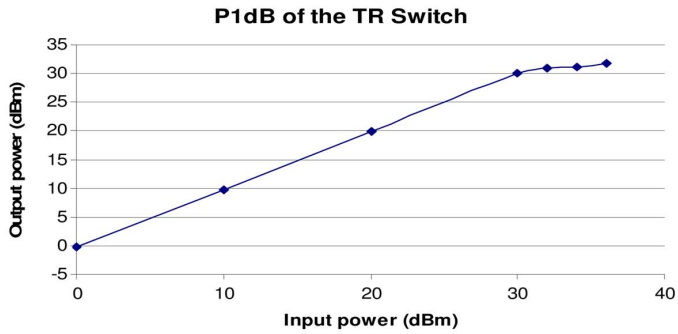
The T/R switch loss in the receive mode was characterized by comparing the measurement results of the LNA in the test chip in Fig. 10 (with the T/R switch) with another LNA having same topology and current consumption without the T/R switch. The difference between the two measurement results is the loss caused by the T/R switch in the receive mode.

The measured P_{1dB} of the T/R switch is approximately 30 dBm. Simulations show that the drain-body diode [Fig. 3(b)] begins to conduct at this point, limiting the performance.

Fig. 12(b) shows the measured P_{1dB} of the T/R switch. P_{1dB} was measured with the transmit side switch shown in the northwest corner of the chip micrograph in Fig. 10. The overall P_{1dB} of the transmitter was measured to be approximately 23 dBm and the P_{1dB} of the switch did not limit the P_{1dB} of the entire chain. The Transmit side switch loss was measured with increasing power levels at 2.4 GHz of frequency. It can be seen



(a)



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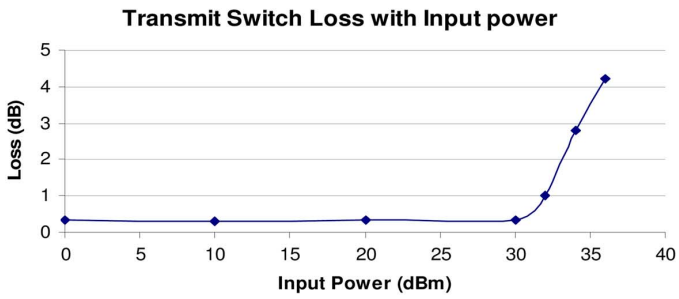

(c)

Fig. 12. (a) S11 of the integrated transceiver in the receive mode. (b) P_{1dB} of the T/R switch. (c) T/R switch loss versus power.

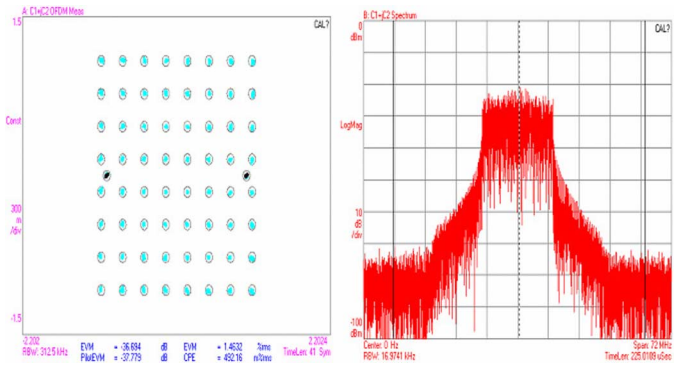

Fig. 13. EVM measurement results for the receive chain in the integrated transceiver.

in Fig. 12(c), the loss of the T/R switch with power levels remains constant until saturation occurs at more than 30 dBm of power. Table III summarizes the measured performance. Fig. 13 shows the measured EVM of the receive chain of the integrated transceiver.

The EVM of the transmitter with the T/R switch was measured to be better than −25 dB for up to 13.5 dBm output power without the use of pre-distortion.

TABLE III
MEASURED PERFORMANCE SUMMARY

Specifications	Measured Results
Operating frequency	2.4-2.484 GHz (WiFi b/g)
Return loss	> 10 dB
Insertion loss (TX mode)	0.4 dB
Insertion loss (RX mode)	< 0.2 dB
Isolation (TX mode)	30 dB
Isolation (RX mode)	16 dB
Linearity (P_{1dB})	30 dBm

TABLE IV
INTEGRATED SWITCH PERFORMANCE COMPARISON

	H. Darabi *et al.* ISSCC 2005 [3]	R. Chang *et al.* ISSCC 2007 [4]	This Work
TX Mode			
TX Insertion Loss (dB)	1.8	1	< 0.5
RX Isolation (dB)	15	TX power degraded by 1dB	> 30
P_{1dB} (dBm)	--	--	> 30
RX Mode			
RX Noise Figure (dB)	6	5.8	5.5*
TX Isolation (dB)	15	20	16
LNA DC Current (mA)	--	8.4	9
RX Supply Voltage (V)	--	1.8	1.3
CMOS Technology	0.18µm	0.18µm	90nm

* External balun-filter included.

VI. CONCLUSION

We have presented a low insertion loss T/R switch fully integrated with an 802.11b/g/n transceiver in 90 nm CMOS. A body isolation technique was used to decrease the substrate loss of transmit switch. The receiver switch was merged with the LNA architecture consuming very little area and degrading the noise figure only by 0.1 dB. By modeling the substrate impedance, optimum layout distances were chosen for this technology. The integrated transceiver achieves a total noise figure of 5.5 dB with an external balun-filter. The insertion loss of the series switch in the transmitter is less than 0.5 dB and has limited impact on the transmitter performance. The integrated WiFi b/g/n solution uses only one external component (balun-filter) in the RF signal path. The total silicon area consumed by the T/R switch is less than 0.02 mm2. The switch exhibits better than 30 dB isolation to the receiver in the TX mode and has better than 30 dBm of P_{1dB} in the transmit mode. Table IV presents recently reported performances of the 2.4 GHz CMOS T/R switches.

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