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Anomalous latchup failure induced by on-chip ESD protection circuit in a high-voltage CMOS IC product

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Abstract

Latchup failure induced by electrostatic discharge (ESD) protection circuits occurred anomalously in a high-voltage IC product. Latchup issues existed at only three output pins, two of which belonged to the top and the other to the side. The layouts of top and bottom output pins are identical, and side output pins have another identical layouts. In our experiments it was found latchup of two top output pins were originated from the latchup of the side output pin, and therefore heat-induced latchup aggravation issue must be noticed during latchup test. Furthermore, large power line current (Idd) existed during triggering this side output pin and led to subsequent latchup. After thorough layout inspection, the layout of this side output pin is identical to all other side output pins except that it has an additional N-well (NW) resistor of gate-triggered high-voltage PMOS beside. It was later proved by engineering experiments that this NW resistor is the origin of inducing latchup in this product, and a new mechanism was proposed for this latchup failure. Improvements and solutions were also provided to successfully solve the latchup issues of these three output pins.

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1. Introduction

Technological advances in ULSI and high-voltage devices have made possible the developments of high-voltage integrated circuits (HVICs). However, with more lightly doped drain junction in order to sustain high enough breakdown voltage, accompanied with higher operating voltage (and resultant high power dissipation), the electrical overstress (EOS) is becoming more severe in high-voltage devices and poses serious threat to device reliability, such as electrostatic discharge (ESD) and latchup.

In this paper, we present an anomalous latchup failure phenomenon of a HVICs. Of all layout-similar output pins, only three pins showed latchup failure under JEDEC Standard 78 test [1]. In later experiments it was found latchup of the first two pins were induced by the latchup of the third pin. Large power line current (Idd) existed when triggering this third pin and latchup occurred. The large power line current was due to the turning on of high-voltage PMOSs (HVPMOSs) of ESD power clamp circuits, and the HVPMOSs were turned on due to negative-gate-biasing by injected electron flow building up voltage drop across the N-well (NW) resistor during the latchup trigger test. Preventing the turning-on of HVPMOSs by focused ion beam (FIB) cutting experiments resolved the large power line currents and subsequent latchup events during JEDEC current trigger test at the same time.

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2. Latchup phenomena and ESD protection circuits of the HVIC product

Latchup is a state in which low-impedance path resulted from an overstress that triggers a parasitic pnpn-silicon controlled rectifier (SCR) structure and persists even after removal of the triggering condition [2]. Since the power supply has then a low shunt impedance to ground during latchup events, large power line current (Idd) will exist between Vdd and ground (Gnd). Irreversible damage or malfunction would occur to the circuit with the existence of this low impedance state.

This product of study is a HVIC operating at 10 V. Gate-triggered HVPMOSs were deployed as Vdd-to-Vss ESD power clamp circuit for whole-chip ESD protection [4]. For IC products, 2kV HBM in ESD level and ±100 mA trigger level in JEDEC Standard 78 Test are required as general ESD and latchup specifications. The product had an ESD level of 3 kV and passed +100 mA test. However, three output pins failed −100 mA in latchup test and are referred here as pin A–C, respectively. The layout schema of the product is shown in Fig. 1(a). It should be noted that their layout are almost identical with all side output pins having same layout and all top and bottom output pins another same layout, as shown in the chip floor plan in Fig. 1(b).

During ESD qualification process, four ESD zap modes are tested [4], with positive and negative Vdd-to-Vss ESD stress in addition. In the two Vdd- to-Vss zap tests, internal circuits are vulnerable to ESD damage if there is no ESD power clamp circuit between Vdd and Vss. Therefore, in order to clamp the ESD voltage across Vdd and Vss power lines efficiently before internal circuits are damaged by ESD overvoltage, an ESD clamp circuit is needed between Vdd and Vss [4]. In this product, shortened gates to Vdd through a series resistor, HVPMOSs with their drains connected to Vss and sources connected to Vdd are used as an ESD power clamp circuit and named here as GRPMOSs, shown in Fig. 1(c). The GRPMOSs utilizes the parasitic capacitor Cgd of HVPMOSs and a NW resistor to comprise an ESD-transient detection circuit. The time constant is designed in the order of sub-microseconds (sub-μs). Therefore the resistance value of this NW resistor is quite large, in tens of kohms, because of small Cgd value. In negative Vdd-to-Vss ESD zap, the ESD current is conducted by the forward biasing of NW/P^+ parasitic diode. In positive Vdd-to-Vss ESD stressing, due to the sub-μs-order time constant, the gates of HVPMOSs remain low. Therefore, HVPMOSs are turned on to discharge ESD current. At normal circuit operation, the HVPMOSs remain off because, under normal power-on condition, the rise time of power-on voltage waveform is in ms-order, and the gate voltage of HVPMOSs can follow Vdd voltage in time and keep HVPMOSs off.

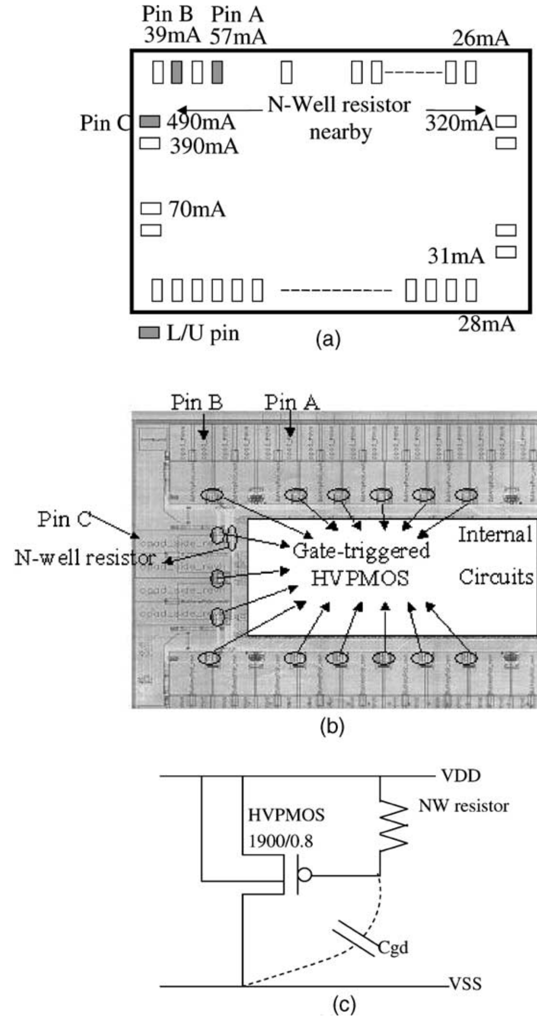

Fig. 1. (a) Whole-chip pin floor plan. Pins in gray are latched pins. Also shown are power pin currents during trigger in subsequent wafer-level latchup tests. (b) Chip floor plan. Output pins are consisted of same cells. (c) Circuit diagram of GRPMOS. The labeled width is the sum of 19 distributed HVPMOSs in parallel.

3. Failure analysis and experimental procedures

For the latchup of pin A and B, reviewing the layout reveals these two output pins to be identical to others on the top of the chip. Since latchup is highly layout dependent, there is no obvious explanation for the latchup of these two pins by layout comparison. For further investigation, we changed the pin test sequence to compare for the difference. Originally pin C was first latchup tested, followed by pin B and pin A. By testing pin A and B first, the outcome was quite surprising that no latchup at these two pins was found. As a comparison, the testing sequence was set to its original condition

and pin C latched this time with subsequent pin B and A latchup. This implies that the latchup events of these three pins are highly correlated with pin C's latchup. One assumption is that latchup of pin C results in substrate temperature raise. The latchup of pin A and B are thereby induced as an aggravated result from produced heat.

For further confirmation, we utilized a simple digital thermometer to measure surface temperature of the package. It should be noted that though the response of digital thermometer was slow compared to temperature change in package, and surface temperature between package and silicon might be quite different, measuring package surface temperature provided a fast observation in relationship between latchup resistance and temperature. Originally the surface temperature was 25 °C when IC was powered up to a steady state. Applying a trigger current to pin C induced large power line current (about 400 mA). Subsequent latchup and current-induced temperature raise (to about 110–130 °C) occurred as a result. At this temperature pin B and A latched in sequential latchup test. Increasing cool-down time between successive trigger from 1 to 5 s showed no latchup at pin A and B in the following sequential test even after latchup of pin C. Therefore, it was concluded that latchup of pin A and B was resulted from latchup of pin C. Resolving pin C latchup problem would also solve the following latchup of pin A and B simultaneously. From investigations performed above, thermal-induced latchup aggravation should be noticed during latchup testing.

In order to locate the latchup site, we used EMission MIcroscope (EMMI) in search for hot spots. Hot spots were later discovered by EMMI to be located within internal circuits, as shown in the right side of Fig. 2 and corresponding magnified layout of internal circuit is in Fig. 3, showing potential latchup paths formed by parasitic SCR. They were further verified by subsequent FIB experiments. As for improvements, Vdd and Vss guard bands (normally placed between I/O and internal circuits [3]) should be added with adequate widths and NW/P-substrate pickups should be placed in p–n–p–n SCR path to strengthen the latchup resistance of internal circuits [7].

Though the failure site was found by EMMI and proved by the subsequent experiments, the reason for large power-line current (Idd) during trigger that resulted in latchup remained unknown. It was assumed that devices was triggered to turn on and conducted large currents, therefore contributing to the detection of large Idd during trigger. Since the pin C was comprised of the same cell layout as other side output pins (as shown in Fig. 1), we focused on other subtle layout difference in order to distinguish layout of pin C from

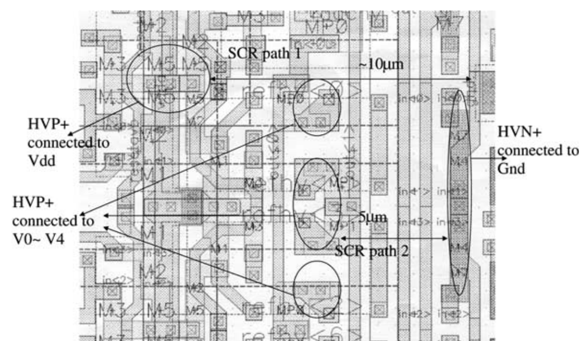

Fig. 3. Layout (fraction) of the internal circuits corresponding to hot spots of Fig. 2.

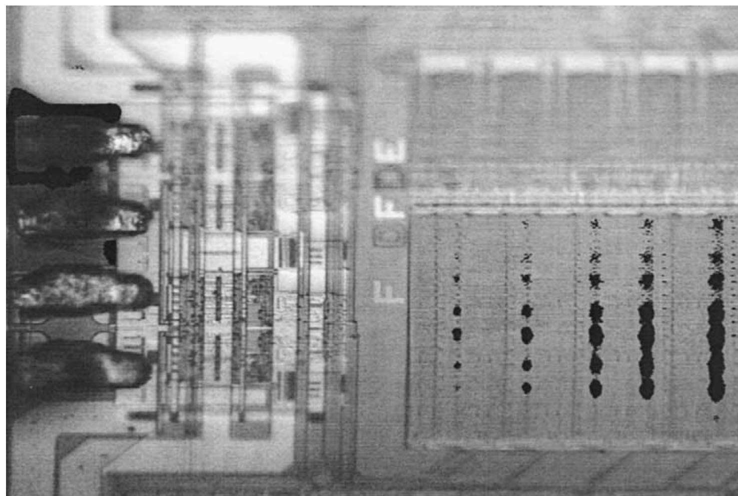

Fig. 2. EMMI of decapped samples during latchup.

others. After thorough comparison, NW resistor beside output cell was discovered and also shown in Fig. 1(b). The NW resistor was used as the resistor of GRPMOS ESD power clamp circuits and was shared by 19 HVPMOSs as a group. The NW resistor had one end connected to Vdd and another connected to the gates of HVPMOSs, as shown in Fig. 1(c) for circuit diagram and Fig. 4 for real circuit layout. For further latchup characteristic investigation, power line current during trigger was monitored and large Idd during trigger was found for pins with NW resistor of GRPMOS near by, recorded in Fig. 1(a). Another pin (referred afterwards as pin D) that is opposite to pin C and comprised of same side output cell and a NW resistor beside was also tested for trigger characteristics. The result also showed large Idd during trigger (~300 mA).

By using prolonged current trigger the EMMI showed hot spots on HVPMOSs that were shunted together, as shown in Fig. 5. Carefully examining the EMMI photo revealed that hot spots emerged for HVPMOSs of the same group, indicating HVPMOSs of this group were probably turned on at the same time. Combining the particular trigger characteristic of pin C with NW resistor beside and the EMMI hot spots on HVPMOS, GRPMOS should be substantially related to large Idd during trigger. Large Idd during trigger contributed from the turning-on of GRPMOS was assumed to be a failure origin, with subsequent heat production that finally led to heat-aggravated latchup. The cross-section view of a GRPMOS and NW resistor was shown in Fig. 6.

The proposed mechanism can be realized from Fig. 6. Since electrons were injected in negative trigger, and one N^+ node of NW resistor was connected to Vdd that is able to collect electrons, if the N^+ pickup between pad and the NW resistor was not enough to collect electrons efficiently, the remaining electrons may reach and flow

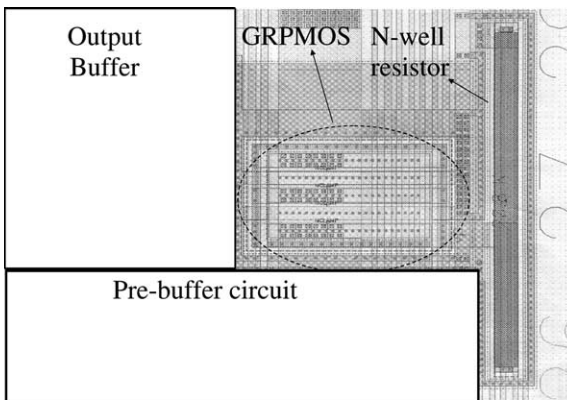

Fig. 4. Layout of the GRPMOS beside pin C. NW resistor was connected between gate of HVPMOSs and Vdd and was shared by 19 shunted HVPMOSs.

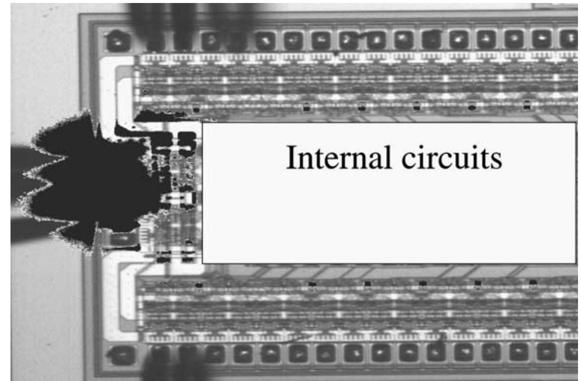

Fig. 5. EMMI photo when pin C was under prolonged trigger. Large Idd existed during trigger period. HVPMOSs with hot spots were in the same group sharing a common NW resistor.

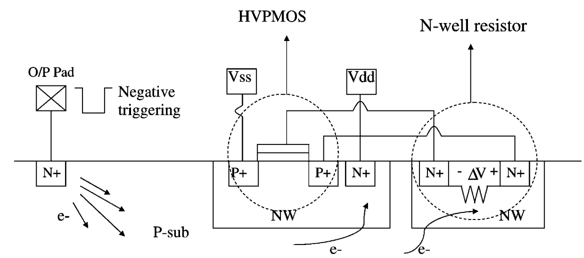

Fig. 6. Cross section of GRPMOS and NW resistor. Only one HVPMOS was shown where in actual the NW resistor is shared by 19 HVPMOSs.

through the NW resistor, then finally become collected by N^+ connected to Vdd at the end. This caused a voltage drop across the NW resistor. Since the sources of HVPMOSs were connected to Vdd and gates were connected to another end of NW resistor, the voltage drop between two ends of the NW resistor also appeared equally across gates and sources of HVPMOSs. If the voltage drop is large enough so that the Vgs of HVPMOSs is more negative (larger in magnitude) than threshold voltage, HVPMOSs may be turned on which explains why the hot spots appears exactly at the group of HVPMOSs belonging to same NW resistor. Since the NW resistor had quite large value, therefore, only small fraction of triggering electron flow is enough for causing voltage drop large enough to turn on PMOS. And since all HVPMOSs of the same group were gate-biased through this NW resistor, they were turned on as a whole in results. The total width of these HVPMOSs was 1900 μm, therefore the turning-on of these HVPMOSs can contribute to large current between Vdd and Vss. From the aforementioned experiments, it was known that the large current could give rise to temperature considerably and result in latchup degradation, finally leading to latchup of internal circuits. Examining

layout revealed that pin C had the nearest distance to the NW resistor and the least N^+ pickups surrounding since most upper area of pin C is blank on silicon substrate except metal line running over the bulk substrate, as compared with other output pins having enough N^+ pickups of neighboring pins surrounding. Therefore, triggering electrons injected from pin C had the largest quantity to reach the NW resistor and resulted in series of latchup-inducing events.

In order to verify our hypothesis, FIB was used to remove this electron flow path to prevent this e^- flow from building up a voltage drop across NW resistor and turning on HVPMOSs. We cut the NW resistor at both ends and shortened the gates of HVPMOSs to Vdd make sure that HVPMOSs are always kept at off state. This resulted in no large Idd during trigger and no hot spot emerged for FIB samples, shown in Fig. 7(a). As a comparison, we tested the aforementioned opposite side pin (pin D) with another NW resistor beside on same FIB-ed samples. Large current ($\sim$300 mA) and hot spots still existed, as shown in Fig. 7(b).

Therefore, from results of preceding experiments, we concluded that large Idd during trigger was due to the turning on of HVPMOSs, and it was originated from the HVPMOS gate–source voltage drop built up by electrons flowing across the NW resistor.

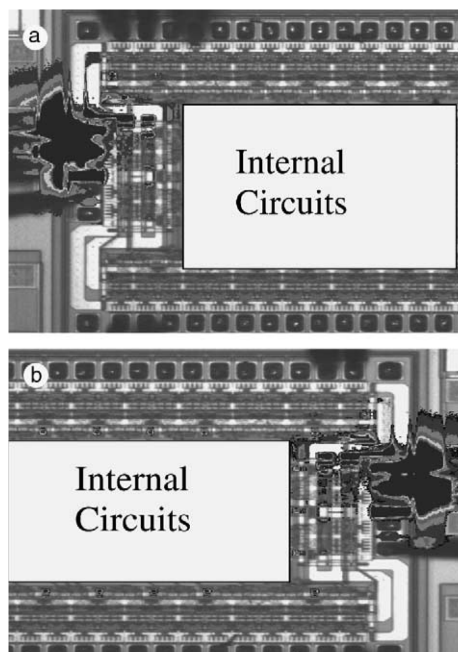

Fig. 7. (a) EMMI on wafer-level samples with NW resistor cut off and HVPMOSs' gates reconnected to Vdd. No hot spot on EMMI and no large Idd during trigger. (b) As a comparison, pin D of same samples were also LU tested. Hot spot and large Idd existed.

In our next revision the latchup improvements were performed abiding by the conclusion of our preceding failure analysis. In order to retain the same chip size the layout style in internal circuit pickups and distance from pad C to NW resistor of ESD power clamp circuits were kept unchanged. However, the N+ guard rings connected to Vdd surrounding the NW resistor altogether with whole-chip Vdd-Vss guard band were added as will be discussed further in next section. With this modification the next revision passed $\pm$100 mA without any latchup issue resurged.

4. Discussion

In order to realize the detailed behavior of injected carrier distribution in the substrate, TCAD process/device simulation [5,6] was also performed on the NW structure of pin C. The electro-thermal simulation with full coupling between the electrical and thermal equations is essential to accurately describe the behavior of the device in the high current region. The coupling between lattice temperature, current densities, impact ionization, mobility and electric field are important in simulating ESD/EOS phenomena in devices. The physical models used in electrothermal simulation are temperature-dependent thermal conductivity, temperature-dependent mobility, temperature-dependent carrier velocity saturation, and temperature-dependent impact ionization coefficient. Because two-dimensional process/device simulators were adopted, the layout of pin C was simplified into a two-dimensional structure. Meanwhile, all key layout parameters and doping profiles were kept the same. The schematic plot of the simulated structure is shown in Fig. 8(a). The N+ (connected to pad)/ P-sub-region forms a parasitic pull-down diode which acts as an electron injector in latchup test, and another N+ node of NW resistor connected to Vss through a coupling capacitor (representing Cgd of HVPMOS) is gate electrode of HVPMOS. Fig. 8(b) is the simulation result of HVPMOS gate voltage versus injecting current level. There is a certain portion of injected carriers, not flowing into the substrate pickups but collected by NW resistor, when triggering current is injected from the N+ injector. The injected carriers flow along NW resistor and establish voltage drop between Vdd terminal and the other terminal connected to PMOS gate with large enough injected carriers. This voltage drop raised high enough to turn on a PMOSFET sufficiently. From Fig. 8(b), it reveals that with increasing injected electrons, the gate voltage could drop rapidly beyond certain injecting level and lead to turn-on of HVPMOS. Because bipolar current gain is positive temperature dependent, both injected current and temperature couple into positive feedback process and induce rapid increase of both factors. This leads to rapid change of the gate voltage.

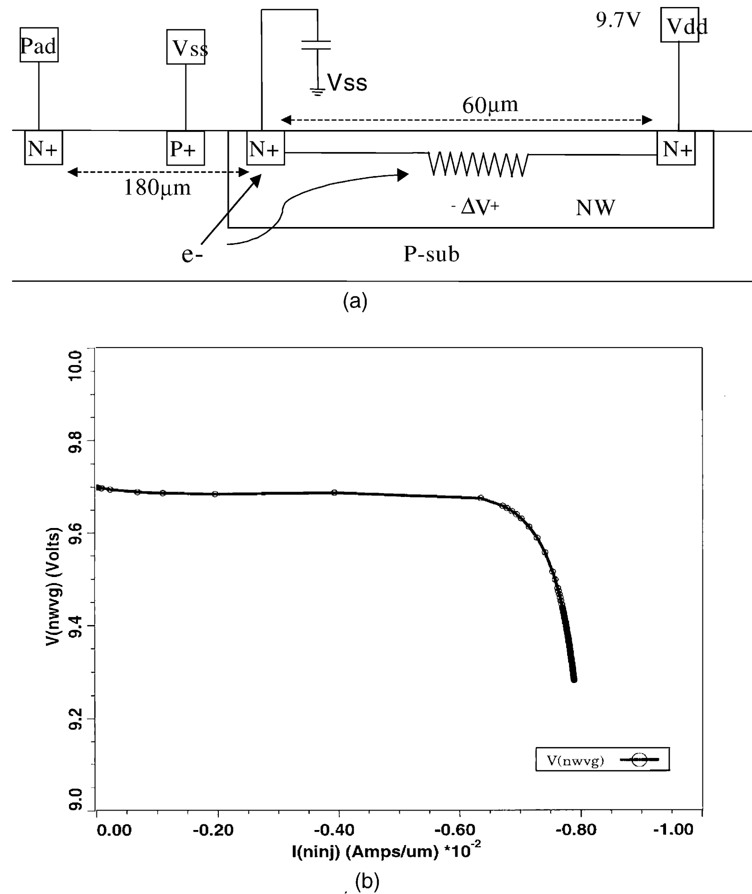

Fig. 8. (a) The schema of simulation structure. (b) Simulation results. The X-axis is the injected current level and the Y-axis is the gate voltage of HVPMOS.

Therefore, it is apparent that the EOS failure issue is actually induced by the turning-on mechanism of ESD power clamp device.

Since the root cause of latchup in this case is clarified to be the NW resistor, the modification to prevent the latchup failure can be done in several ways. It should be noted that these modifications also applies to other technology and products given the same failure mechanism. For large power line current during trigger to be diminished, HVPMOSs shall remain off during trigger. The first and most convenient method is to modify one mask (only metal layer) to shorten the gates of HVPMOSs of ESD protection circuits to Vdd to make them always off and conduct ESD currents in breakdown mode. However, degradation in ESD performance is expected. Another method lies in the key that the NW resistor will not build up enough voltage drop if there are not sufficient injecting carriers. In order to eliminate latchup issue while sustaining same ESD level, modification can be done by placing the NW resistor farther away from I/O cells and add N^+ guard rings [2]. Since the injected carriers from pad are recombined as they diffuse toward internal circuits, farther distance between latchup-sensitive devices and pad implies less injecting carriers to the latchup-sensitive devices and better latchup resistance. In addition, the N+ guard ring connected to Vdd surrounding the NW resistor can efficiently collect injecting electrons of negative trigger current before injected electrons are collected to the Vdd-terminal of NW resistor and result in voltage drop across it.

Though the gate-triggered structures have been widely used and proved to be efficient ESD protection circuits, the resultant LU failure caused by this structure has not been presented as authors' knowledge, and that the gate-biasing of MOS could only occur in gate-triggered PMOS since the NW is connected to Vdd at one end. In the case of gate-triggered NMOS, the NW resistor is connected to Vss and would not draw electron flow. Thus, there would be no voltage drop across NW resistor during normal trigger, and NMOS would not be biased to turn on.

5. Conclusion

From the experiments, we can conclude that the latchup event in this study was induced by large Idd-assisted latchup degradation resulted from the turning on of HVPMOSs in ESD protection circuit, and the turning on of the HVPMOSs is due to the voltage build-up of NW resistor by injecting electrons in latchup testing.

The improvements to LU failure in this case can be made in following ways. One is to increase the internal circuit robustness against latchup and another is to remove the trigger source that induced large Idd during latchup tests. In order to increase the latchup robustness of internal circuits the whole-chip Vdd–Vss guard bands should be added between I/O injector and internal circuits. Also suitable pickup should be added in internal circuits to prevent the parasitic SCR from turning on to produce latchup.

To remove the trigger source, since latchup in this case has originated from electrons flowing through NW resistor, the way to remove this trigger source is to eliminate this path. This could be achieved by removing NW resistor and use grounded-gate HVPMOS as whole-chip ESD protection. If NW resistor must remain intact for maintaining ESD performance, N+ guard ring connected to Vdd and surrounding this NW resistor can be added to collect the electrons to prevent them from turning on HVPMOSs. The latter was implemented and proved to work successfully in the new revision, validating the veracity of our work and theory.

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