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Improved Annealing Process for Electroless Pd Plating Induced Crystallization of Amorphous Silicon

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Electroless Pd plating induced crystallization of amorphous silicon (a-Si) thin films has been proposed for fabricating low-temperature polycrystalline silicon thin film transistors (LTPS TFTs). However, the current crystallization process often leads to poor device performance due to the large amount of Pd-silicide residues in the poly-Si thin films. It was found that the amount of Pd silicide increased with annealing time and temperature. In this study, a two-step annealing process was developed to obtain the appropriate amount of Pd silicide for inducing the crystallization of a-Si. The device characteristics were significantly improved by this two-step process. [DOI: 10.1143/JJAP.42.L895]

KEYWORDS: thin-film transistor, amorphous silicon, polycrystalline silicon, metal-induced crystallization, electroless plating and physical vapor deposition

Low-temperature polycrystalline silicon thin film transistors have attracted considerable attention for active matrix liquid crystal display (AMLCD) application due to their good electrical properties and capability of integrating peripheral circuits into inexpensive glass substrates.[1,2] Since poly-Si thin film transistors (poly-Si TFTs) should be fabricated on glass substrates to reduce the fabrication cost, intensive studies have been carried out to reduce the fabrication temperature of polycrystalline silicon (poly-Si) thin films. Metal-induced crystallization (MIC) of a-Si has been one of these efforts. In MIC, a metal thin film (Ni,[3–6] Pd[7] or Al[8]) is deposited on top of an as-deposited a-Si film and this is followed by crystallization at a temperature lower than 600°C. Nevertheless, metal films are generally deposited by the physical vapor deposition (PVD) method, which is still very time-consuming and expensive in terms of equipment cost.

To reduce the process time and cost, in previous studies, we proposed an electroless Pd plating method to induce crystallization of a-Si thin films.[9,10] After sample was annealed at 530 and 550°C, two kinds of needlelike grains were found. The direction of the primary grain was along ⟨211⟩ and the growth of the secondary grain occurred along the ⟨011⟩ direction, which was normal to the primary grain growth direction. However, the leakage current increased significantly due to the Pd-silicide residues in the channel of the poly-Si TFTs. In this study, a two-step annealing process was used to reduce Pd-silicide contamination and thus improve the TFT performance.

Si wafers were used in this study. After a wet oxide layer was grown, silane-based a-Si films of 100 nm thickness were deposited by a low-pressure chemical vapor deposition (LPCVD) system. The wafers were cleaned in a diluted HF solution, and then immediately dipped into a plating solution of $PdCl_2$ (1 g/ℓ) and HCl (100 ml/ℓ) for 10 min.[9] The following two methods were employed to induce the crystallization of a-Si films.

(a) conventional furnace annealing (CFA): Samples were annealed in nitrogen atmosphere at 550°C for 18 h to crystallize the Si films. After annealing, the unreacted Pd clusters were removed by chemical etching.

(b) Two-step annealing: Samples were preannealed to form the appropriate amount of Pd silicide. The unreacted Pd clusters were removed by chemical etching, then the samples were annealed in nitrogen atmosphere at 550°C for 18 h.

A post rapid thermal annealing (RTA) treatment at 850°C for 75 s was used to improve the crystallinity and uniformity of both Si films. The TFT devices were then fabricated by defining the active areas on the poly-Si films. A 100-nm-thick SiO_2 film for gate oxide was deposited by plasma-enhanced chemical vapor deposition (PECVD). Subsequently, a 200-nm-thick SiH_4-based a-Si film was deposited at 550°C by the LPCVD system and lithographically patterned as the gates. The gate electrode and source/drain were doped by self-aligned phosphorus implantation at a dose of 5×10^{15} ions/cm^2. Then dopant activation and crystallization of a-Si gate electrodes were performed at 850°C for 30 min in N_2 atmosphere. After the 200-nm-thick tetraethylorthosilicate (TEOS) oxide deposition, contact holes were formed for gate, source and drain electrodes. Electrode pads were formed after the Al film deposition. Sintering was performed at 400°C for 30 min. Then the 4 h NH_3 plasma treatment was adopted to passivate the devices.

Figure 1(a) shows the typical characteristics of CFA-TFT devices. Their performance was very poor. Scanning electron microscopy (SEM) was used to study their poor performance of CFA poly-Si. Figure 2 shows the SEM images of Secco-etched CFA poly-Si annealed at 550°C for 18 h. There were two kinds of needlelike grains on the Si films as shown in Fig. 2(a). The direction of the primary grain was along ⟨211⟩ and the growth of the secondary grain occurred along the ⟨011⟩ direction, which was normal to the primary grain direction.[9,10] Nevertheless, not all of the a-Si film was transformed to c-Si. As shown in Fig. 2(a), between neighboring needlelike Si grains, there still remained some gaps, which were uncrystallized a-Si regions that had been etched away by Secco solution. However, in addition to these a-Si regions, there were numerous holes on the CFA poly-Si film as shown in Fig. 2(b). The high-resolution micrograph of these holes in Fig. 2(c) shows some Pd clusters around the holes. Therefore, we believe that the holes in Fig. 2(b) were Pd silicide that had been etched away by Secco solution.

To improve the device performance, Pd-silicide contamination must be reduced since it traps charge carriers and builds up potential barriers to the flow of the carriers.

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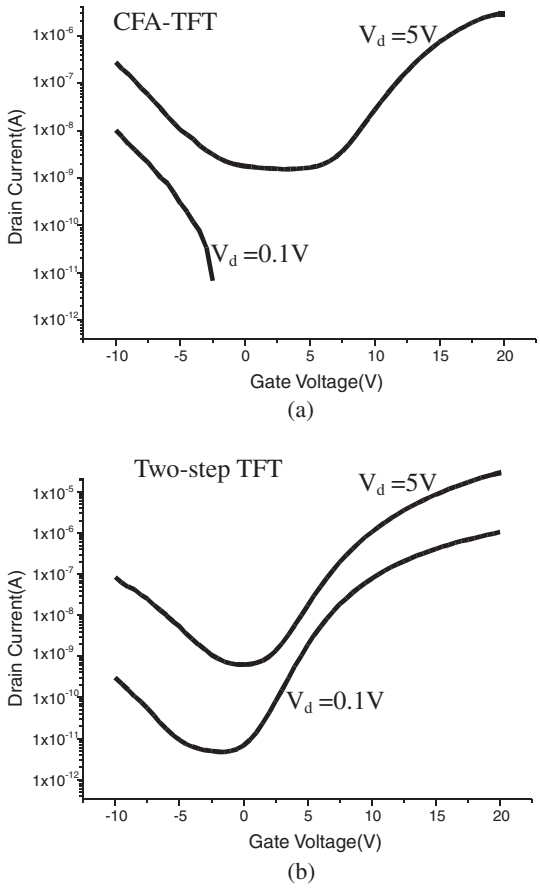

Fig. 1. The $I_d - V_g$ characteristics of (a) CFA poly-Si TFTs and (b) two-step poly-Si TFTs.

Furthermore, the presence of these potential barriers and additional scattering at the boundaries degrade the TFT performance.

The studies of the CFA Si surface morphologies and device characteristics described above clearly showed that Pd could lead to the formation of poly-Si at lower temperature, but it also caused the formation of Pd silicide, which degraded the device characteristics. For this reason, a two-step annealing process was developed to obtain the appropriate amount of Pd silicide to induce the crystallization of a-Si.

In the two-step annealing process, two annealing steps were carried out after the electroless Pd plating. The first annealing step was performed in nitrogen atmosphere to form silicides either in a RTA furnace (pre-RTA) or a CFA furnace (pre-CFA). Then, the unreacted Pd clusters were removed by chemical etching. The second annealing step was carried out in a conventional furnace at 550°C for 18 h to crystallize a-Si.

The pre-RTA process was used as the first annealing step because it can control the annealing time precisely. It was performed at 400–700°C for 15 s. After the second CFA annealing step, SEM was used to examine the surface of the Secco-etched poly-Si films. As shown in Figs. 3(a)–3(c), the number and area of the silicide holes decreased with decreasing pre-RTA temperature, which is consistent with the observation that the formation of Pd silicide decreases with decreasing temperature. However, even with the lowest pre-RTA temperature (400°C), there was still a high amount

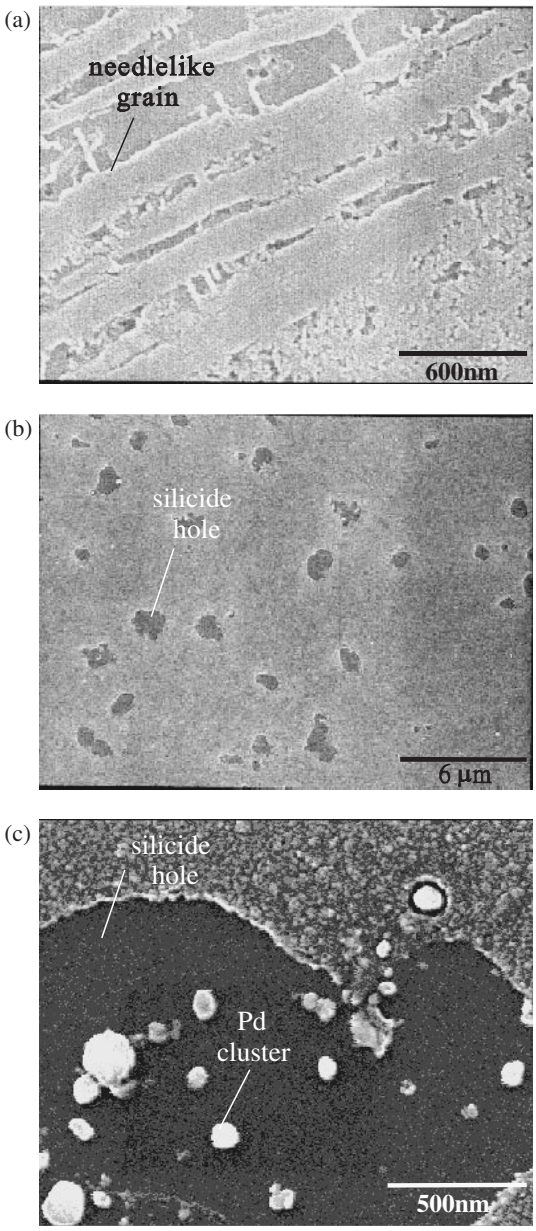

Fig. 2. SEM images of Secco-etched CFA poly-Si annealed at 550°C for 18 h. (a) the image of two kinds of needlelike grains. The direction of the primary grain was along ⟨211⟩ and the growth of the secondary grain occurred along the ⟨011⟩ direction. (b) the holes on the CFA poly-Si films. (c) the high-resolution micrograph of the holes showing Pd clusters around the holes.

of Pd silicide. Thus, the device characteristics were still poor.

To reduce the annealing temperature, a CFA furnace was used for the first annealing step because the lowest operating temperature of our RTA furnace is 400°C. Samples were annealed at 200°C for 30 min. After the second CFA annealing step, the surface of the Secco-etched poly-Si films was examined by SEM. As shown in Fig. 3(d), silicide holes were difficult to find on the poly-Si surface. The poly-Si grains were still needlelike, such as those shown in Fig. 2(a), but with a lower number of silicide holes. Therefore, 200°C pre-CFA was selected as the first annealing step for the two-step annealing process.

The device characteristics of two-step annealing poly-Si films are shown in Fig. 1(b). Compared with CFA poly-Si

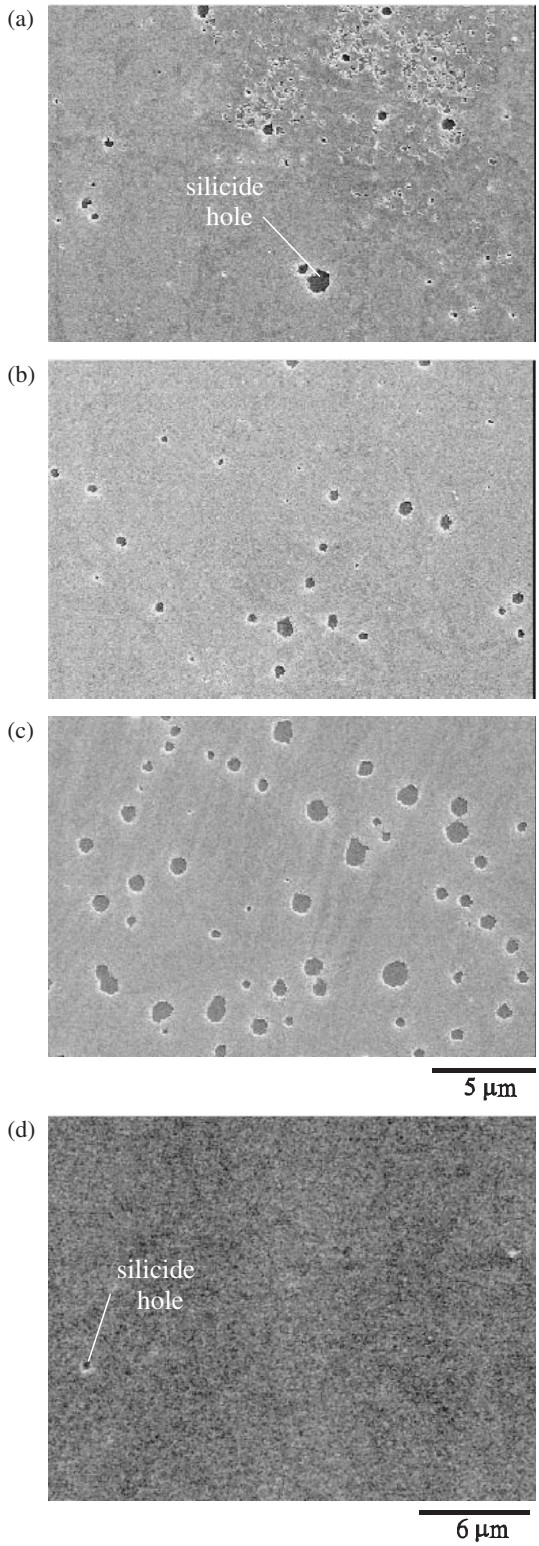

Fig. 3. SEM images of Secco-etched poly-Si annealed at 550°C for 18 h with various preannealing temperatures and times: (a) pre-RTA 400°C for 15 s, (b) pre-RTA 500°C for 15 s, (c) pre-RTA 600°C for 15 s and (d) pre-CFA 200°C for 30 min.

TFTs (Fig. 1(a)), the performance of two-step poly-Si TFTs was significantly improved. The two-step TFTs had a higher mobility ($12.88\,cm^2/V{\cdot}s$), a smaller subthreshold slope (1.95 V/dec) and a smaller leakage current/channel width (6.10 pA/μm).

After investigating the relationship between annealing conditions (temperature and time) and the amount of Pd silicide in poly-Si films, this study has led to the development of an effective process for preparing poly-Si films. It was found that poor device performance caused by Pd-silicide residues could be minimized by a two-step annealing process. In the two-step annealing process, two annealing steps were carried out after electroless Pd plating. The first annealing step was performed in nitrogen atmosphere to form the appropriate amount of Pd silicide at 200°C for 30 min. After unreacted Pd clusters were removed by chemical etching, the second annealing step was carried out in a conventional furnace at 550°C for 18 h to crystallize a-Si. Then, a post-RTA treatment was used to improve the crystallinity and uniformity of Si films at 850°C for 75 s.

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