A Study of Parasitic Resistance Effects in Thin-Channel Polycrystalline Silicon TFTs With Tungsten-Clad Source/Drain

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***Abstract*—With selectively-deposited tungsten film grown on source/drain regions, the parasitic source/drain resistance of thin-channel polycrystalline silicon (poly-Si) thin film transistors can be greatly reduced, leading to the improvement of device driving ability. After extracting the parasitic resistance from characteristics of devices with different channel length, the influences of parasitic resistance on device performances were discussed. A physically-based equation containing the parasitic resistance effects was derived to explain the behavior of linear transconductance under high gate voltage. Good agreements were found between calculated and measured data for both the thin-channel devices with or without tungsten-clad source/drain structure.**

***Index Terms*—Parasitic resistance, poly-Si TFT, S/D resistance, selective tungsten, thin channel.**

I. Introduction

It has been reported that improved device performance such as high driving ability and small leakage current can be obtained by reducing the channel thickness of poly-Si TFTs [1]. However, shrinking the thickness of channel layer also enlarge the parasitic source/drain resistance, leading to a degraded driving ability. Similar problems occurred in thin-film silicon-on-insulators (SOIs) have been solved by using self-aligned silicide (SALICIDE) or selective tungsten chemical vapor deposition (SWCVD) technologies to reduce S/D resistance [2], [3]. For thin-channel poly-Si TFTs, however, most studies focus on fabricating various raised-S/D structures [4], [5]. The capability of using SALICIDE or SWCVD process on thin-channel poly-Si TFTs has never been verified. Moreover, when most papers address the improvement of device driving ability [4], [5], the parasitic resistance effects still lack for discussion. In this letter, thin-channel poly-Si TFTs with tungsten-clad S/D (W-TFTs) are demonstrated using SWCVD process, which has smaller silicon consumption than SALICIDE technologies [3], [6]. The parasitic resistance influences are studied by extracting parasitic resistance from device characteristics. The degradation of linear transconductance caused by parasitic resistance is also explained by a physical derivation.

II. Experimental

Proposed W-TFTs are prepared by the following process steps with a structure shown in the inset of Fig. 1. First, a 30 nm amorphous silicon layer was deposited by low-pressure chemical vapor deposition (LPCVD) at 550 °C on oxidized silicon wafers. After active region patterning, a 60 nm tetraethoxysilane (TEOS) oxide layer and subsequently a 300 nm a-Si layer were deposited by LPCVD. The a-Si layer was then recrystallized by solid phase crystallization (SPC) at 600 °C for 24 h. After defining gate electrode, n^- lightly-doped drain (LDD) implant was performed using phosphorus ions at a dose of 3×10^{13} cm^{-2}. A 200 nm oxide sidewall spacer abutting the gate was formed by conformal deposition of a TEOS oxide layer and subsequent reactive ion etching. Phosphorus ions at a dose of 5×10^{15} cm^{-2} were implanted to form the n^+ S/D region, then activated by rapid thermal annealing (RTA) at 750 °C for 20 sec. After removing the remaining oxide on source/drain regions by diluted HF, wafers were loaded into SWCVD system (ULVAC ERA-1000) to selectively deposit W film on exposed gate, source and drain regions with WF_6/SiH_4 gas flow rate as $20/6$ and process temperature of 300 °C. Conventional devices without W film deposition were also fabricated on the same wafer to serve as controls. A 500 nm Al film is deposited and defined to be metal pads. To reduce trap density and improve interface quality, wafers were also immured in an NH_3 plasma generated by plasma enhanced CVD (PECVD) at 300 °C for 1 h [7]. The cross sectional SEM image of the proposed W-TFTs is shown in Fig. 1. It is observed that the thickness of the W film is about 120 nm and the silicon consumption in S/D region is less than 20 nm (not fully-consumed), ensuring good contact resistance in ultrathin channel devices [6].

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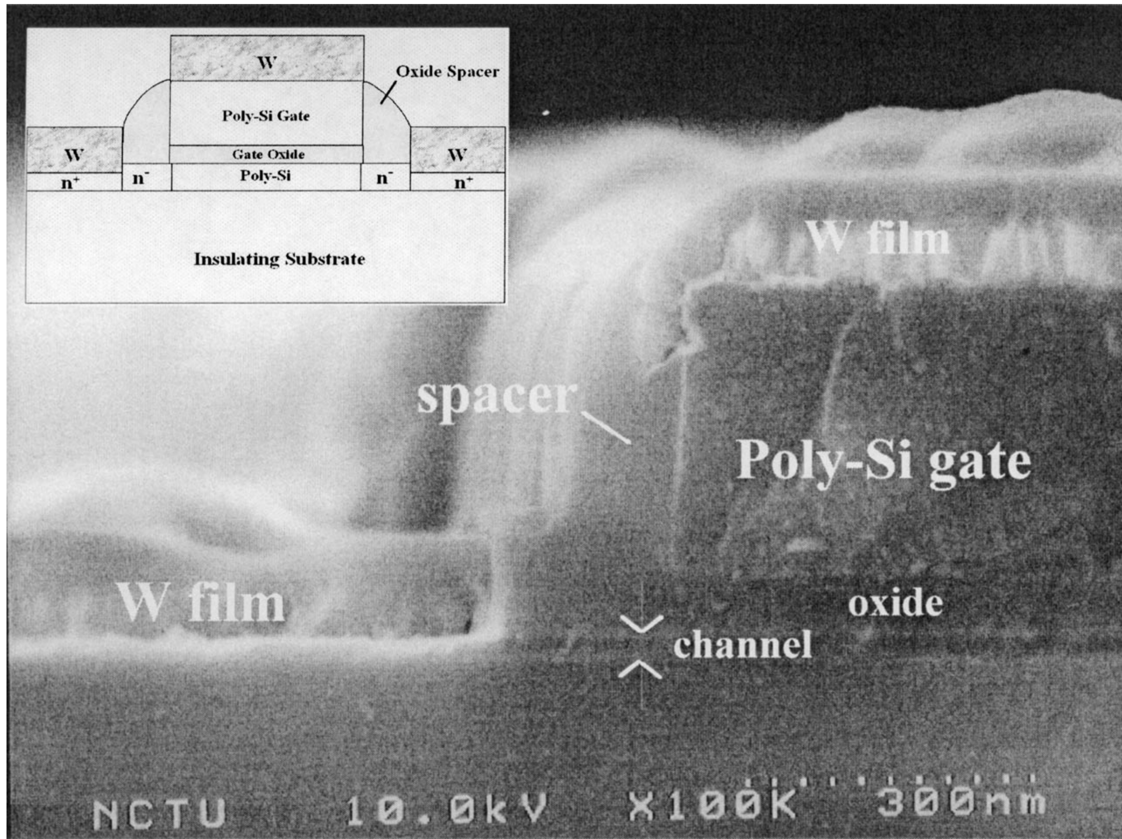

Fig. 1. Schematic cross sectional view (in the inset) and the SEM image of the proposed W-TFTs.

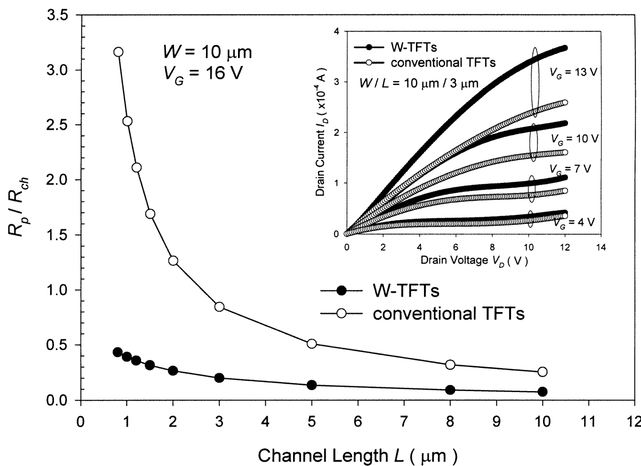

Fig. 2. Parasitic resistance over channel resistance as a function of channel length. Black circles represent data from W-TFTs, while white circles stand for data from conventional TFTs. A comparison of output characteristics for thin-channel W-TFTs and conventional TFTs is shown in the inset with nominal channel width and length of 10 μm and 3 μm.

III. Results and Discussions

The comparison of typical output characteristics of thin-channel W-TFTs and conventional ones are shown in the inset of Fig. 2. Obviously W-TFTs exhibit larger ON current than conventional ones. According to [8], the parasitic resistance R_p of devices can be extracted by plotting the channel width normalized ON resistance $R_{on}W$ against the channel length L. With different gate bias, the relationship between $R_{on}W$ and L can be expressed by several straight lines that extend to merge at a characteristics length l_0 representing the accumulation channel in LDD (and S/D) area and have a residual value of a gate-voltage independent parasitic resistance R_pW [8]. The ON resistance is therefore expressed as

$$R_{on} = \frac{\partial V_D}{\partial I_D} = R_p + R_{ch} = R_p + \frac{L - l_0}{W C_{ox} \mu_n (V_G - V_{TH})} \quad (1)$$

where R_{ch} represents the channel resistance, C_{ox} is the gate oxide capacitance per unit area, μ_n is the intrinsic carrier mobility without the parasitic resistance effects, V_{TH} is the device threshold voltage, and $L - l_0$ is defined as the effective channel length. Compared to the extracted R_p (13.2 kΩ) of conventional thin-channel devices, W-TFTs are found to exhibit smaller R_p (3.5 kΩ). Though R_p consists of S/D resistance and the parasitic resistance in LDD regions in our experiment, the latter one is the same by using identical LDD formation process. Accordingly, the improvement of R_p in W-TFTs is mostly contributed by reducing the S/D resistance. The influence of R_p is further revealed by plotting (R_p/R_{ch}) against channel length in Fig. 2(b). When channel length scaled down, (R_p/R_{ch}) keeps rising because of the reduced channel resistance. However, for conventional TFTs, the (R_p/R_{ch}) increases much more drastically than that of W-TFTs. Moreover, the R_p of conventional devices starts to dominate device performance when channel length is less than 2 μm.

When plotting the reciprocal of the slope, $[\Delta(R_{on}W)/\Delta L]^{-1}$ versus gate voltage V_G as given in Fig. 3, linear relationships are found for both W-TFTs and conventional ones [8]. The slope of the curves, representing

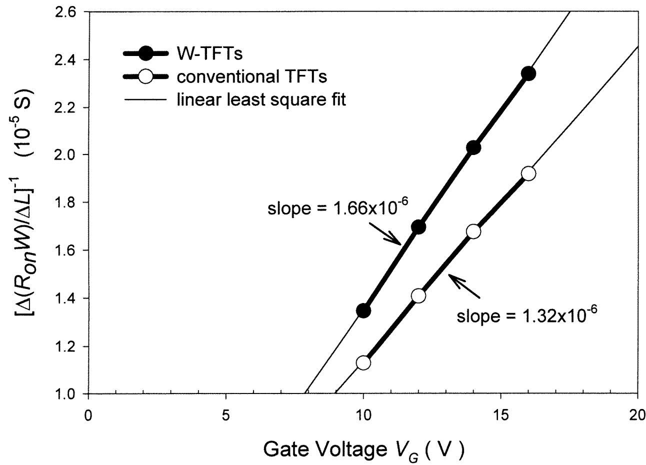

Fig. 3. Channel sheet conductance as a function of gate voltage. The solid line represents the linear least square fit of data while its slope contains the carrier mobility independent of channel length and parasitic resistance effects.

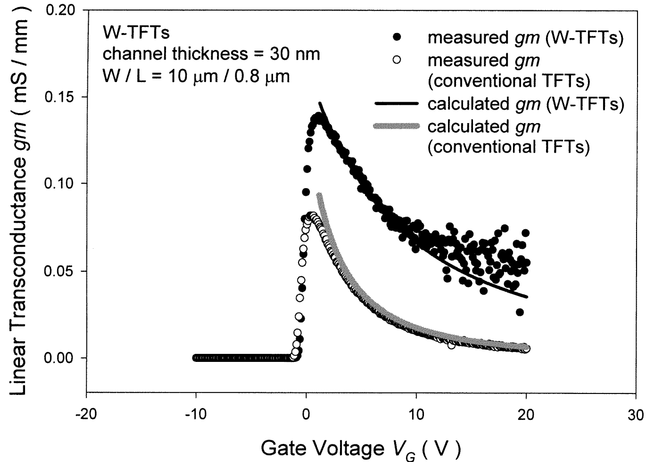

Fig. 4. Comparison between calculated and measured linear region transconductances. The nominal channel width and length are 10 μm and 0.8 μm, respectively.

the intrinsic carrier mobility, has no dependence on the gate voltage. This implies that the grain boundary barrier height, which dominates carrier transport in poly-Si film, have negligible variation with the gate voltage in linear region [9]. As a result, the intrinsic mobility μ_n of W-TFTs is 14.4 cm^2/Vs while that of conventional TFTs is 11.5 cm^2/Vs. The linear region transconductance can be derived by

$$I_D = V_D (R_p + R_{ch})^{-1} \quad (2)$$

$$gm \equiv \frac{\partial I_D}{\partial V_G} = AV_D \left(\frac{R_{ch}}{R_p + R_{ch}}\right) 2 = AV_D \left[AR_p (V_G - V_{TH}) + 1\right]^{-2} \quad (3)$$

where $A \equiv W\mu_n C_{ox}/L - l_0$. With R_p and l_0 obtained previously, gm calculated by eqn (3) is compared with measured data in Fig. 4. A good agreement is found, verifying the fact that the linear region gm is dominated by parasitic resistance effect especially in short channel devices. Larger R_p value gives rise to smaller gm maximum value and severer gm degradation under high gate voltages.

IV. Conclusion

Thin-channel poly-Si TFTs with reduced parasitic resistance are fabricated by capping tungsten film on S/D regions. The parasitic resistance can be reduced to 3.8 times smaller than that of control samples. W-TFTs therefore exhibit less pronounced parasitic resistance effects. By extracting the intrinsic carrier mobility, the gate voltage is found to have no influence on carrier transport in linear region. The degradation of linear region transconductance can be explained well by including the parasitic resistance effect into device current–voltage characteristics.

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