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Thickness Dependence of Microstructure of Laterally Crystallized Poly-Si Thin Films and Electrical Characteristics of Low-Temperature Poly-Si TFTs

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The effects of thickness of a-Si thin films on the resulting microstructure of metal-induced laterally crystallized (MILC) poly-Si and electrical characteristics of MILC low temperature poly-Si (LTPS) thin film transistors (TFTs) were investigated. The TEM images revealed a double-layer structure in the 1000-Å MILC poly-Si thin film. However, for the 400-Å MILC poly-Si thin film, there were single-layer grains within the thin film layer. The reason has been ascribed to the geometry restriction in the crystallization procedure. The average mobility of fabricated MILC LTPS TFTs with active layer thickness of 400 Å showed a little higher than that with 1000 Å active layer. Moreover, the MILC LTPS TFTs with active layer thickness of 400 Å exhibited better electrical uniformity than those with 1000 Å active layer either in threshold voltage or field-effect mobility. The reason should also be attributed to the different crystalline structures within the two thin-film layers.
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Low-temperature poly-Si (LTPS) thin-film transistors (TFTs) have received much attention in recent years because of their increasing use in active matrix displays, such as active matrix liquid crystal displays (AMLCDs)[1-5] and active matrix organic light-emitting displays (AMOLEDs),[6-10] and potential for three-dimensional integrated circuit (IC) applications.[11] The ability of fabricating high-performance LTPS TFTs enables their use in a wide range of applications. Therefore, there is great interest in improving the performance of LTPS TFTs. Solid-phase crystallization (SPC) has been a popular crystallization method for producing large-grain poly-Si thin films at low process temperature. However, a major drawback of conventional SPC is the long crystallization times at a temperature of about 600°C, which is not suitable for large-area glass substrate applications. Besides, conventional SPC also suffers from large defect density in the grains, which makes it hard to produce high-performance TFTs. Although excimer laser crystallization (ELC), a promising technique for mass production of LTPS TFTs on large-area glass substrates, can produce large-grain poly-Si with low intragrain defect density at low temperature, it suffers from high initial facility cost, high process complexity, and a narrow process window. Recently, Pd or Ni was found to induce crystallization of a-Si outside its coverage area.[12-14] This phenomenon of metal-induced "lateral" crystallization, or MILC for short, produces poly-Si thin films largely free of metal contamination, with better crystallinity than those produced by SPC. Among various metals, Ni has been shown to be the best candidate of inducing lateral crystallization at low temperature for fabricating good-performance poly-Si TFTs.

Although the MILC process and the electrical characteristics of MILC LTPS TFTs have been widely studied, there are still unsolved questions requiring identification. In this work, the effect of thin-film thickness on the results of MILC poly-Si thin films and the electrical characteristics of MILC LTPS TFTs is discussed. The detail mechanism of MILC with different thin-film thicknesses is also analyzed.

Experimental

A schematic graph shown in Fig. 1 illustrates the fabrication process of MILC LTPS TFTs. Various thicknesses of a-Si thin films were first deposited on oxidized silicon wafers by decomposition of pure silane (SiH_4) with low-pressure chemical vapor deposition (LPCVD) at 550°C. 2000 Å thick screen oxides were then deposited by plasma-enhanced chemical vapor deposition (PECVD). Ni seeding windows were patterned next to the device active channel region and etched to expose the seeding windows for Ni deposition. A 100 Å Ni layer was then deposited by thermal evaporation and lateral crystallization was carried out subsequently at 500°C for several hours in N_2 ambient. The remaining Ni and capping oxide were removed completely after crystallization. After defining the device active layer, 1000 Å tetraethyl orthosilicate (TEOS) gate oxides were deposited by PECVD at 385°C. 3000 Å TaN films were then deposited by sputtering for gate electrode. The TaN films and gate oxides were etched by reactive ion etching (RIE) to form gate electrodes. Next, a self-aligned phosphorous implantation with a dose of $5 \times 10^{15}\ cm^{-2}$ was carried out to form the source and drain regions. 3000 Å thick passivation TEOS oxides were then deposited by PECVD, following by 12 h thermal annealing at 550°C for activation of implanted dopants. Finally, contact hole formation and metallization were carried out to complete the process. A 20 min sintering process was carried out at 400°C to reduce the contact series resistance of the source/drain electrodes.

Results and Discussion

Figure 2 shows the dependence of crystallization rate on the thickness of a-Si thin film. The crystallization was carried out at 500°C, and the crystallization rate was measured after 20 h thermal annealing. The MILC rate decreases gradually with decreasing thickness from 1000 to 400 Å. Below 400 Å, a drastic reduction of crystallization rate is observed. The MILC process is mediated by the migration of the $NiSi_2$ precipitates.[15] For thick a-Si film, all $NiSi_2$ precipitates can act as nucleation sites and participate in the lateral crystallization process although ⟨110⟩-oriented precipitates may dominate the substantial growth of Si. Because more $NiSi_2$ precipitates can participate in the lateral crystallization process, the thick a-Si films reasonably exhibit a fast crystallization rate. When the thickness of a-Si film decreases, the migration of $NiSi_2$ precipitates is restricted by the top and bottom surface of the a-Si thin film. The nucleus that inclines from the ⟨110⟩ direction can hardly lead to the growth of crystallites because of the intersection of the {111} plane normals with the top or bottom surface. Due to the reduction of $NiSi_2$ precipitates that can induce lateral crystallization, the lateral crystallization rate decreases with decreasing thickness. For a-Si thin film $<$400 Å, in addition to the restriction of $NiSi_2$ precipitate migration by the top and bottom surface of a-Si thin film, the formation of new $NiSi_2$ precipitates during the lateral crystallization

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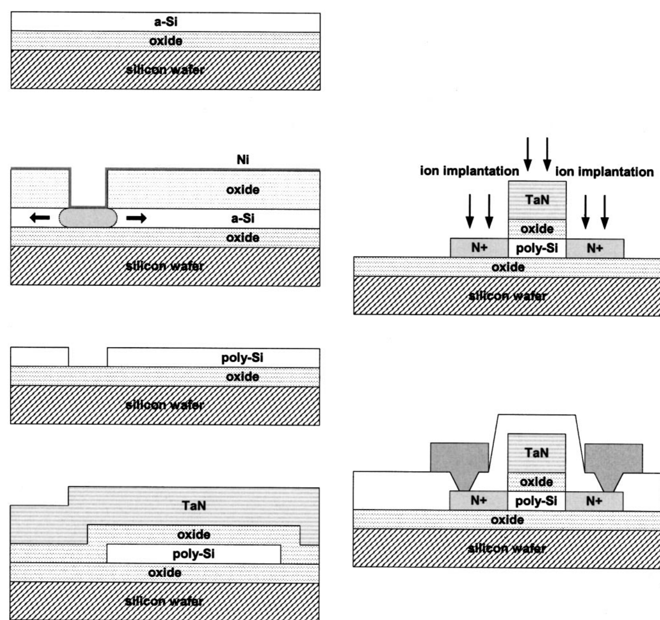

Figure 1. The fabrication process of Ni-MILC LTPS TFTs.

process becomes difficult, because the size of $NiSi_2$ precipitate is generally about several tens of nanometers.[16] As a result, a drastic reduction of crystallization rate is observed for a-Si thin film <400 Å. To obtain an acceptable lateral crystallization rate, thin film thickness above 400 Å is suitable for device fabrication.

Figures 3 and 4 show cross-sectional transmission electron microscopy (TEM) images of 1000 and 400 Å MILC poly-Si thin films, respectively. The images reveal two different crystalline structures within the thin film. From the image contrast, a double-layer structure is found in the 1000 Å MILC poly-Si thin film. That is, within the thin film layer, there are two grains of different orientations. However, for the 400 Å MILC poly-Si thin film, there is single layer grains within the thin-film layer. The magnified image shown in Fig. 4 also indicates a perfect crystalline structure having a single orientation within the 400 Å MILC poly-Si thin film.

For 1000 Å a-Si thin film, two $NiSi_2$ precipitates with different orientations may have the chance to induce growth of Si simulta-

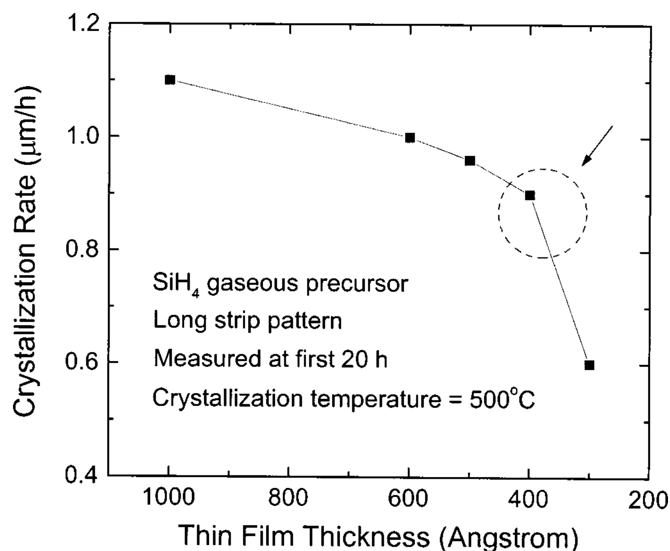

Figure 2. The dependence of lateral crystallization rate on the thickness on a-Si thin film.

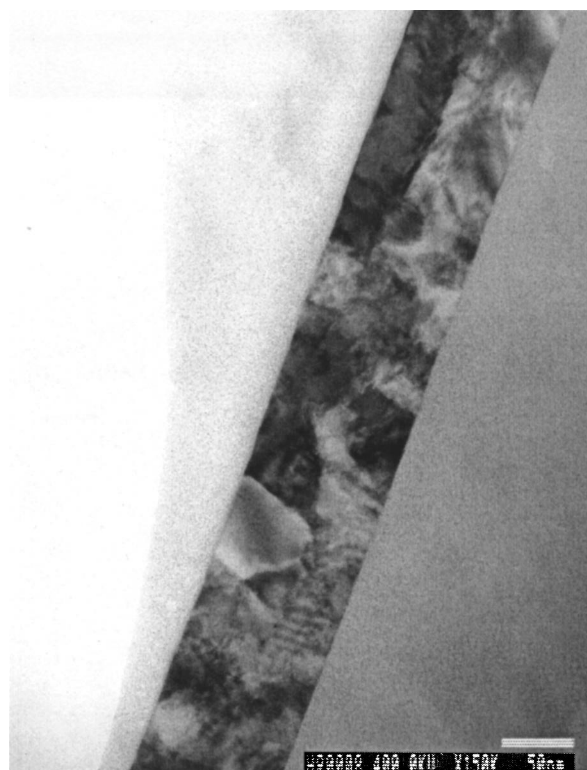

Figure 3. Cross-sectional TEM image of a 1000 Å Ni-MILC poly-Si thin film.

Figure 4. Cross-sectional TEM image of a 400 Å Ni-MILC poly-Si thin film.

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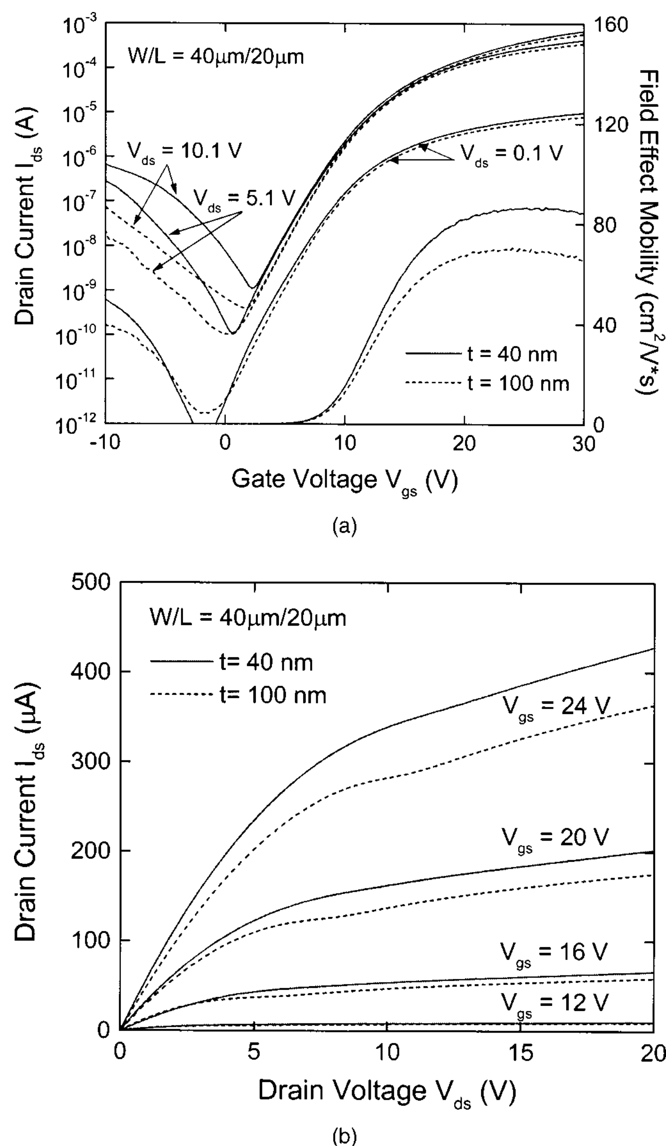

Figure 5. I-V curves of Ni-MILC LTPS TFTs (a) transfer characteristics and (b) output characteristics.

neously within the thin-film layer. This is because the thickness of the thin film is about twice as large as the $NiSi_2$ precipitate. In this case, grains with different orientations can exist simultaneously within a thin-film layer. However, when the thickness of a-Si thin film decreases to 400 Å, migration of $NiSi_2$ precipitates is restricted by the top and bottom surface of a-Si thin film, and only ⟨110⟩-oriented precipitates can lead to the growth of crystallites because the thickness of the thin film is approximately equal to the size of the $NiSi_2$ precipitate. As a result, only one crystalline orientation is found within the 400 Å thin-film layer.

Typical transfer characteristics curves and output characteristics curves of fabricated MILC LTPS TFTs with an active layer thickness of 1000 and 400 Å are shown in Fig. 5a and b, respectively. Table I lists some important typical device electrical characteristics. In this case, the field-effect mobility and subthreshold swing were measured at $V_{ds} = 0.1$ V, and the threshold voltage was defined as the gate voltage required to achieve a normalized drain current of $I_{ds} = (W/L) \times 10^{-8}$ A at $V_{ds} = 0.1$ V. The typical mobilities of MILC LTPS TFTs with active layer thickness of 1000 and 400 Å are 70 and 86 cm^2/V s although there are some variations in these devices. The average mobility of Ni-MILC LTPS TFTs with an active

Table I. Measured electrical characteristics of Ni-MILC LTPS TFTs.

Ni-MILC LTPS TFT	Mobility (cm^2/V s)	Threshold voltage (V)	Subthreshold swing (V/decade)	On/off current ratio at $V_{ds} = 5.1$ V
400 Å active layer	86	7.5	2.24	4.11×10^6
1000 Å active layer	70	7.7	2.21	3.41×10^6

layer thickness of 400 Å is a little higher than that with a 1000 Å active layer. The reason may be attributed to the different crystalline structures within the thin-film layer, which has been discussed above.

Figure 6a and b shows the statistical distribution of the threshold voltage (V_T) and field-effect mobility (μ_{FE}) of MILC LTPS TFTs for different thicknesses of active layer. Twenty TFTs were measured in each case. It is clear that the MILC LTPS TFTs with an active layer thickness of 400 Å exhibit better electrical uniformity

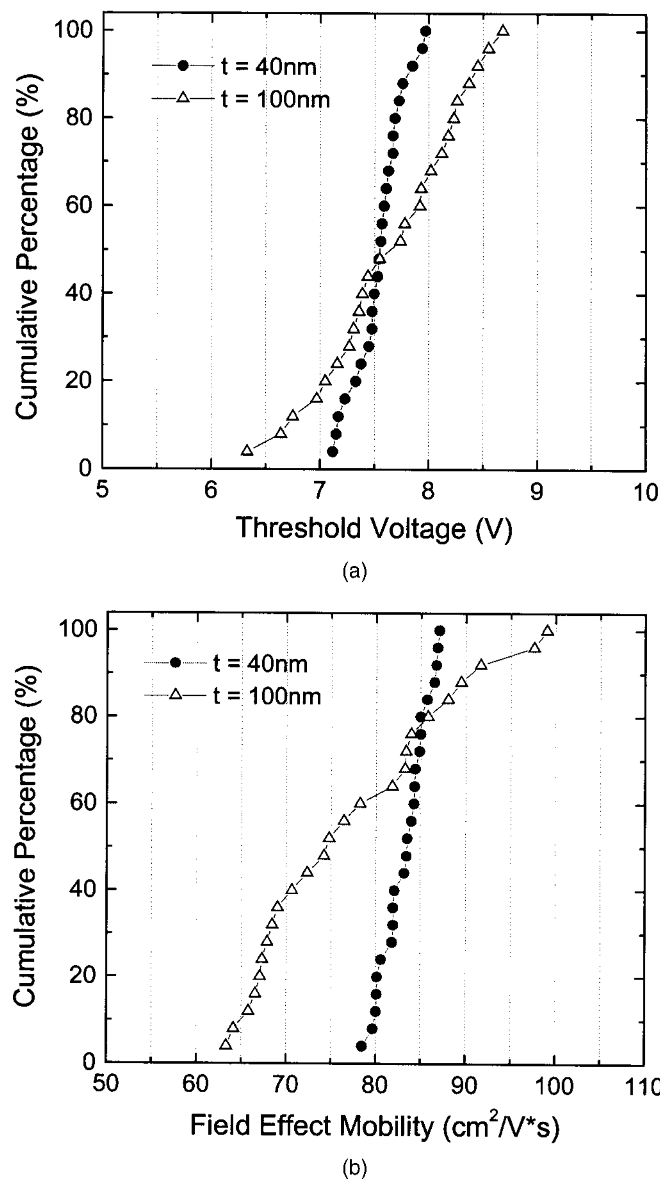

Figure 6. Statistical distribution of (a) threshold voltage and (b) field-effect mobility for Ni-MILC LTPS TFTs.

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compared to those with a 1000 Å active layer either in threshold voltage or field-effect mobility. The reason should also be attributed to the different crystalline structures within the two thin-film layers. The electrical characteristics of poly-Si TFT are profoundly affected by the properties of poly-Si thin film, including crystallinity, grain size, grain structure, grain orientation, and type of grain boundary. Because the properties of MILC poly-Si are more uniform in the 400 Å thin film, the electrical characteristics of MILC LTPS TFTs with an active layer thickness of 400 Å deservedly show little variation. Clearly, a tighter parameter distribution is advantageous, allowing more predictable device performance and easier circuit design. As a result, a thinner active layer is more suitable for device applications.

Conclusions

The thickness of a-Si thin film has a profound influence on the resulting microstructure of MILC poly-Si thin film and the electrical characteristics of fabricated MILC LTPS TFTs. The MILC rate decreased gradually with decreasing thickness from 1000 to 400 Å and a drastic reduction of crystallization rate was found as thin-film thickness was reduced below 400 Å due to the restriction of $NiSi_2$ precipitate migration by the top and bottom surface of a-Si thin film. The 400 Å MILC poly-Si thin film shows better crystalline uniformity within the thin-film layer compared to the thicker one (1000 Å), and MILC LTPS TFTs fabricated using 400 Å MILC poly-Si thin film exhibited better performance and uniformity.

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