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Discrete-Dopant-Fluctuated Transient Behavior and Variability Suppression in 16-nm-Gate Complementary Metal–Oxide–Semiconductor Field-Effect Transistors

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Variability in the characteristics of nanoscale complementary metal–oxide–semiconductor (CMOS) field-effect transistors is a major challenge to scaling and integration. However, little attention has been focused on the existence of transient behavior fluctuations of devices owing to random dopant placement. In this study, we explore the discrete-dopant-induced transient behavior fluctuations of 16-nm-gate CMOS circuits through a three-dimensional large-scale statistically sound "atomistic" device-circuit-coupled simulation approach, concurrently capturing "dopant concentration variation" and "dopant position fluctuation". For a 16-nm-gate CMOS inverter, a 3.5% variation of the rise time, a 2.4% variation of the fall time, an 18.3% variation of the high-to-low delay time, and a 13.2% variation of the low-to-high delay time are estimated and discussed. Fluctuation suppression techniques proposed from the device and the circuit viewpoints are implemented to examine the associated intrinsic fluctuations. © 2009 The Japan Society of Applied Physics

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1. Introduction

The gate lengths of scaled metal–oxide–semiconductor field-effect transistors (MOSFETs) are now below 30 nm in 45-nm-node high-performance circuit design.[1] Devices with gate lengths of less 10 nm are currently being explored.[2–5] Local device variation and the uncertainty of signal propagation time have become crucial for the variation of system timing and the determination of clock speed.[4,5] Yield analysis and optimization, which take into account the manufacturing tolerances, model uncertainties, variations in the process parameters, and so forth, are known as indispensable components of circuit design.[6–10] With device scaling, various random effects resulting from the nature of the manufacturing process, such as ion implantation, diffusion, and thermal annealing,[11] have induced significant fluctuation of electrical characteristics in nanoscale MOSFETs. The number of dopants is now of the order of tens in the depletion region of a nanoscale MOSFET, and the effect of this factor on device characteristics is large enough to be distinct.[12] The fluctuation of characteristic is caused not only by variation in average doping density, which is associated with a fluctuation in the number of impurities, but also by the particular random distribution of impurities in the channel region. Diverse approaches have recently been proposed to study fluctuation-related issues in semiconductor devices[13–30] and circuit.[31–36] However, little attention has been focused on the existence of transient characteristic fluctuations in the active devices due to random dopant placement. Moreover, due to the randomness of dopant position in the devices, the fluctuation of device gate capacitance is nonlinear and difficult to model with the current compact models.[24)]

In this study, we propose a large-scale statistically sound device-circuit-coupled simulation approach to analyze the random dopant effect in nanoscale complementary MOS (CMOS) circuits, whereby the discrete-dopant-number- and discrete-dopant-position-induced fluctuations can be captured concurrently. Based on the statistically generated large-scale doping profiles, device simulation is performed by solving a set of three-dimensional (3D) drift-diffusion equations with density-gradient quantum corrections method,[37–40] which is conducted using a parallel computing system.[41–43] For the investigation of the transient characteristic fluctuations of a circuit, a device-circuit-coupled simulation[44–46] with various discrete dopant distributions is conducted. The accuracy of the developed analyzing technique has been quantitatively verified in the experimentally measured characteristics of 20 nm devices.[17–22] The development of fluctuation suppression techniques can be from the circuit and device viewpoints. From the circuit viewpoint, the use of devices with different threshold voltages (V_{th}) and changes in the circuit topology are useful for the design of the sensing circuit and static random-access memory. From the device viewpoint, we may change the device architecture,[17,21,29] or use the high-k dielectrics and thin gate oxide,[18,36] and channel engineering[16,22,25–27] to suppress the discrete-dopant-induced fluctuations. However, the techniques for suppression of transient characteristics fluctuation are still not well-developed. Therefore, three fluctuation suppression techniques from the circuit viewpoint (an inverter with shunt n-MOSFETs) and the device viewpoint (vertical doping profile engineering and lateral asymmetry doping profile) are proposed and examined. The relationship between the suppression of DC and transient characteristics fluctuations is investigated. Each suppression technique exhibits advantages and disadvantages in DC and transient characteristics. The proposed simulation approach can estimate the fluctuation in circuit characteristics and accelerate the development of next-generation nanoelectronic circuits and systems.

The paper is organized as follows. In §2, we describe the analyzing technique for studying the random dopant effect in nanoscale devices and circuits. In §3, we examine the discrete-dopant-induced characteristic fluctuations of the 16-nm-gate device and inverter circuit. Three fluctuation suppression techniques are implemented and investigated. Finally, we draw conclusions and suggest future work.

2. The Simulation Technique

The nominal channel doping concentration of the explored devices is 1.48×10^{18} cm^{-3}. They have a 16 nm gate, a gate oxide thickness of 1.2 nm, and a work function of 4.4 eV. Outside the channel, the doping concentrations in the source/drain and background are 1.1×10^{20} and 1×10^{15} cm^{-3}, respectively. For the channel region, to consider the

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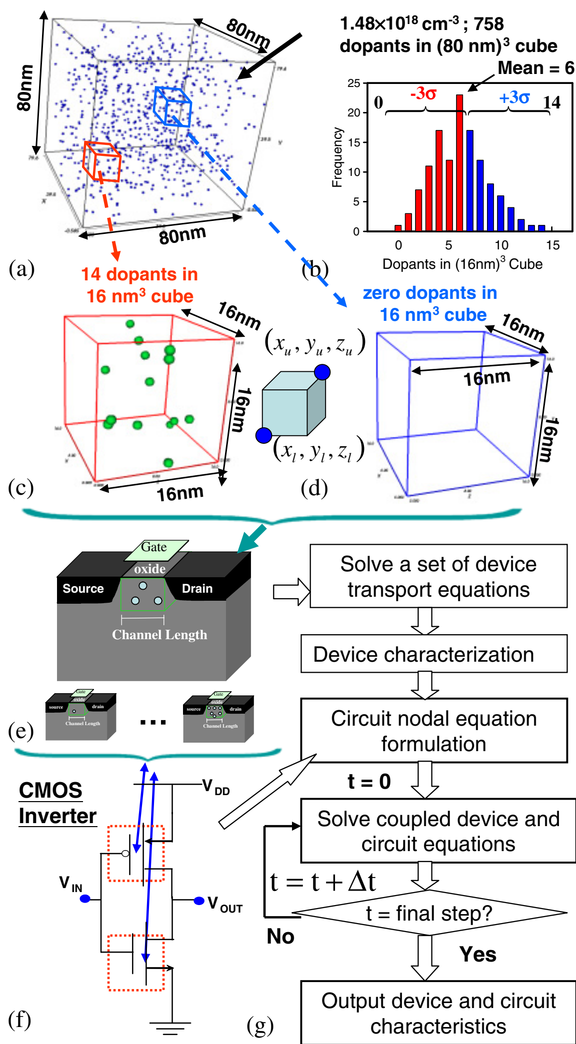

Fig. 1. (Color online) (a) Discrete dopants randomly distributed in the cube of side 80 nm at an average concentration of 1.48 x 10^{18} cm^{-3}. (b)–(d) There are 758 dopants within the cube, but the number of dopants in subcubes of side 16 nm varies from 0 to 14 (with an average of 6). The 125 subcubes are equivalently mapped into the channel region for dopant-position/number-sensitive device simulation and device-circuit coupled simulation as shown in (c)–(e), where the inverter is used as a test circuit for timing variation estimation.

effect of random fluctuation of the number and location of discrete channel dopants, 758 dopants are first randomly generated in a cube of side 80 nm, in which the equivalent doping concentration is $1.48 \times 10^{18}\,\mathrm{cm}^{-3}$, as shown in Fig. 1(a). The generation of dopant distribution is totally random, and performed by computer program. The dopant generation approach is mainly based on the fundamental principles of statistics. This totally random of dopants generated in three dimensions, can ensure that the nominal doping concentration is $1.48 \times 10^{18}\,\mathrm{cm}^{-3}$ [= 758 dopants/$(80\,\mathrm{nm})^3$]. The $(80\,\mathrm{nm})^3$ cube is then partitioned into 125 subcubes of side 16 nm. The number of dopants in each subcube varies from zero to 14, with an average of 6, as shown in Figs. 1(b)–1(d). Since the average dopant number is 6, the 3σ of the dopant number in this study is about 7.3. Thus, the number of dopants in a subcube can vary from 0 to 14, which corresponds to the generated results shown in Fig. 1(b) indicating that the simulation approach is statistical-sound. Each of the 125 generated subcubes is then equivalently mapped into the channel region of the device channel for the 3D device simulations with discrete dopants, as shown in Fig. 1(e). The device simulation is performed by solving a set of 3D density-gradient equations coupled with Poisson equations as well as electron–hole current continuity equations[37–40] on a parallel computing system.[17–21,40–43] A step function, as shown below, is used to define the concentration and positions of channel dopants, N_A, in solving the device transport equations.

$$H(x,y,z) = \begin{cases} 1, & x \geq 0, y \geq 0, z \geq 0 \\ 0, & \text{otherwise} \end{cases} \tag{1}$$

$$N_A = \sum_{i=0}^{k} N_A^{\text{dopant}} \cdot [H(x - x_l, y - y_l, z - z_l) - H(x - x_u, y - y_u, z - z_u)], \tag{2}$$

where (x_l, y_l, z_l) and (x_u, y_u, z_u) are the lower and upper coordinates of a discrete dopant, as shown in Fig. 1(d). k is the number of dopants in the device channel, and N_A^{dopant} is the associated doping concentration for a dopant within a box, whose concentration is $1/[(x_u - x_l)(y_u - y_l)(z_u - z_l)]$. Then, N_A is substituted into the source of the Poisson equation and solved with the electron–hole current continuity equations and density-gradient quantum correction equations simultaneously for discrete-dopant-fluctuated device characteristics. Note that the generation of dopant distribution can ensure the mean doping concentration is $1.48 \times 10^{18}\,\mathrm{cm}^{-3}$ [= 758 dopants/$(80\,\mathrm{nm})^3$]. Although the variance may not be always the same, it still adheres to the statistical principles. Channel dopants will definitely appear outside the defined subcube of side 16 nm in particle manufacturing processes. However, since the operation of MOSFETs is achieved through surface conduction, the influence of such channel dopants is not significant in random dopant fluctuation. Thus, in this study, we only define the channel doping profile in the $(16\,\mathrm{nm})^3$ cube, as shown in Fig. 1(c). Therefore the channel dopants only appear in the subcube of side 16 nm and there are no dopants located outside the cubic channel region. According to this analyzing scenario, only channel dopants are treated discretely. The doping profile remains continuous in the source/drain region because the volume of source/drain dopants is significantly larger than that of the channel region. However, as a consequence, the present simulations only provide qualitative results. Nevertheless, this approach allows us to focus on the study of the characteristic fluctuations induced by the randomness in the number and position of dopants in the channel simultaneously. The accuracy of the simulation technique was confirmed by comparing simulated fluctuation results with measurements of experimentally fabricated 20 nm devices.[18] Figure 1(d) shows the CMOS inverter circuit used as the test circuit for exploring the transient characteristic fluctuations in nanoscale CMOS circuits. Similarly, we can generate 125 discrete-dopant-fluctuated cases for pMOS through the flow of Figs. 1(a)–1(c). Then, 125 pairs of nMOS and pMOS devices are randomly selected from a pool of discrete-dopant-fluctuated devices and are used for the examination of circuit characteristics fluctuations. For the sake of simplicity, the n- and p-MOSFETs are with the same device

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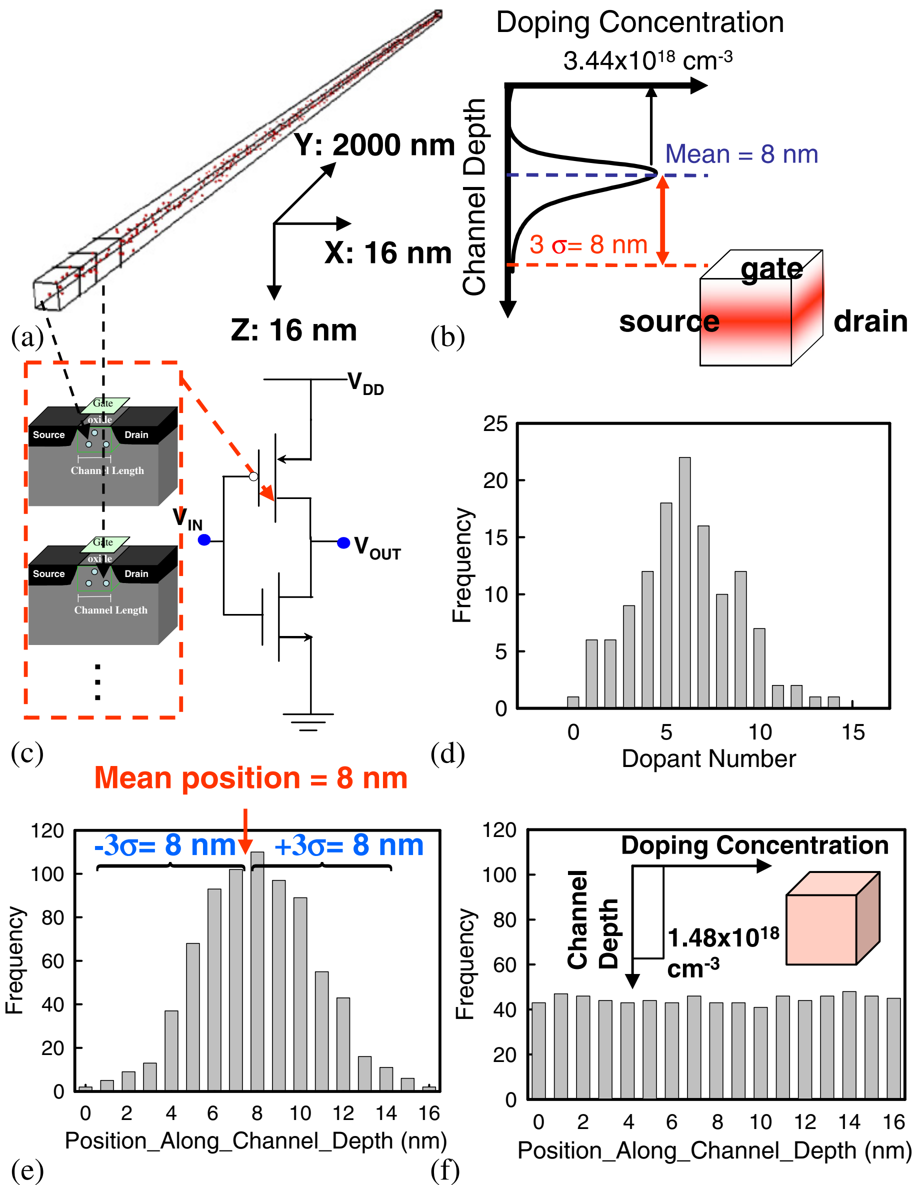

Fig. 2. (Color online) (a) There are 758 dopants are within a prolongated solid, in which the equivalent doping concentration is 1.48 x 10^{18} cm^{-3}. The dopant distribution in the direction of channel depth, represented by an arrow in Fig. 1(e), follows a normal distribution (b). The partitioned cubes are equivalently mapped into the channel region for dopant position/number-sensitive device simulation and device-circuit-coupled simulation, as shown in (c). Similarly, the number of dopants within the subcube of side 16 nm varies from 0 to 14 (with an average of 6) (d). The vertical dopant distributions of the improved and original doping profile are shown in (e) and (f), respectively.

dimension (the gate length and the device width are both 16 nm). Since there is no well-established compact model for such ultrasmall nanoscale devices, and for capturing the discrete-dopant-position-induced fluctuations, a device-circuit-coupled simulation approach[17–21,45,46] is developed, as shown in Fig. 1(e). The characteristics of devices of test circuit are first estimated by solving the device transport equations and using as initial guesses in the device-circuit-coupled simulation. The simulated device result is then transferred to a circuit simulation through circuit nodal equations. The circuit nodal equations of the test circuit are formulated and then directly coupled to the device transport equations (in the form of a large matrix containing the circuit and device equations), which are solved simultaneously to obtain the circuit characteristics. Note that the proposed simulation technique is statistically sound for characterizing the random dopant fluctuation.

To examine the effectiveness of the channel engineering technique in both nanoscale devices and circuits, various doping profile engineering approaches have been proposed. The generation of the dopant distribution can be further extended to the study of lateral and vertical doping profiles. Without loss of generality, we show the generation of a vertical doping profile as an example as below. To effectively compare the results of fluctuation suppression, the nominal threshold voltage is first calibrated to 140 mV, which is the same as that in the original cases. Then, 758 dopants are randomly generated in a large elongated solid (gate width, source–drain direction, channel depth: $16 \times 2000 \times 16\,\text{nm}^3$), in which a doping concentration equivalent to $1.48 \times 10^{18}\,\text{cm}^{-3}$ is set, as shown in Fig. 2(a). The profiles of the generated dopants in the z-direction are the normally distributed, as shown in Fig. 2(b). Both the mean position and the three sigma of this distribution are 8 nm,

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which can be controlled by the manufacturing processes of ion implementation and thermal annealing. The dopant distributions along the source–drain and gate width directions are totally random as described in Fig. 1. The inset of Fig. 2(b) shows the nominal case of vertical doping profile engineering, where the darker region indicates a higher doping concentration. The large rectangular solid is then partitioned into 125 subcubes of side 16 nm and mapped into the device channel for discrete-dopant and device-circuit-coupled simulation, as shown in Fig. 2(c). The number of dopants varies from 0 to 14 with an average of 6, as shown in Fig. 2(d). The longitudinal dopant distributions of the improved and the original doping profiles, which are generated from Fig. 1, are plotted in Figs. 2(e) and 2(f), respectively. The inset of Fig. 2(f) shows the distribution of doping concentration for the original doping profile. Since the position of discrete dopants generated in Fig. 1 is random in each direction, the distribution of dopant number in the direction of channel depth is uniform. The result shows that the numbers of dopants appearing near the channel surface for the improved doping profile is significantly less than that for the original doping profile, and thus may induce less surface potential fluctuation. Similarly, for the lateral asymmetry doping, a larger numbers of dopants are generated in a large rectangular solid (gate width, source–drain direction, channel depth: $40 \times 80 \times 80\,\mathrm{nm}^3$). The generation of dopant distribution is totally random. Then the large cube is partitioned into 125 ($8 \times 16 \times 16\,\mathrm{nm}^3$) subregions and mapped into the drain end of the channel region for discrete dopant simulation.

3. Results and Discussion

In this section, the transient characteristic fluctuations are investigated in terms of the rise time, fall time, and delay time. The correlation between transient and DC characteristic fluctuations is discussed. Then, three fluctuation suppression techniques from device and circuit viewpoints are investigated.

Figure 3(a) shows the input and output transient characteristics for the 16-nm-gate CMOS inverter circuit. The dotted line shows the input signal, the rise time, fall time, and hold time of which are 2.0, 2.0, and 30.0 ps, respectively, and the solid and dashed lines are the output signals. The magnified plots, Figs. 3(b) and 3(c), show the high-to-low and low-to-high transitions for the output signal, respectively, where the solid line shows the nominal case (the continuously doped channel with a doping concentration of $1.48 \times 10^{18}\,\mathrm{cm}^{-3}$) and the dashed lines are random-dopant-fluctuated cases. For the high-to-low transition, the nMOS device is on and starts to discharge load capacitance, causing the output signal to transit from logic "1" to logic "0". The fall time (t_f) is defined as the time required for the output voltage to change from 90% of the logic "1" level to 10% of the logic "1" level, and the high-to-low delay time (t_{HL}) is the time difference between the points of 50% input and 50% output signals, as shown in Fig. 3(b). Similarly, for the low-to-high transition characteristics, the pMOS device is turned on and starts to charge the load capacitance, causing the output voltage to transit from logic "0" to logic "1". The rise time (t_r) and low-to-high delay time (t_{LH}) are defined in Fig. 3(c). Figure 4(a) shows t_{HL} as a function of

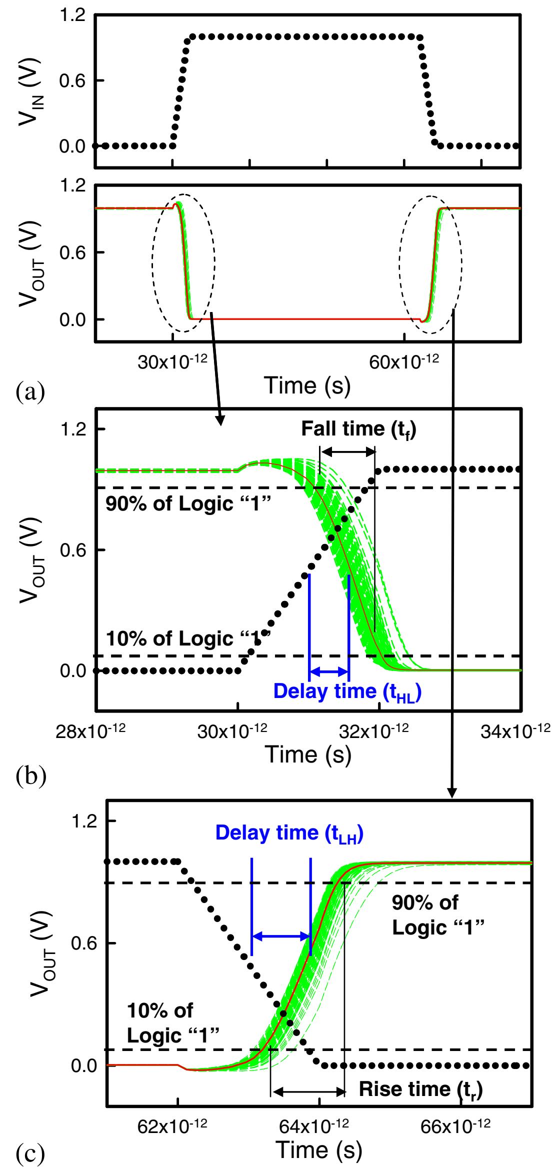

Fig. 3. (Color online) (a) The input and output signals for the discrete-dopant-fluctuated 16-nm-gate inverter circuit. The magnified plots show (b) the fall and (c) the rise transitions, where the rise time, fall time, high-to-low delay time, and low-to-high delay time are defined.

the channel dopant number in n-MOSFETs, in which each symbol indicates one discrete-dopant-fluctuated case. Since the equivalent channel doping concentration is $1.48 \times 10^{18}\,\mathrm{cm}^{-3}$, the number of dopants in a cubic channel region of side 16 nm may vary from 0 to 14 with an average of 6. The delay time is dependent on the start of the signal transition. For the high-to-low signal transition, the start of t_{HL} is determined by the V_{th} of the n-MOSFETs. Therefore, as the number of dopants in the nMOS channel is increased, the time at which the output signal transition starts is delayed resulting in an increase in t_{HL}. The increase of t_{HL} owing to the increasing channel dopants is the result of discrete-dopant-number-induced fluctuation. However, we found that even with the same dopant number inside the channel, the delay time can still vary significantly. Take the cases of six dopants inside the nMOS device as an example; the maximum t_{HL} difference is about 0.3 ps, where the nominal

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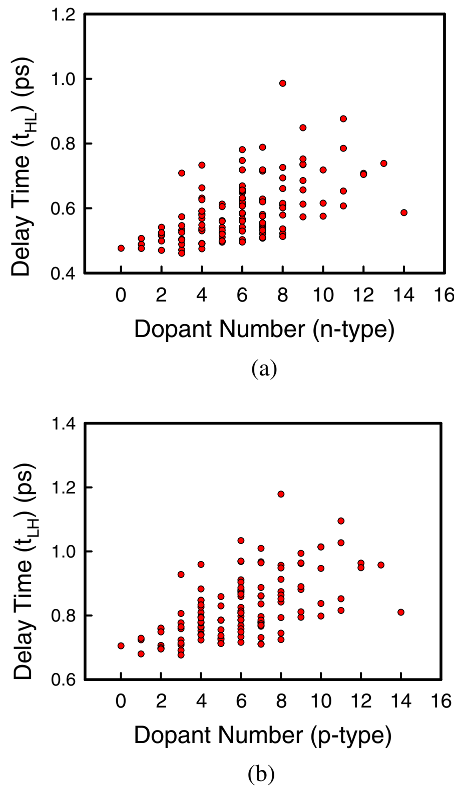

Fig. 4. (Color online) The fluctuations of (a) high-to-low and (b) low-to-high delay time as a function of the channel dopant number in the n- and p-MOSFETs for the discrete-dopan-fluctuated CMOS inverters.

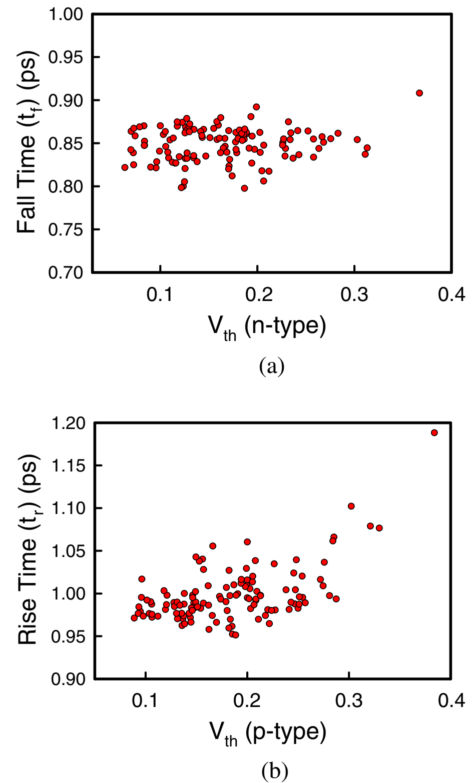

Fig. 5. (Color online) The fluctuations of (a) the high-to-low and (b) low-to-high delay time as a function of the threshold voltage in the n- and p-MOSFETs for the discrete-dopant-fluctuated CMOS inverters.

t_{HL} is 0.59 ps. We refer to this effect as discrete-dopant-position-induced fluctuation. Note that the magnitude of discrete-dopant-position-induced fluctuations increases as dopant number increases because of the increasing number of fluctuation sources (dopants). The mechanism is described in detail elsewhere.[11,18,21,30] Similarly, for t_{LH}, the time at which the signal transition starts is dependent on the operation of p-MOSFETs and therefore increases as the number of channel dopants in p-MOSFETs increases, as shown in Fig. 4(b). Figures 5(a) and 5(b) show the fall time and rise time as a function of the threshold voltage for n- and p-MOSFETs, respectively. The fall time is dependent on the discharge capability of the nMOS device, and the rise time is dependent on the charge capability of the pMOS device. As the threshold voltages of the n- and p-MOSFETs are increased, the discharge and charge ability for given values of t_f and t_r decrease. Therefore, the time required for the fall and rise transitions increases. The trend for t_f is not clear because in this study, only the transistors gate capacitance was used as the load capacitance. The small load capacitance and strong driving capability of n-MOSFETs make the trend of t_f fluctuation insignificant. Figure 6(a) summarizes the normalized timing fluctuations. For rise and fall time fluctuations, the driving capability of the device is relevant. Therefore, the fall time fluctuation is smaller than the rise time fluctuation owing to the stronger discharge capability of nMOS devices in the fall transition than the charge capability of pMOS devices in the rise transition. The delay time fluctuations are related to the threshold voltage fluctuation of the controlling device. Therefore, the t_{HL} fluctuation is larger than the t_{LH} fluctuation because of

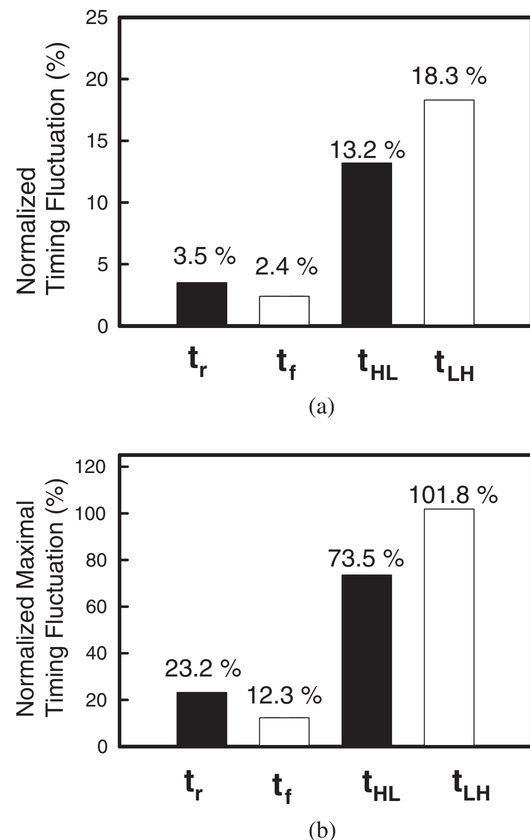

Fig. 6. A summary of (a) normalized and (b) normalized maximal timing fluctuations for the explored 16-nm-gate CMOS inverter.

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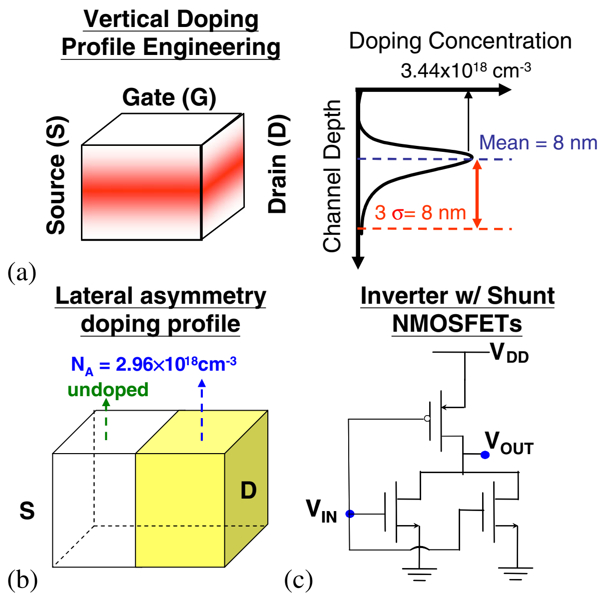

Fig. 7. (Color online) The proposed fluctuation suppression techniques according to the device viewpoint: (a) the vertical doping profile engineering and (b) the lateral asymmetry doping profile, and from the circuit viewpoint: (c) the inverter with shunt n-MOSFETs.

the larger V_{th} fluctuation of n-MOSFETs than that of p-MOSFETs. The delay time fluctuation is the dominating factor in the transient characteristics fluctuation. However, the maximal rise and fall time fluctuations are about 23.2 and 12.3%, respectively, which are large enough to induce timing variations in digital circuits. Moreover, the rise and fall time fluctuations can be added to the delay time characteristics and enhance the delay time fluctuation.

The delay time fluctuation is the dominating factor affecting timing characteristics, and t_{HL} fluctuation is larger than t_{LH} fluctuation; therefore, this study focuses on the suppression of the fluctuations that are induced by n-MOSFETs. To suppress the discrete-dopant-induced transient characteristic fluctuations, three fluctuation suppression techniques are proposed. From the device viewpoint, vertical doping profile engineering and the lateral asymmetry doping profile are selected, as shown in Figs. 7(a) and 7(b), respectively, because the fluctuations are caused by dopants themselves. Moreover, the doping profile engineering may be a cheaper way to suppress fluctuations, because there is no additional process required in the standard CMOS fabrication procedure. From the circuit viewpoint, an inverter with shunt n-MOSFETs is proposed, as shown in Fig. 7(c). The concept behind the shunt transistor approach is to increase the effective width of the transistor, which is the most fluctuation-sensitive element in circuits. For vertical doping profile engineering, the doping profile from the device surface to the substrate follows a normal distribution. The aim of vertical doping profile engineering is to locate fewer dopants near the current conducting path[16,25–27] to suppress the device characteristic fluctuations. For the lateral asymmetry doping profile, in contrast to conventional lateral asymmetry devices[47,48] with a higher channel doping concentration near the source end, the channel doping concentration is higher near the drain end. According to previous work,[49] dopants located at the source end and drain end of the channel region may degrade the injection velocity and saturation velocity, respectively. The low- and medium-field regions at the beginning of the channel act as a bottleneck for determination of the on-current, and therefore the dopants located at the source end channel may induce larger current fluctuation than those at the drain end. To compare the device characteristics on the same basis, the nominal threshold voltages for devices with vertical doping profile engineering and lateral asymmetry doping profile are calibrated to 140 mV, which is the same as that of the original devices. Figure 8 summarizes the improvement of the DC and gate capacitance (C_g) fluctuations for the two doping profile engineering approaches with respect to the original doping profile. Both of these approaches exhibit significant improvement in the V_{th} and C_g fluctuations. The lateral asymmetry doping profile devices exhibit smaller fluctuations of V_{th}, the on-state current (I_{on}), and the C_g than those of the vertical doping profile engineering devices. However, a large off-state current (I_{off}) fluctuation is induced because of the weak channel controllability near the source end.

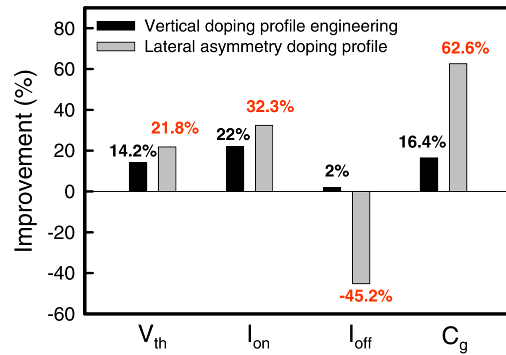

Fig. 8. (Color online) The improvement of DC and gate capacitance by vertical doping profile and the lateral asymmetry doping profile engineering with respect to the original doping profile.

Figures 9(a) and 9(b) respectively show $\sigma t_r/\sigma t_f$, and the nominal t_r/t_f for (A) the original doping profile devices, (B) the vertical doping profile engineering devices, (C) the lateral asymmetry doping profile devices, and (D) the inverters with shunt n-MOSFETs, respectively. The t_r and σt_r, of the original, vertical, and lateral asymmetry doping profile cases are similar due to the similar characteristics of p-MOSFETs and the use of the same nominal V_{th} for n-MOSFETs (140 mV). The nominal t_r for the inverter with shunt n-MOSFETs scenario is increased due to the increased number of transistor, resulting in greater load capacitance in circuit. Moreover, due to the increased number of transistor, the number of fluctuation sources in the circuit is increased, resulting in increased σt_r. For the fall time characteristics, the values of σt_f for the vertical and lateral asymmetry doping profile devices are decreased due to the smaller C_g and I_{on} fluctuations. The reduction in fluctuation is not significant due to the small load capacitance in this simulation scenario. For the CMOS inverters with shunt n-MOSFETs, due to the increased number of n-MOSFETs to discharge the load capacitance, the nominal t_f and σt_f are significantly decreased. Figure 9(c) summarizes the normalized maximal rise and fall time fluctuations, which are defined by $\max(t_{r/f,\text{fluctuation}} - t_{\text{nominal}})/t_{\text{nominal}}$. The vertical

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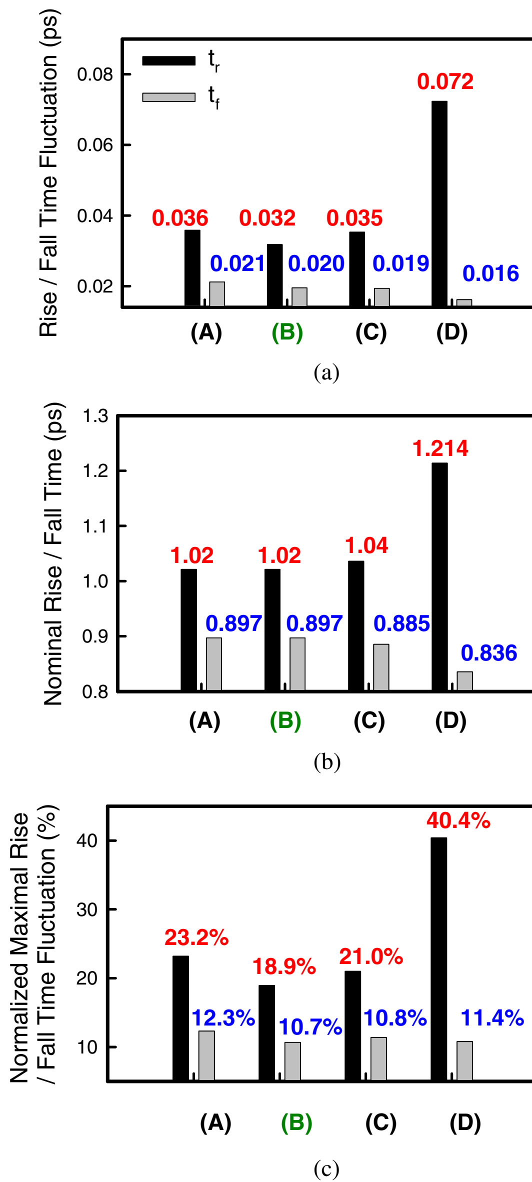

Fig. 9. (Color online) (a) The rise/fall time fluctuation, (b) the nominal rise/fall time, and (c) the normalized maximal rise/fall time fluctuation for (A) the original doping profile, (B) the vertical doping profile engineering, (C) the lateral asymmetry doping profile, and (D) the inverter with shunt n-MOSFETs.

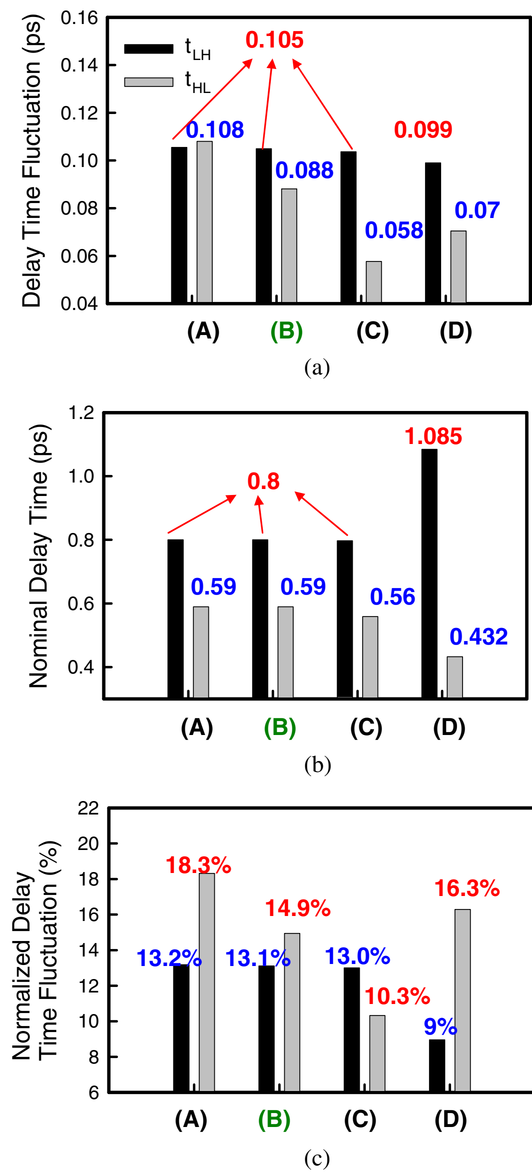

Fig. 10. (Color online) (a) The low-to-high/high-to-low delay time fluctuation, (b) the nominal low-to-high/high-to-low delay time, and (c) the normalized low-to-high/ high-to-low delay time fluctuation for (A) the original doping profile, (B) the vertical doping profile engineering, (C) the lateral asymmetry doping profile, and (D) the inverter with shunt n-MOSFETs.

doping profile engineering device shows a slightly greater improvement of fluctuation in rise time and fall time characteristics owing to the smaller short-channel effect and the I_{off} fluctuation than the lateral asymmetry doping profile device. Note that although the CMOS inverters with shunt n-MOSFETs does not show the smallest normalized rise and fall fluctuations, its nominal t_f and σt_f are smallest at the cost of worse t_r and σt_r. Figures 10(a) and 10(b) show the delay time fluctuation and the nominal delay time, respectively. Because of the similar threshold voltage fluctuation of p-MOSFETs, t_{LH} and σt_{LH} for (A) the original, (B) the vertical, and (C) the lateral asymmetry doping profiles devices are similar. The lateral asymmetry doping profile devices exhibit the smallest σt_{HL} owing to the smallest threshold voltage fluctuation of n-MOSFETs, as depicted in Fig. 8. For σt_{LH}, (D) the inverters with shunted n-MOSFETs exhibit the smallest fluctuation at the cost of a larger t_{LH}. The high-to-low and low-to-high transitions of the inverters with shunted n-MOSFETs are investigated with respect to the original cases in Figs. 11(a) and 11(b), respectively. Since the high-to-low transition starts upon one of the nMOS transistors being turned on, t_{HL} and σt_{HL} are reduced owing to the higher probability for the inverters with low V_{th} n-MOSFETs. However, for the low-to-high transition, the transition becomes significant as both the shunt n-MOSFETs are turned off. Therefore, the t_{LH} is increased. Similarly, σt_{HL} is suppressed owing to the higher probability for the inverters with low V_{th} n-MOSFETs. The occurrence of different V_{th} of n-MOSFETs explains the increased t_{LH} and the decreased $t_{HL}/\sigma t_{HL}/\sigma t_{LH}$ in Figs. 10(a) and 10(b). Figure 10(c) and Table I summary the normalized delay time fluctuation, and the improvements obtained by the three fluctuation suppression techniques with respect to the original cases. The inverter with shunt n-MOSFETs

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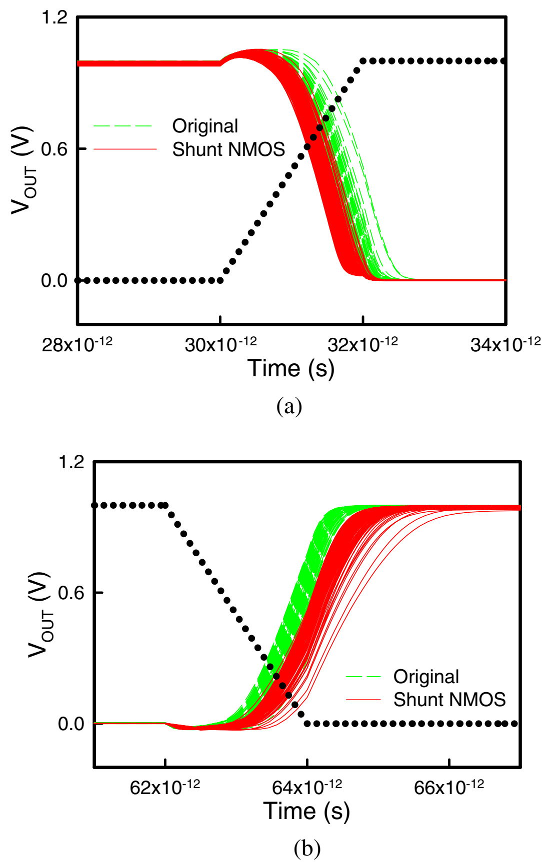

Fig. 11. (Color online) Comparison of the (a) high-to-low and (b) low-to-high delay times for the original inverter circuit and the inverter circuit with shunt n-MOSFETs.

shows the smallest nominal t_{HL} at the cost of higher t_{LH}. With the except of this case, the lateral asymmetry doping profile cases exhibit the smallest normalized delay time fluctuations at the cost of larger short-channel effect and power consumption. For low-power applications, vertical doping profile engineering can be appropriate because it can improve the timing characteristics with only a slight effect on the leakage power of the circuit. The inverters with shunt n-MOSFETs may reduce t_f, σt_f, t_{HL}, σt_{LH}, and σt_{LH} effectively. However, t_{LH} and leakage power are increased due to the occurrence of a V_{th} mismatch. Moreover, the chip area is larger. The shunt transistor approach is suitable to suppress the fluctuations of the most fluctuation sensitive element in circuits.

4. Conclusions

In this study, a 3D "atomistic" device-circuit-coupled simulation approach has been proposed to investigate the random-dopant-induced transient characteristic fluctuations in nanoscale CMOS circuits, concurrently capturing the random discrete-dopant-number- and random discrete-dopant-position-induced fluctuations. Our preliminary results show that the number of discrete dopants, varying from zero to 14 in the 16-nm-gate CMOS inverter circuits, results in a 3.5% variation of the rise time, a 2.4% variation of the fall time, an 18.3% variation of the high-to-low delay time, and a 13.2% variation of the low-to-high delay time. The significant transient characteristic fluctuations induce significant delay and timing variations in circuits and systems. Three fluctuation suppression techniques proposed from the device and circuit viewpoints are implemented to examine the associated intrinsic fluctuation. The inverter with shunt n-MOSFETs may reduce t_f, σt_f, t_{HL}, σt_{LH}, and σt_{LH} effectively at the cost of a increase of t_{LH}, leakage power, and chip area. Therefore, to pursue the smallest delay time fluctuation, the lateral asymmetry doping profile engineering is suitable at the cost of a larger short-channel effect and higher power consumption. The improvement of transient characteristics fluctuation for vertical channel doping profile engineering is not as effective as the other techniques; the leakage current is not significantly increased and may therefore be suitable for low-power applications. The proposed analyzing approach was used to explore the fluctuation of transient behavior in nanoscale CMOS circuits and examine the corresponding fluctuation suppression techniques. It is considered that links should be established between circuit design and fundamental device technology to allow circuits and systems to accommodate the individual behavior of every transistor on a silicon chip.

Table I. Improvement obtained from the three fluctuation suppression techniques with respect to the original doping profile. (+: improved; −: degraded) [*We assume the layout area for one device and for one shunt device are approximately 1 and 1.75 arbitrary unit, respectively. The layout area for the original inverter and the shunted n-MOSFETs inverter are approximately 2 and 2.75 arbitrary unit, respectively. The increase in the size of the chip area is (2.75 − 2)/2 = 37.5%.]

Improvement (%)	Vertical doping profile engineering	Lateral asymmetry doping profile	Shunt nMOS circuit topology
Fall time fluctuation	+3.0	+7.3	+12.2
Rise time fluctuation	+18.5	+9.5	−72.4
High-to-low delay time fluctuation	+18.6	+43.71	−10.9 (t_{HL}: +73%)
Low-to-high delay time fluctuation	+0.76	+1.5	+31.8 (t_{LH}: −37.5%)
Area cost	0	0	−37.5%*

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