Single-Inductor Multi-Output (SIMO) DC-DC Converters With High Light-Load Efficiency and Minimized Cross-Regulation for Portable Devices

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***Abstract*—A load-dependant peak-current control single-inductor multiple-output (SIMO) DC-DC converter with hysteresis mode is proposed. It includes multiple buck and boost output voltages. Owing to the adaptive adjustment of the load-dependant peak-current control technique and the hysteresis mode, the cross-regulation can be minimized. Furthermore, a new delta-voltage generator can automatically switch the operating mode from pulse width modulation (PWM) mode to hysteresis mode, thereby avoiding inductor current accumulation when the total power of the buck output terminals is larger than that of the boost output terminals. The proposed SIMO DC-DC converter was fabricated in TSMC 0.25 μm 2P5M technology. The experimental results show high conversion efficiency at light loads and small cross-regulation within 0.35%. The power conversion efficiency varies from 80% at light loads to 93% at heavy loads.**

***Index Terms*—Cross-regulation, single-inductor multi-output (SIMO) DC-DC converter, SoC system.**

I. Introduction

TODAY'S power management units of portable products require high power conversion efficiency, fast line/load transient response, and small power module volume. In particular, cell phones, digital cameras, MP3 players, PDAs, and portable products require varied voltage/current levels of power supplies for delivery to different sub-modules in portable products. Thus, there are different designs that provide different voltage/current levels as shown in Fig. 1. Low dropout (LDO) regulator arrays are one of the designs for different voltage/current levels as depicted in Fig. 1(a), where the index i is from 1 to n which is used to index the nth output. However, LDO regulator arrays sacrifice power conversion efficiency and greatly reduce battery life. The other solution is illustrated in Fig. 1(b), which combines with different inductive switching converters. The high power conversion efficiency is ensured by the inductive switching converter. However, the large number of inductors occupies the large footprint area and increase fabrication cost. To achieve microminiaturization and high power conversion efficiency for a power management unit, the single inductor multiple output (SIMO) DC-DC converter has been developed as a suitable solution. The conceptual SIMO DC-DC converter is shown in Fig. 1(c). It only uses one inductor component to generate multiple voltage/current levels for different sub-modules in the portable products. The SIMO DC-DC converter not only reduces the footprint area and fabrication cost but also provides highly power conversion efficiency [1]. However, all load current conditions of the multiple output terminals arise in the current level of the inductor. When the load current condition of each output accumulates in the same inductor, the design challenges of the SIMO DC-DC converter such as cross-regulation, power conversion efficiency, system stability, and lack of flexibility of both the buck and boost must be seriously addressed. Thus, several topologies and control techniques have been proposed to implement SIMO DC-DC converters [2]–[13]. The SIMO DC-DC converter in [1] uses the peak current control method and state machine to regulate output voltage. The work in [2] proposed the charge control method and divided one period to regulate the multiple output voltages. Due to the high freewheeling current level, the power conversion efficiency is greatly decreased in light load condition. The works in [3] and [10] calculate the cross-regulation problem when one period is divided to regulate the multiple boost output voltages. Moreover, the work in [10] proposed the pseudo-continuous conduction mode (PCCM) which involves the advantages of continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The works in [4]–[8], and [12] show time multiplexing (TM) techniques to regulate the multiple output voltages and to reduce cross-regulation. The works in [11] are proposed to monitor freewheeling current as the inductor current control method for dual boost output voltages. The work in [13] orders the power distribution of four boost output voltages. Its first three output voltages are controlled using comparators and are thus called comparator-controlled output voltages, while the last-ordered output is P-I controlled with an error amplifier. However, the flexibility of the buck and boost output voltages is limited by the structure of the converter and control methodology. Thus, to simultaneously generate buck and boost output voltages, the previous works in [2] proposed the charge control method and used minimum switches to provide one buck and one boost output voltage. The SIMO DC-DC converter which uses minimum switches is going to cause charge accumulation in the inductor during unbalanced output loads. Thus, this paper studies previous design problems and applies extended solutions to a study case. A load-dependant peak-current control SIMO DC-DC converter with hysteresis mode is proposed to provide multiple buck and boost output voltages and to solve

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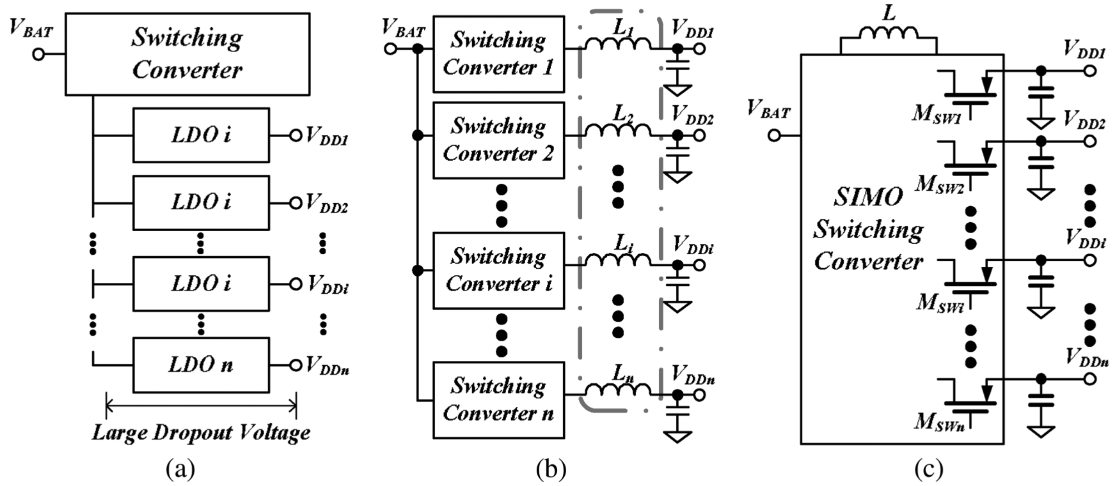


Fig. 1. Different power management designs. (a) Use of many LDO regulators. (b) Use of many switching converters. (c) Use of a single-inductor and multiple-output converter.

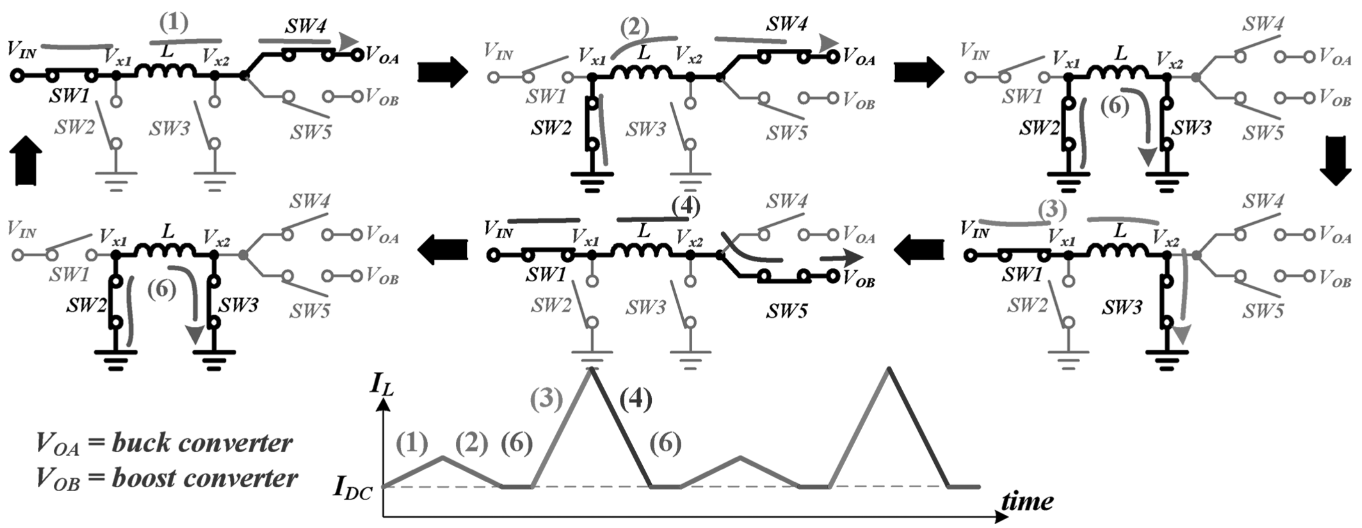


Fig. 2. Conventional SIDO DC-DC converter with one buck and one boost output in [2], and [12].

the challenges of cross-regulation, power conversion efficiency, and system stability [9].

The organization of this paper is as follows. Section II describes the minimum switch methodology of the SIMO DC-DC converter with the load-dependent peak-current control technique in order to improve cross-regulation and light load efficiency. Section III describes the implementation of the proposed SIMO DC-DC converter. Section IV presents the power comparator and delta-voltage generators to smoothly switch the operating mode between the PWM and hysteresis modes. In Section V, the experimental results show the minimized cross-regulation and performance of the proposed SIMO DC-DC converter. Finally, the conclusion is made in Section VI.

II. Minimum Switch Number Structure With the Load-Dependant Peak-Current Control Technique

A. Controlling Sequence Used to Minimize the Number of Switches

Fig. 2 shows the topology of a conventional single inductor dual output (SIDO) DCDC converter with buck and boost output voltages [2] and [12]. Five kinds of inductor current path are used to regulate the output voltages during one switching cycle. Paths 1 and 2 provide the charge to the buck output V_{OA}. Paths 3 and 4 deliver the charge to the boost output V_{OB}. Path 6 is used to hold the charge in the inductor and to function as a freewheeling current loop. As in previous works, the minimum number of power switches is shown in [10], [11], and [13]. These works generated the boost output voltages and controlled the storage charge of the inductor in order to regulate the output voltage during one switching cycle. Thus, to minimize the number of power switches in the SIMO DC-DC converter, the dual boost output terminals converter as shown in Fig. 3 is going to generate one buck and one boost output voltage [2]. According to the operation of conventional SIDO DC-DC converter, paths 1, 3, and 4 must be kept in the structure. Path 1 is the only one path to deliver charge to the buck output. Path 3 is the only choice to store charge in the inductor with a large current slope, and path 4 is the only path to deliver charge to the boost output. Furthermore, the buck output voltage can only be regulated by path 1. Thus, path 2 can be removed. This means the switches S_1 and S_2 in Fig. 2 are removed for a minimum number of power switches. After the removal of path 2, a switch S_6 is added to generate a freewheeling current loop.

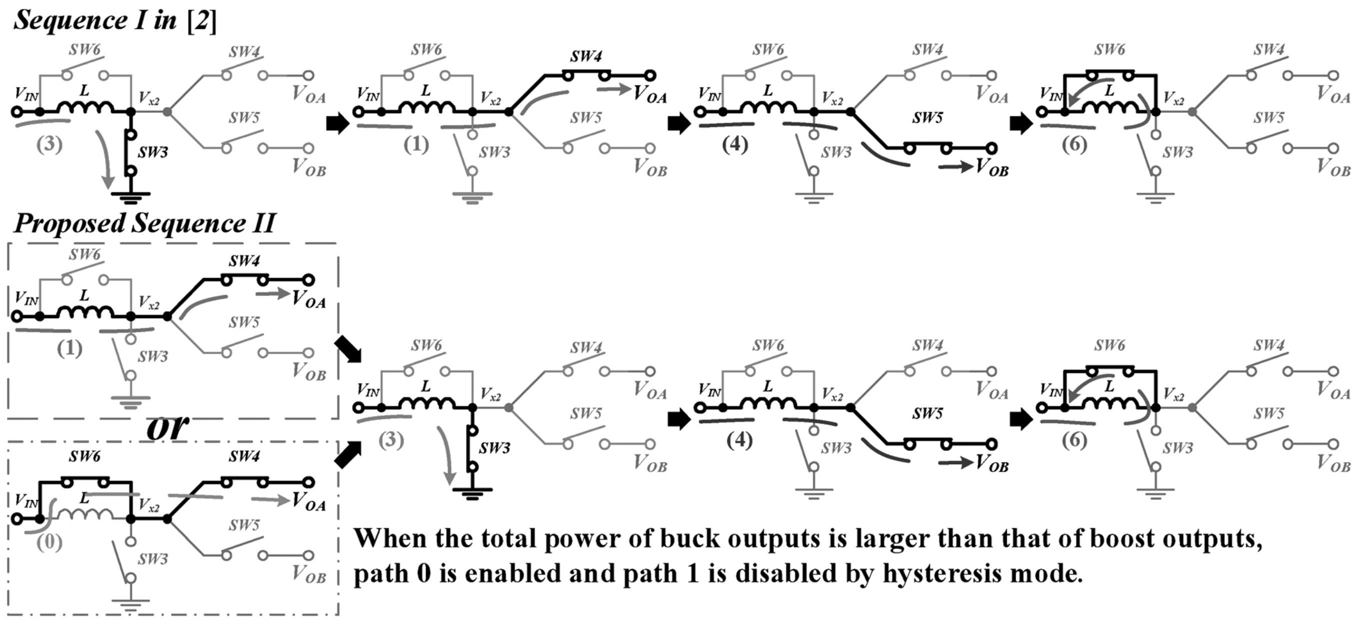


Fig. 3. Topology of minimum number of switches in [2] with one buck and one boost output voltage, and the proposed controlling sequence and path 0 of the hysteresis mode.

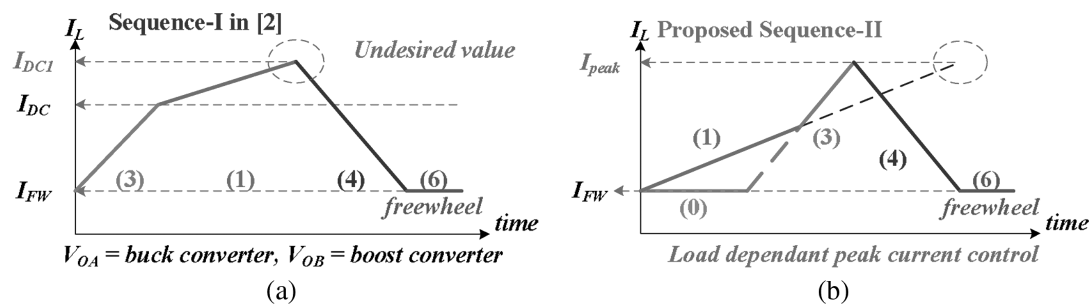


Fig. 4. Comparison of two topologies with four switches to implement the SIDO DC-DC converter. (a) The previous proposed controlling Sequence-I in [2]. (b) The proposed Sequence-II with the load-dependant peak current control technique.

A previous controlling sequence-I is depicted for one buck and one boost output in Fig. 4(a) [2]. At the beginning of each switching cycle, path 3 in Fig. 3 stores the charge of the inductor from the freewheeling current level I_{FW} to the pre-defined and fixed current level I_{DC}. Then path 1 is selected to deliver charge to the buck output, and the inductor current level is increased to the value I_{DC1}, which is dependent on the load condition of the buck output at the same time. After buck output operation, the boost output draws the charge from path 4, and the inductor current drops back to I_{FW}. Finally, the current level I_{FW} of the inductor is kept by path 6. The inefficient performance is the major disadvantage since the inductor current is increased to a highly undesired value if the buck output is derived during heavy load condition. The other drawback is the pre-defined and fixed I_{DC} that contribute to the highly freewheeling current level and the serious decrease in power conversion efficiency in the light-load condition. The highly undesired current value I_{DC1} of the inductor also causes the serious cross-regulation in the output voltages. As a result, there is difficulty in ensuring the conversion efficiency and minimum cross-regulation of the controlling sequence-I. Furthermore, when the load condition of the buck output is larger than that of the boost output in the structure of Fig. 3, the storage charge of the inductor accumulates without a releasing path. The highly current level appears in the inductor and results in unregulation. To address these issues, a new controlling sequence-II with the load-dependent peak-current control technique is presented as illustrated in Fig. 4(b). In the beginning of controlling sequence-II, path 1 is used to simultaneously regulate the buck output voltage and store the charge in the inductor. After path 1, the inductor current is rapidly increased to the load-dependant peak-current control level I_{peak} by path 3. Then controlling sequence-II switches to path 4 to draw the charge of the inductor to boost the output; after which, it drops back to the current level of the inductor to I_{FW}. Finally, the current level of the inductor is kept by path 6. Since the current level I_{peak} increases during heavy load condition and decreases during light load condition, the power losses during the freewheeling loop can be minimized. Due to the storage charge of the inductor in path 1 having been fully taken into account in controlling sequence-II, the highly undesired value I_{DC1} is eliminated. Thus, power conversion efficiency and cross-regulation can be improved. In addition, a hysteresis control mode has been proposed to eliminate the unregulation during the unbalanced load condition in the next section.

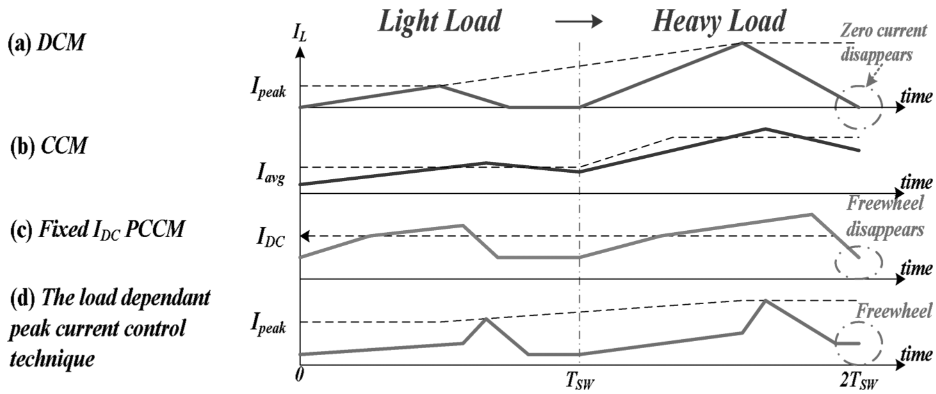


Fig. 5. Scenarios of different operation modes when the load current changes from light to heavy. (a) DCM; (b) CCM; (c) fixed I_{DC} PCCM; (d) the load dependent peak current control technique.

B. Load-Dependent Peak-Current Control for Improving Light-Load Efficiency and Reduction of Cross-Regulation

The inductor waveform represents the status of storage charge and the order of the system. Four inductor current waveforms are depicted in Fig. 5. At first, the inductor current waveform of the operation of DCM is shown in Fig. 5(a). The order of the system is equal to one, and one low-frequency pole exists in the closed loop. When the power is larger than the maximum power limitation of DCM, the inductor current will switch to CCM operation as shown in Fig. 5(b). The order of the system becomes two and thus the compensation of the system needs a complicated method like a proportional-integral-differential (PID) compensator to ensure large low-frequency gain and a suitable phase margin. The PCCM operation was proposed to address the disadvantages in DCM or CCM operation [3] and [10], [11]. The PCCM technique sets a fixed inductor current DC level to store enough energy in the inductor as depicted in Fig. 5(c). Thus, the order of the system is similar to that in DCM operation, while the maximum power delivered by the operation of PCCM is larger than that in DCM operation. This simplifies the compensation scheme. Once the disappearance of the freewheeling stage happens when the load current exceeds the maximum power limitation or when a sudden load current rises from light to heavy, the stability and minimized cross-regulation are not guaranteed since the order of the system becomes two. As illustrated in Fig. 5(d), the load-dependent peak-current control technique is proposed to adaptively store suitable charge in the inductor. When the load current becomes small, the peak current level will be decreased to a small current level to ensure high power conversion efficiency at light loads. Furthermore, a minimum peak inductor current is defined to prevent the output from having a too large transient dip voltage.

III. The Implementation of the Proposed SIMO DC-DC Converter

According to the proposed controlling sequence-II and the load-dependent peak-current control technique, the architecture of the proposed SIMO DC-DC converter is illustrated in Fig. 6. The following sub-sections describe the details of the sub-modules.

A. Load-Dependent Peak-Current Decision Circuit

To improve the power conversion efficiency at light loads and to reduce the effect of cross-regulation, a peak current decision circuit is depicted in Fig. 7. All output voltages of the error amplifiers are converted current signals by the V-I converters. Each V-I converter outputs two current output signals with a conversion ratio $(1 : N : M)$. The current signals $I_{EK1} \sim I_{EKn}$ and $I_{ET1} \sim I_{ETn}$ (the index i is 1 to n) are used to work as discharging currents of the charge reservation circuit. The other $2n$ current signals are summed to generate the load-dependent peak-current $I_{peak(dynamic)}$, which varies with load currents. Furthermore, to avoid the zero inductor peak current, a minimum peak inductor current is set by a current source $I_{DC(\min)}$. The non-inverting input of the comparator is decided by the voltage signal V_{Ipeak}, which is generated by flowing two current signals $I_{peak(dynamic)}$ and $I_{DC(\min)}$ through the resistor R_{peak}. The value of V_{Ipeak} is determined by

$$V_{Ipeak} = R_{peak} \cdot \left(I_{peak(dynamic)} + I_{DC(\min)}\right). \quad (1)$$

The input voltages of the V-I converters are $V_{EK1} \sim V_{EKn}$ and $V_{ET1} \sim V_{ETn}$ from the error amplifier array that indicates the load conditions of all multiple buck and boost output terminals. For a dip in one of the output terminals due to an increase in load current, for example, the control system increases the duty ratio, which in turn indirectly causes an increased peak inductor current. The energy stored in the inductor is gradually increased to minimize cross-regulation due to the load-dependant peak inductor current level at heavy loads. Similarly, the period of freewheel stage occupies little duration of every switching cycle. The order of the system is still kept as one, and the power dissipation is always kept small. Therefore, the proportional-integral (PI) compensator can ensure the stability of the system, and the heavy-load power conversion efficiency can be kept high.

B. The Current Sensor and Charge Reservation Circuits

The current sensor shown in the left side of Fig. 8 [2] and [3] has register R_S which is N times of the sensing resistor R_{SEN}. To achieve the load-dependant peak-current control technique, the current sensor cannot be turned off during the whole switching cycle. Thus, the freewheeling power MOSFET as illustrated in Fig. 6 is connected between the input power

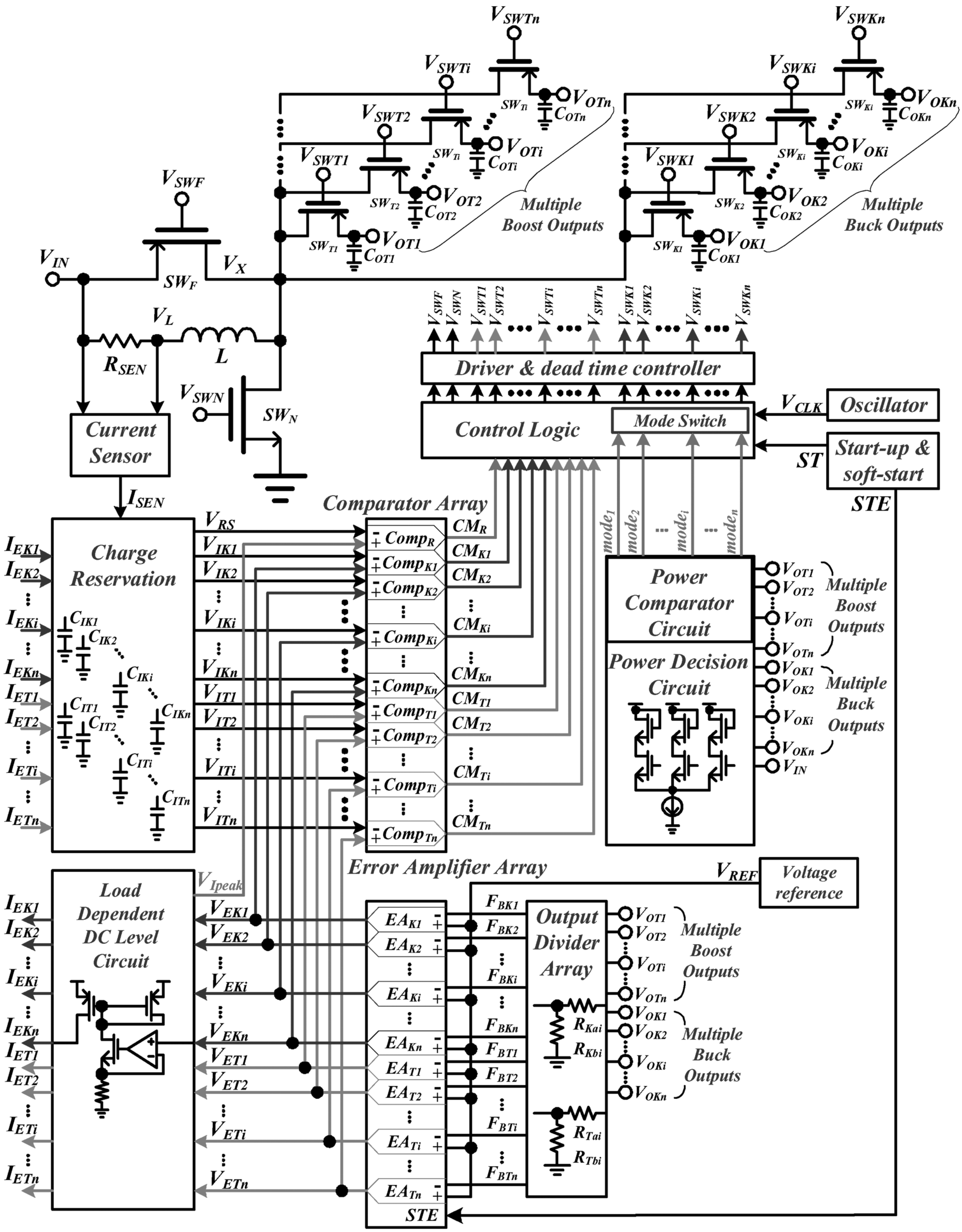


Fig. 6. The proposed load-dependent peak current control SIMO DC-DC converter with hysteresis mode for high power conversion efficiency and minimum cross-regulation.

source and the node V_X at the expense of power conversion efficiency during the freewheeling stage. The architecture of the charge reservation circuit is shown in the right side of Fig. 8. The sensing current I_{sense} is converted to the voltage V_{RS}, which is sent to compare with the peak current level V_{Ipeak} as illustrated in Fig. 6. The sensing current is also used to determine the individual duty cycle of each buck or boost output. Thus, there are $2n$ charge monitoring circuits in the charge

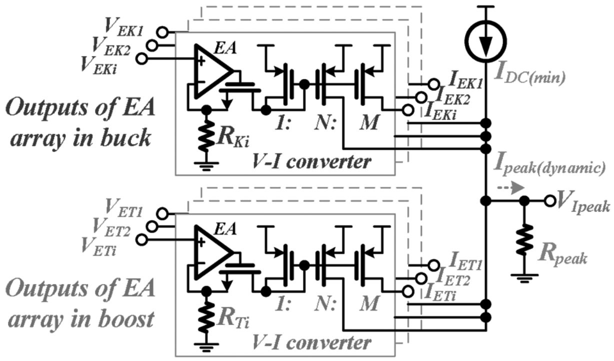


Fig. 7. The load-dependent peak current control circuit dynamically adjusts the peak current level according to the value of the load current.

reservation circuit. The internal capacitors $C_{IK1} \sim C_{IKn}$ and $C_{IT1} \sim C_{ITn}$ are used to monitor the buck and boost output voltages, respectively. The charge monitoring circuit in the sub-block is also shown in Fig. 8. When the voltage of V_{SW} is low, I_{sense} flows into capacitor C_I to indicate the energy delivering condition of one of buck or boost output voltage. Once the voltage V_{SW} changes from low to high, the discharging current I_{in}, which comes from the load-dependence peak-current control circuit, starts to discharge capacitor C_I. Thus, the values of $\Delta V_{IK1} \sim \Delta V_{IKn}$ and $\Delta V_{IT1} \sim \Delta V_{ITn}$ on $C_{IK1} \sim C_{IKn}$ and $C_{IT1} \sim C_{ITn}$ can monitor the status of the buck and boost output voltages. As a result, the duty cycle can be determined by voltage V_I on the capacitor C_I and the feedback voltage V_{EKi} (or V_{ETi}) after the operation of the comparator in Fig. 6.

Assume that the value of ΔV_{IKi} (or ΔV_{ITi}) is k_{Ki} (or k_{Ti}) times that of ΔV_{OKi} (or ΔV_{OTi}) for the buck (or boost) output i, and the index i is 1 to n. The values of ΔV_{IKi} and ΔV_{ITi} are set within the input common mode range of the comparator array in Fig. 6. Since the value of I_L is N times that of I_{sense}, the values of internal capacitors C_{IKi} (or C_{ITi}) in the charge reservation circuit are $1/Nk_{Ki}$ (or $1/Nk_{Ti}$) times that of C_{OKi} (or C_{OTi}), respectively. To generate the discharging current I_{in}, which comes from the load-dependence peak current control circuit in Fig. 7, the values of resistor R_{Ki} and R_{Ti} are described as (2) for the buck output i and for the boost output i.

$$R_{Ki} = \frac{G\beta_{Ki}t_{Ki}}{Nk_{Ki}C_{IKi}} \text{ and } R_{Ti} = \frac{G\beta_{Ti}t_{Ti}}{Nk_{Ti}C_{ITi}} \tag{2}$$

G and β_{Ki} (or β_{Ti}) are the transconductance of the error amplifier and the ratio of the voltage divider, respectively. The values of the resistors R_{Ki} and R_{Ti} ensure that the discharging currents are proportional to the load current. The values of the discharging currents are expressed as (3) for buck output i and boost output i, respectively.

$$I_{EKi} = V_{EKi}\frac{Nk_{Ki}C_{IKi}}{G\beta_{Ki}t_{Ki}} \text{ and } I_{ETi} = V_{ETi}\frac{Nk_{Ti}C_{ITi}}{G\beta_{Ti}t_{Ti}} \tag{3}$$

The charge stored on internal capacitor C_{IKi} or C_{ITi} can effectively represent the regulated output voltage at the buck or boost output terminal. Thus, the proposed charge reservation circuit can accurately decide the duty cycle of the buck or boost output terminals.

C. Logic Control Circuit With Automatic Mode Switch to Avoid Instability

The control logic generator with mode switch controller is depicted in Fig. 9. The operation of the control logic is divided into four durations (paths 1, 3, 4, and 5), which stand for the four energy delivering paths in Fig. 4(b). At the beginning of path 1, the clock signal V_{CLK} is triggered by positive edge, and its duty cycle is 90%. During Path 1, the energy is delivered to the multiple buck output terminals in Fig. 3. The input signal CM_{Ki} (i is 1 to n) is from one of the output voltages of the comparator array in Fig. 6, which decides the duty cycle of buck output i. At the same time, the inductor current is also increased. Once the signal CM_{Ki} changes to a low level when the value of VI_{Ki} is larger than that of VE_{Ki} in Fig. 6, path 3 starts to ensure sufficient energy to be stored in the inductor. In path 3, the signal V_{Ipeak} in (1) and the value of V_{RS} in Fig. 8 are used to determine the duty cycle of D_{SWN} for increasing the inductor current to the $I_{peak(dynamic)}$ level until the value of V_{RS} is large than that of V_{Ipeak}.

However, the duty cycle of D_{SWN} may be zero if the inductor current is increased to exceed the $I_{peak(dynamic)}$ level during path 1. This means that the inductor current level is high enough to provide sufficient energy to the multiple boost output terminals after path 1. There is no need to store more charge in the inductor since it may cause current accumulation in Fig. 10. Once the value of V_{RS} is large than that of V_{Ipeak}, CM_R changes to a low level. Path 4 starts to deliver energy to the multiple boost output terminals. At the same time, the inductor current is decreased according to the load condition of the boost output voltages. Once CM_{Ti} is changed to a low level by the comparator array when the value of V_{ITi} is larger than that of V_{ETi}, the energy delivery to the multiple boost output terminals is completed. Then the controlling sequence enters path 6 named as freewheeling stage. That is, the energy is reserved in the inductor. The longer the period of the freewheeling stage is, the lower the conversion efficiency. Owing to the adjustment of the inductor peak current, the inductor current level at the freewheeling stage is kept at a low level and thus the conduction loss can be reduced at light loads. All the output signals $D_{SWK1} \sim D_{SWKn}$, D_{SWN}, $D_{SWT1} \sim D_{SWTn}$, and D_{SWF} of the control logic generator are converted by the driver and the dead-time controller block shown in Fig. 6 to the gate control signals $V_{SWK1} \sim V_{SWKn}$, V_{SWN}, $V_{SWT1} \sim V_{SWTn}$, and V_{SWF}, which are used to control the power MOSFET switches $SW_{K1} \sim SW_{Kn}$, SW_N, $SW_{T1} \sim SW_{Tn}$, and SW_F.

As illustrated in Fig. 10, current accumulation occurs when the power of the buck output terminals is larger than that of the boost output terminals. The accumulated current causes serious cross-regulation and poor conversion efficiency at light loads. To address this problem, it is important to provide a hysteresis mode to alleviate the instability. In Fig. 3, at the hysteresis mode, path 1 is changed to path 0 to force the current to flow through switch S_6 to the buck output terminals. The energy of the buck output terminals does not cause current accumulation in the inductor. Thus, the converter works as a hysteresis buck converter, and the output voltage is directly regulated and limited

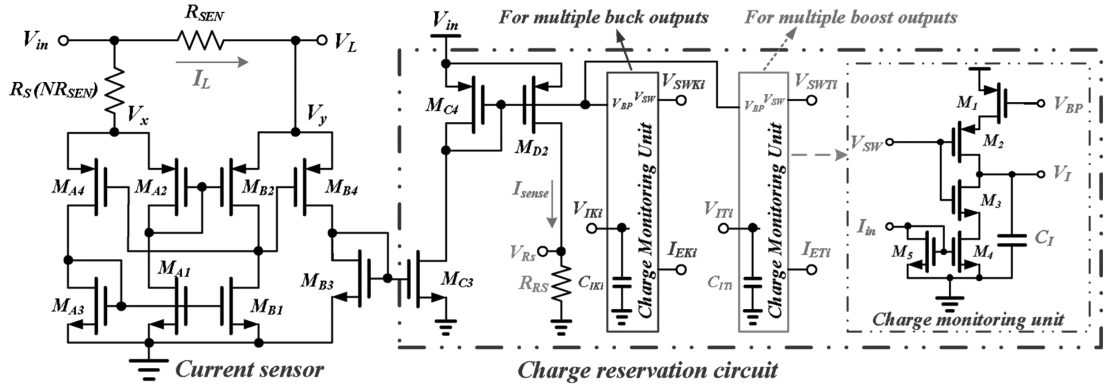


Fig. 8. The current sensor [2] and [3], charge reservation circuits, and the charge monitoring circuit for reducing output ripple.

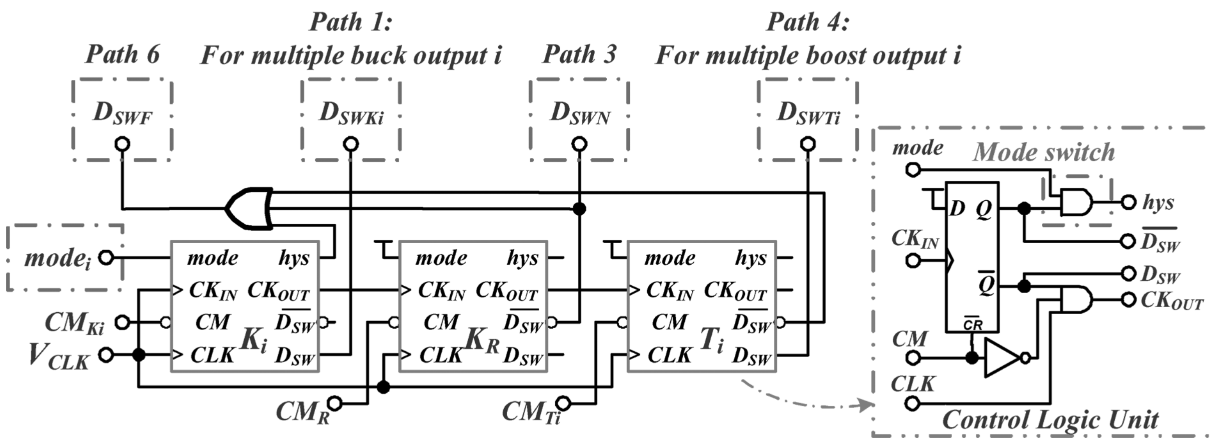


Fig. 9. The control logic generator with the mode switch controller.

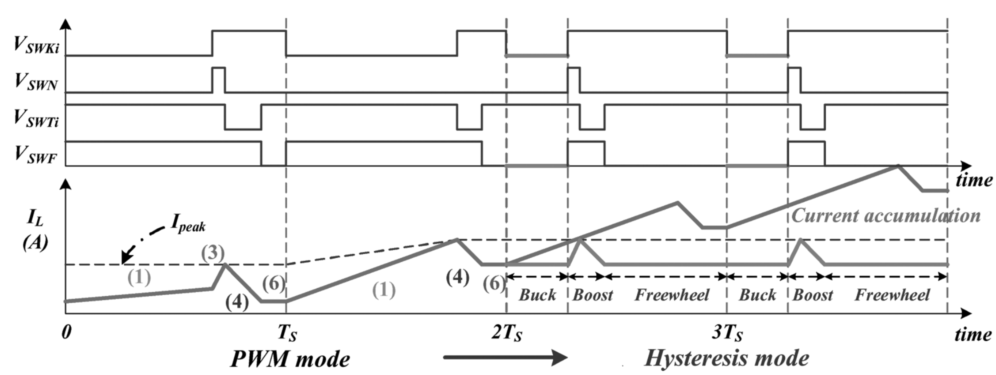


Fig. 10. Timing diagram of the transition from the PWM mode to the hysteresis mode.

by a hysteresis window. The control signal and inductor current waveform as depicted in Fig. 10 show the transition from the PWM mode to the hysteresis mode. To achieve the hysteresis control mode, a mode switch, a power comparator, and a novel delta-voltage generator are proposed. The mode switch as shown in the sub-block of Fig. 9 is composed of only one AND gate, and the signal "hys" is kept at a high level during the PWM operation until the signal "$mode_i$" that comes from the power comparator circuit is changed to a low level. Then the operation of the buck output is switched to the hysteresis mode. Since path 6 directly connects the buck output to the power supply, the output ripple is slightly increased for ensuring system stability during hysteresis mode.

IV. Power Comparator and Delta-Voltage Generator

To smoothly switch between two operation modes, the power comparator and delta-voltage generators are proposed to decide the operation mode of the converter.

A. Power Comparator Circuit

The inductor current waveform as depicted in Fig. 11 precisely describes the boundary condition between the PWM and

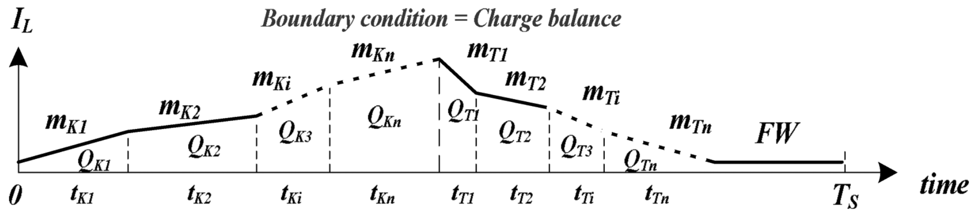


Fig. 11. The boundary waveform of the hysteresis control mode.

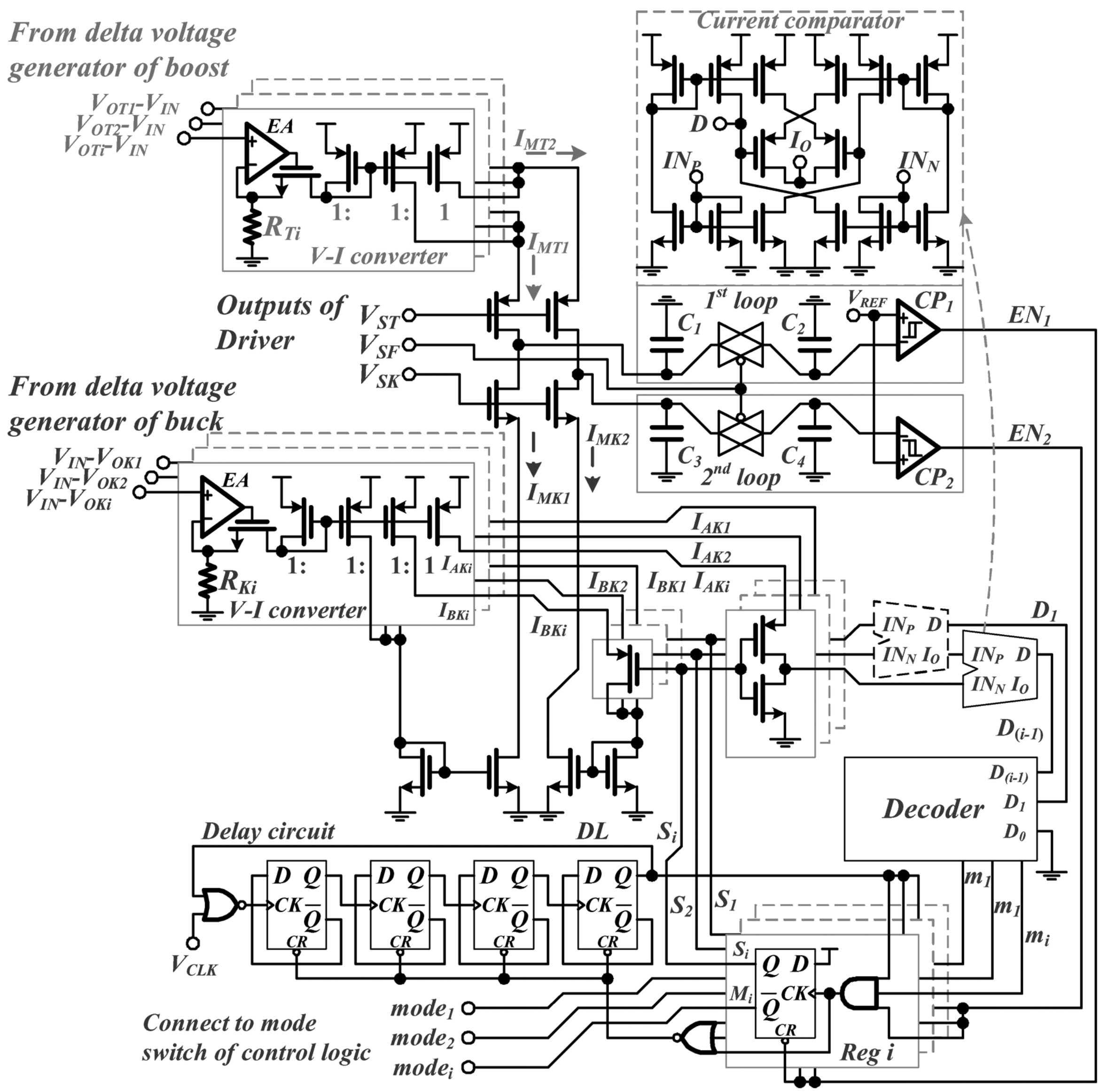


Fig. 12. The power comparator circuit.

hysteresis modes. Assume that the slopes of the inductor current for the buck and boost output terminals are expressed as (4). The operation modes and boundary condition can be determined by (5) and (7).

$$m_{Ki} = \frac{V_{IN} - V_{OKi}}{L} \text{ for buck output } i \quad \text{and}$$
$$m_{Ti} = \frac{V_{OTi} - V_{IN}}{L} \text{ for boost output } i \tag{4}$$

$$\sum_{i=1}^{n} m_{Ki} t_{Ki} < \sum_{i=1}^{n} m_{Ti} t_{Ti} \Rightarrow \sum_{i=1}^{n} Q_{Ki} < \sum_{i=1}^{n} Q_{Ti} \Rightarrow \text{PWM mode} \tag{5}$$

$$\sum_{i=1}^{n} m_{Ki} t_{Ki} > \sum_{i=1}^{n} m_{Ti} t_{Ti} \Rightarrow \sum_{i=1}^{n} Q_{Ki} > \sum_{i=1}^{n} Q_{Ti} \Rightarrow \text{Hysteresis mode} \tag{6}$$

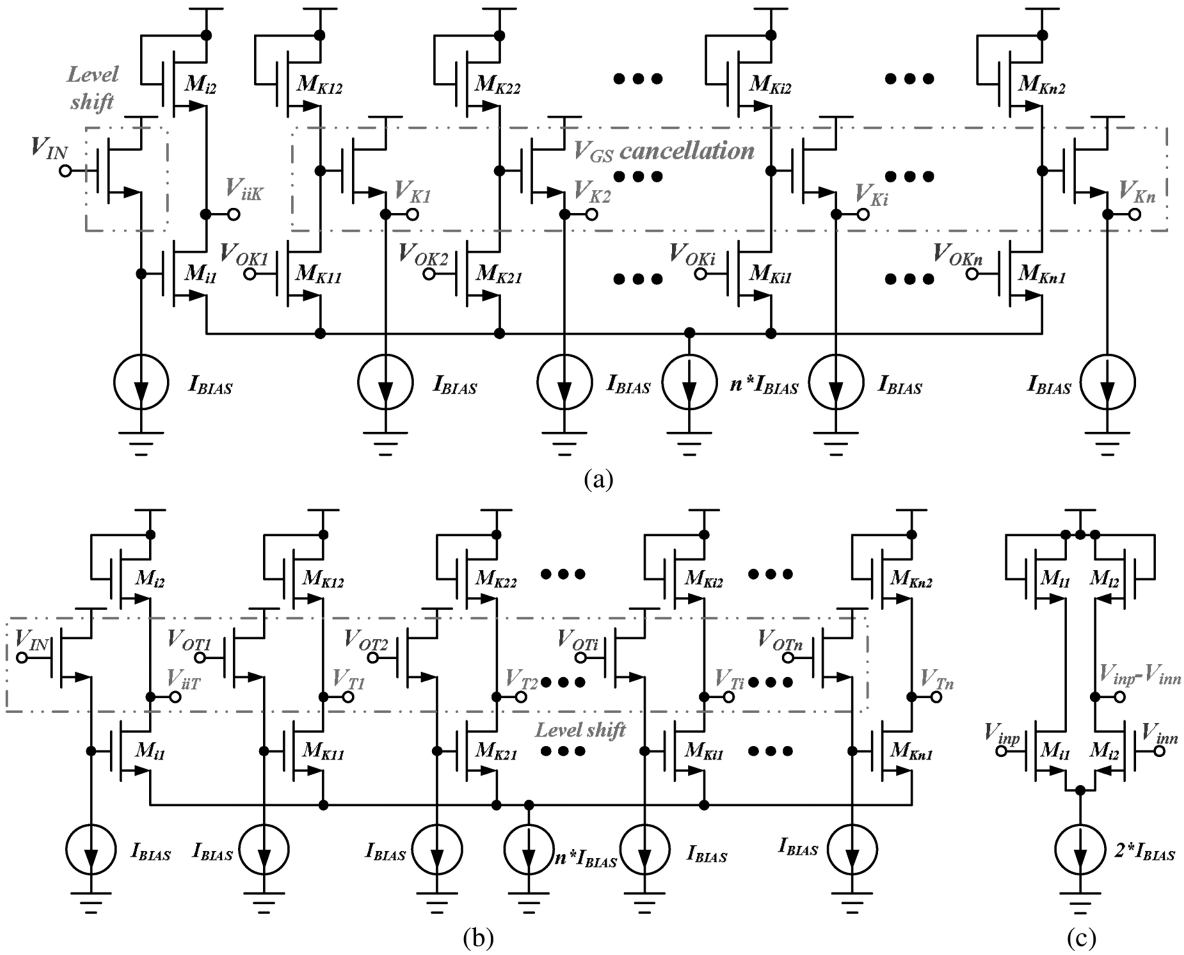


Fig. 13. (a) The power decision circuit for multiple buck output voltages. (b) The power decision circuit for multiple boost output voltages. (c) The differential transconductance amplifier for the generation of the inductor current slope.

$$\sum_{i=1}^{n} Q_{Ki} = \sum_{i=1}^{n} Q_{Ti} \Rightarrow \sum_{i=1}^{n} m_{Ki}t_{Ki} = \sum_{i=1}^{n} m_{Ti}t_{Ti} \Rightarrow \text{Boundary condition.} \quad (7)$$

In Fig. 12, the power comparator is used to decide which one of the multiple buck output terminals needs to enter hysteresis operation according to the largest load current. The summation current I_{mK1} and I_{mT1} indicate the slope values of the multiple buck and boost output terminals, respectively. I_{mK1} is used to discharge capacitor C_1 during the buck operation, and I_{mT1} is used to charge capacitor C_1 during boost operation. At the free-wheeling stage, the sample and hold (S/H) circuit sample the voltage on capacitor C_1 and hold it on the capacitor C_2. Thus, the boundary condition is monitored.

In the PWM mode, I_{MK1} is smaller than I_{MT1}, and E_{N1} is set to a low level in the first loop. The output signals $M_1 \sim M_i$ of registers $Reg.1 \sim Reg.i$ are set to a low level to disable the mode switch of Fig. 9. Thus, the mirrored current signals $I_{BK1} \sim I_{BKi}$ sum up in I_{MK2}, and all mirrored current signals $I_{AK1} \sim I_{AKi}$ of the delta-voltage generator for buck are separately switched to detect the maximum slope by the current comparators in Fig. 12. In the meanwhile, the generated I_{MK2} is compared with I_{MT2} and outputs the low state of E_{N2} in the second loop. This second loop is designed to detect the operating mode of each buck output according to the buck output with the largest load current selected for hysteresis mode. When the E_{N2} is low, the trigger signals of $Reg.1 \sim Reg.i$ are inhibited by E_{N2} and the output DL of delay circuit. The delay circuit is enabled to avoid the oscillation of the second loop and

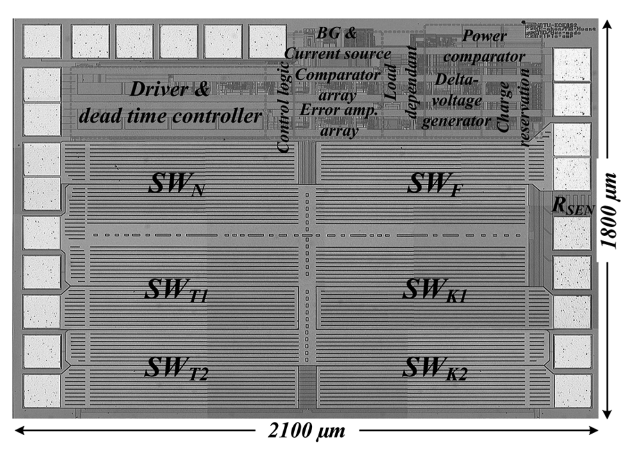


Fig. 14. Micrograph of the proposed SIMO converter, with the chip being $1800 * 2100\ \mu\text{m}^2$.

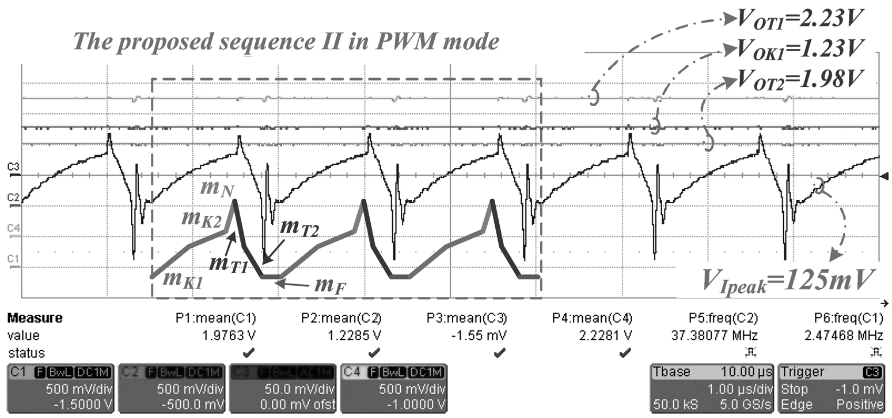
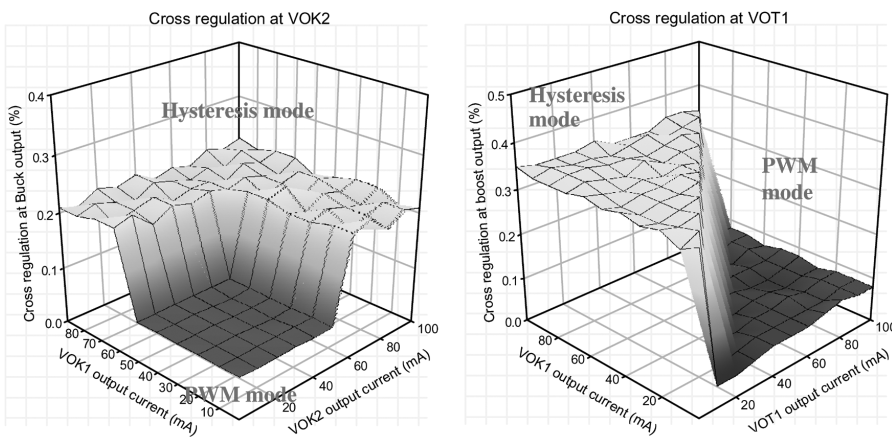


Fig. 15. The inductor current controlling sequence measured waveform with heavy loads.



(a) (b)

Fig. 16. The cross-regulation statistic chart of the SIMO DC-DC converter. (a) The cross-regulation at the buck output V_{OK2} in the PWM and hysteresis modes. (b) The cross-regulation at the boost output V_{OT1} in the PWM and hysteresis modes.

to ensure the storage charge in the steady state when one of the buck output terminals enters hysteresis mode.

When the loads of the buck output terminals are larger than those of boost the output terminals, E_{N1} and E_{N2} become high. $I_{AK1} \sim I_{AKi}$ flow into the current comparator and generate the detecting codes $D_1 \sim D_{(i-1)}$ during the period of delay circuit. The code is converted by (8) to indicate which one of the buck output terminals has the maximum loads and needs to operate in hysteresis mode.

$$\begin{aligned} m_1 &= \left(D_1 \cdot D_2 \cdot \ldots \cdot D_{(X-1)} \cdot D_X \cdot \ldots \cdot D_{(n-1)}\right), \\ m_2 &= \left(\overline{D}_1 \cdot D_2 \cdot \ldots \cdot D_{(X-1)} \cdot D_X \cdot \ldots \cdot D_{(n-1)}\right), \ldots, \\ m_X &= \left(\overline{D_{(X-1)}} \cdot D_X \cdot D_{(X+1)} \cdots \cdot D_{(n-1)}\right), \ldots, \\ m_i &= \left(\overline{D_{(i-1)}}\right) \end{aligned} \tag{8}$$

where the index X is from 1 to i. Once one of the buck output terminals is selected, m_X triggers $Reg.X$ to set the signal $mode_X$ to a low level. Moreover, the inverse S_X of $mode_X$ inhibits the related current signals I_{AKX} and I_{BKX}. As a result, I_{MK2} can be expressed as $I_{MK2(n)} = I_{MK2(0)} - I_{BKX(1)} - I_{BKX(2)} - \ldots - I_{BKX(n)}$, where the index n is used to indicate the n operating times of the second loop. $I_{MK2(n)}$ and $I_{BKX(n)}$ are the current signals by the n^{th} operation of the second loop according to the priority of loads. Once $I_{MK2(n)}$ is smaller than I_{MT2}, E_{N2} is set back to low. That is, the charge detection process is ended, and the proposed converter can really avoid the current accumulation and minimize the output ripples of the buck output terminals in hysteresis mode. The hysteresis mode can operate until I_{MK1} is smaller than I_{MT1}. E_{N1} is set to low, and the hysteresis mode is switched to PWM mode.

B. Delta-Voltage Generator

The novel delta-voltage generator is proposed in Fig. 13 to generate the different inductor current slopes for the smooth switching between the hysteresis and PWM modes. For the buck output terminals, the amplifier with multiple output voltages including V_{IN}, $V_{OK1} \sim V_{OKn}$ is depicted in Fig. 13(a). The block of the V_{GS} cancellation is used to remove the V_{GS} term in the difference voltage between V_{IN} and V_{Ki}. The amplifier with multiple output voltages is used to generate the intermediate values V_{iiK} and V_{Ki} from (9) to (10).

$$\begin{aligned} V_{iiK} = \frac{1}{n}\,[&(1-n) \times V_{IN} + V_{OK1} + V_{OK2} + \ldots + V_{OKi} + \\ &\ldots + V_{OKn} + (n-1) \times V_{GS}] \end{aligned} \tag{9}$$

$$\begin{aligned} V_{Ki} = \frac{1}{n}\,[&V_{IN} + V_{OK1} + V_{OK2} + \ldots + (1-n) \times V_{OKi} + \\ &\ldots + V_{OKn} + (n-1) \times V_{GS}]. \end{aligned} \tag{10}$$

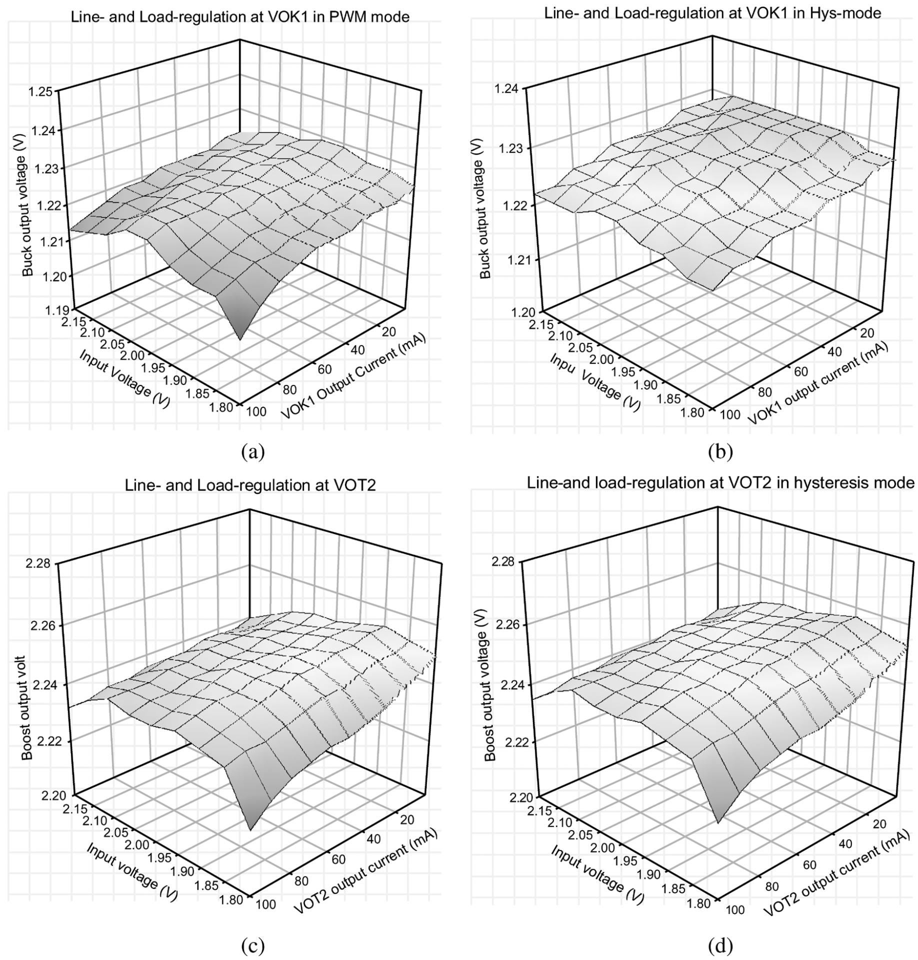


Fig. 17. The line and load regulation statistic charts. (a) The buck output voltage operates in the PWM mode when the boost output voltage operates at heavy loads. (b) The buck output voltage operates in hysteresis mode when the boost output voltage operates at light loads. (c) The boost output voltage in the PWM mode when the buck output voltage operates at light loads. (d) The boost output voltage in the hysteresis mode when the buck output voltage operates at heavy loads.

Similarly, for the multiple boost output terminals, the amplifier with multiple output voltages as shown in Fig. 13(b) can generate intermediate values V_{iiT} and V_{Ti} from (11) to (12).

$$V_{iiT} = \frac{1}{n} \cdot \left[(1-n) \times V_{IN} + V_{OT1} + V_{OT2} + \cdots + V_{OTi} + \cdots + V_{OTn} + n \cdot V_{GS} - \sum_{j=1}^{n} V_{GSj} \right] \tag{11}$$

$$V_{Ti} = \frac{1}{n} \cdot \left[V_{IN} + V_{OT1} + V_{OT2} + \cdots + (1-n) \times V_{OTi} + \cdots + V_{OTn} + n \cdot V_{GS} - \sum_{j=1}^{n} V_{GSj} \right]. \tag{12}$$

The current slope m_{Ki} of the buck output i is derived as (13). The inductor current slope m_{Ti} of the boost output i is derived as (14).

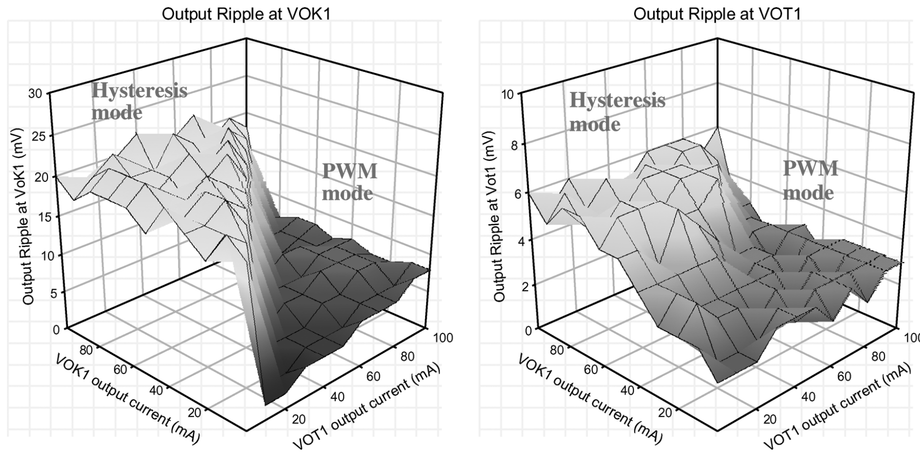
$$m_{Ki} = V_{Ki} - V_{iiK} = V_{IN} - V_{OKi} \tag{13}$$

$$m_{Ti} = V_{iiT} - V_{Ti} = V_{OTi} - V_{IN}. \tag{14}$$

(13) and (14) are implemented by the differential transconductance amplifier, which is illustrated in Fig. 13(c). V_{inp} and V_{inn} are connected to the output of the delta-voltage generator. All of output voltages m_{Ki} and m_{Ti} are sent to the input voltages of the power comparator circuit in Fig. 12. Therefore, the smooth transition between the PWM and hysteresis modes can be determined.

V. Measurement Results

The proposed SIMO DC-DC converter with the load-dependent peak-current control technique was implemented in TSMC 0.25 μm 2P5M technology. The micrograph of the SIMO DC-DC converter with 4 output terminals is shown in Fig. 14. The supply voltage is 1.8 V. The pre-defined output voltages are 1.25 V and 1.35 V for the two buck output voltages and 2.0 V and 2.25 V for the two boost output voltages, respectively. The measured inductor current waveform of the PWM mode at heavy loads is shown in Fig. 15. The ac coupling measurement of V_{Ipeak} clearly shows the controlling sequence-II in the inductor current, which is similar to the description in the previous section as illustrated in Fig. 4(b). Since large information was measured, the statistic chart is used to describe the performance of the proposed converter. The cross-regulation charts of the buck and boost output voltages are shown in Fig. 16(a) and (b), respectively. In Fig. 16(a), the load current of 50 mA is added to the boost output terminals in



(a) (b)

Fig. 18. (a) The output ripples estimation of buck output in the SIMO converter. (b) The output ripples estimation of boost output in the SIMO converter.

TABLE I
SUMMARY OF THE PERFORMANCE

Supply voltage		1.8V~2.2V @ Temperature = -20 °C ~ 120 °C			
Inductor		10 μH (±10%)			
Filter capacitor		33 μF with low ESR (small than 50mΩ)			
Switching frequency		660 kHz			
Process		TSMC 0.25μm 2P5M CMOS			
Chip area		1800*2100μm^2			
Converters		Buck$_1$ (V_{OK1})	Buck$_2$ (V_{OK2})	Boost$_1$ (V_{OT1})	Boost$_2$ (V_{OT2})
Output voltage		*1.25V*	*1.35V*	*2.0V*	*2.25V*
Output ripples	PWM mode	*4mV*		*3mV*	
	Hysteresis mode	*22mV*		*6mV*	
Load-regulation		*2%*	*1.5%*	*1%*	*0.9%*
Line-regulation		*0.8%/V*	*0.55%/V*	*0.5%/V*	*0.4%/V*
Cross-regulation	V_{OK1} at heavy load	*NA*	*0.22%*	*0.35%*	*0.31%*
	V_{OK2} at heavy load	*0.24%*	*NA*	*0.35%*	*0.31%*
	V_{OT1} at heavy load	*0.08%*	*0.074%*	*NA*	*0%*
	V_{OT2} at heavy load	*0.16%*	*0.074%*	*0.05%*	*NA*
Conversion efficiency	PWM mode	*90%*		*93%*	
	Hysteresis mode	*80%*		*NA*	

order to show the cross-regulation of different operation modes. This indicates that the hysteresis mode increases the cross-regulation from 0.07% to 0.22%. Similarly, the cross-regulation of the boost output V_{OT1} is shown in Fig. 16(b). It is slightly increased from 0.05% to 0.35% in the hysteresis mode. It is smaller than the value of 0.79% in the literature [1].

The line-and load-regulation charts of the buck output in PWM and hysteresis modes are shown in Fig. 17(a) and (b). In the PWM mode, the boost converter is operated at heavy loads. Contrarily, in the hysteresis mode, the boost converter is operated at light loads. The line-regulations of the buck output voltages are smaller than 0.8%/V, and the load-regulations of the buck output voltages are smaller than 2% in the two operating modes. Fig. 17(c) and (d) show the boost output voltages in the PWM and hysteresis modes. The results depict that the line-and load-regulations between the two modes are similar. The load-regulations of the boost output voltages are smaller than 1%, and the line-regulations of the boost output voltages are smaller than 0.5%/V. The output ripples of the buck and boost output voltages are depicted in Fig. 18(a) and (b). In the PWM mode, the output ripple is controlled by the values of the inductor and output capacitor, and thus the value is smaller than 4 mV$_{\mathrm{P-P}}$. In the hysteresis mode, the output ripple of the buck output voltages is increased to 22 mV$_{\mathrm{P-P}}$, and the output ripple of the boost output voltages is increased to 6 mV$_{\mathrm{P-P}}$. The power conversion efficiency is shown in Fig. 19. The PWM operation with load-dependent peak-current control has improved highly power conversion efficiency from 85% to 93%. In the hysteresis mode, due to the energy delivering path without flowing through the inductor, the conversion efficiency drops to 80%∼85%. The performance of the SIMO DC-DC converter is summarized in Table I.

VI. CONCLUSION

This paper proposes a compact-sized and highly efficient SIMO DC-DC converter for a portable device. The new proposed SIMO DC-DC converter with minimized switch transistors utilizes only a single inductor to provide multiple buck and multiple boost output voltages. The energy stored in the inductor can be effectively delivered to the buck or boost output

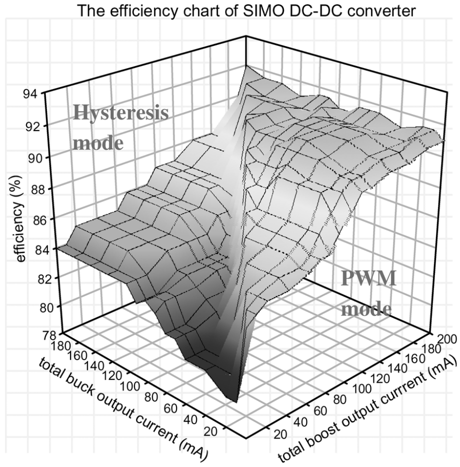


Fig. 19. Power conversion efficiency of the SIMO DC-DC converter with the load-dependant peak current technique.

without inductor current accumulation. In other words, the proposed hysteresis mode operation and the new delta-voltage generator correct the current accumulation. Thus, the proposed SIMO DC-DC converter not only provides multiple output sources but also minimizes cross-regulation within 0.35%. Furthermore, owing to the load-dependant peak current technique, the SIMO DC-DC converter achieves high conversion efficiency from 80% at light load condition to 93% at heavy load condition in the experimental results.

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