InAs-Channel High-Electron-Mobility Transistors for Ultralow-Power Low Noise Amplifier Applications

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InAs-Channel High-Electron-Mobility Transistors for Ultralow-Power Low Noise Amplifier Applications

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An InAs-channel high-electron-mobility transistor (HEMT) with an 80 nm gate length for ultralow-power low-noise amplifier (LNA) applications has been fabricated and characterized on a 2-in. InP substrate. Small-signal *S*-parameter measurements performed on the InAs-channel HEMT at a low drain-source voltage of 0.2 V exhibited an excellent f_T of 120 GHz and an f_{max} of 157 GHz. At an extremely low level of dc power consumption of 1.2 mW, the device demonstrated an associated gain of 9.7 dB with a noise figure of less than 0.8 dB at 12 GHz. Such a device also demonstrated a higher associated gain and a lower noise figure than other InGaAs-channel HEMTs at extremely low dc power consumption. These results indicate the outstanding potential of InAs-channel HEMT technology for ultralow-power space-based radar, mobile millimeter-wave communications and handheld imager applications.

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1. Introduction

Recently, space-based radar, mobile millimeter-wave communications, and handheld imagers have attracted considerable attention. Such designs favor high-gain and low-power antennas, where prime power is limited. Moreover, a large signal-to-noise ratio for feature recognition is also an important characteristic for such systems.[1–3)]

Excellent RF performance has been demonstrated by InAlAs/InGaAs high-electron-mobility transistors (HEMTs) on InP substrates.[4)] Generally, higher electron mobility and velocity can be realized by increasing the indium content in the InGaAs channel, which makes InAs-channel heterostructure FETs (HFETs) very suitable for low-power and high-speed applications owing to their extremely high electron mobility of more than 30000 $cm^2/(V \cdot s)$.[5,6)]

The superior performance of InAs-channel HEMTs is primarily attributed to their high electron mobility, peak electron velocity, and high sheet carrier density under low bias conditions that result in unparalleled speed-power performance.[7–9)] As a result, while operating in the V_{DS} range below 0.5 V, InAs-Channel HEMT is capable of reducing dc power dissipation by an order of magnitude compared with equivalent GaAs pseudomorphic HEMTs and by a factor of 3–5 compared with equivalent GaAs metamorphic HEMTs.[10)] Furthermore, the high-gain and high frequency responses of InAs-channel HEMTs have made such technology the best candidate for ultralow power low noise applications at very high frequencies, such as space-based radar, mobile millimeter-wave communications, and handheld imager systems.

In this work, an 80-nm-gate-length InAs-channel/$In_{0.53}Ga_{0.47}As$ sub-channel HEMT for ultralow-dc-power and low noise application is presented. The excellent results clearly indicate the potential of such a device for ultralow-power circuits.

2. Material Growth and Device Fabrication

The schematic of the HEMT structure grown on a 2-in. semi-insulating InP substrate by molecular beam epitaxy (MBE) is shown in Fig. 1. The structure from bottom to top consisted of a 500-nm-thick $In_{0.52}Al_{0.48}As$ buffer layer, a 3-nm-thick $In_{0.53}Ga_{0.47}As$ lower sub-channel, a 5-nm-thick InAs channel layer, a 2-nm-thick $In_{0.53}Ga_{0.47}As$ upper sub-channel, a 3-nm-thick $In_{0.52}Al_{0.48}As$ spacer layer, a Si δ-doped (sheet density of 4×10^{12} cm^{-2}) layer, a 5-nm-thick $In_{0.52}Al_{0.48}As$ barrier, a 5-nm-thick InP etching stop layer, and a 40-nm-thick Si-doped $In_{0.53}Ga_{0.47}As$ cap (2×10^{19} cm^{-3}). By succinic-acid-based wet etching, room-temperature Hall mobility measurement showed a mobility of 9520 $cm^2\,V^{-1}\,s^{-1}$ with electronic sheet density of 2.44×10^{12} cm^{-2}.

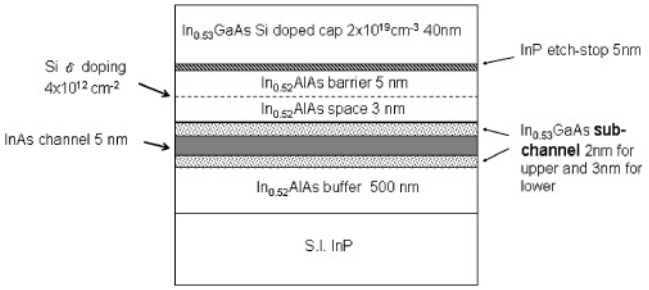

Fig. 1. Layer structure of an InAs-channel HEMT grown by MBE on semi-insulating 2-in.-diameter InP substrate.

High-indium-content devices typically suffer from a marked kink effect, low breakdown voltage, and high output transconductance caused by electron–hole pair generation. This phenomenon is even more marked for InAs/AlSb structures because of the lack of hole confinement due to type II alignment.[5)] In this study, a higher-energy-bandgap InAs/$In_{0.53}Ga_{0.47}As$ heterostructure was used to obtain a lower gate leakage current and a higher breakdown voltage resulting in better device performance.

The InP etching stop layer was used to improve the selectivity of wet chemical recess etching and provide semiconductor surface passivation on each side of the gate to reduce the trapping effect on the InAlAs surface.[11)] With the use of the InP etching stop layer, the lateral recess length was easy to control and RF performance was improved.[12)]

Mesa isolation was carried out by wet chemical etching. Source and drain ohmic metals were formed with 240-nm-

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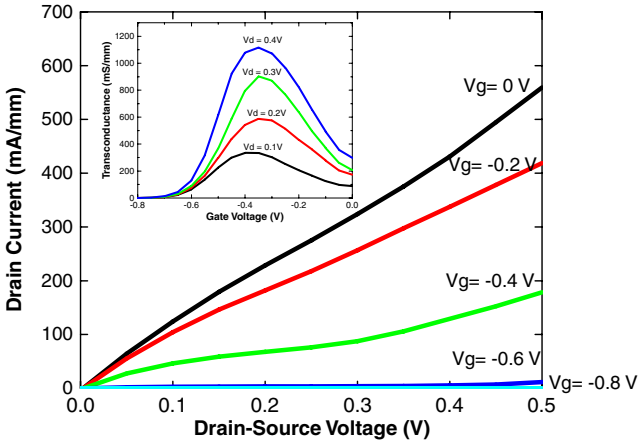

Fig. 2. (Color online) Current–voltage characteristics of 0.08 × 100 μm^2 InAs-channel HEMT.

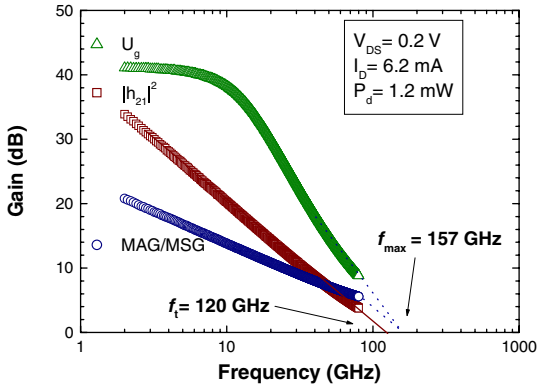

Fig. 4. (Color online) Typical current gain $|h_{21}|$, MAG/MSG and U_g as a function of frequency for a 0.08 × 100 μm^2 InAs-channel HEMT for ultralow-power operation. V_{DS} is 0.2 V and dc power is 1.2 mW.

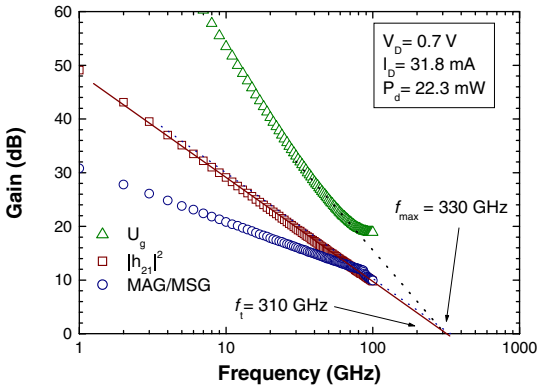

Fig. 3. (Color online) Typical current gain $|h_{21}|$, MAG/MSG and U_g as a function of frequency for a 0.08 × 100 μm^2 InAs-channel HEMT. V_{DS} is 0.7 V and the dc power is 22.3 mW.

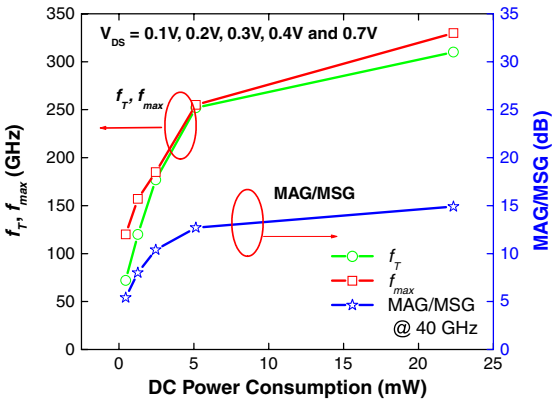

Fig. 5. (Color online) RF performance figures of merit as a function of dc power consumption for a 0.08 × 100 μm^2 InAs-channel HEMT.

thick Au/Ge/Ni/Au and alloyed by rapid thermal annealing at 250 °C for 30 s. As a result of the highly Si-doped cap, a low ohmic contact resistance (R_c) of 0.025 Ω·mm and an sheet resistance (R_{sh}) of 35.3 Ω/□ were obtained by the transmission line model method. T-shaped gate lithography was carried out in a 50 keV JEOL electron beam lithography system (E-beam). The gate recess was fabricated by wet chemical etching using succinic-acid-based solution. The Ti/Pt/Au gate metal was formed by evaporation and lift off. The gate length of 80 nm was estimated by scanning electron microscopy (SEM). Devices were passivated using a 100-nm-thick plasma-enhanced chemical vapor deposition (PECVD) silicon nitride film. Finally, the airbridges were formed with 2 μm plated Au.

3. Experimental Results and Discussion

The fabricated device exhibited good low-leakage output current–voltage (I–V) characteristics with an 80 nm gate length and a 2 × 50 μm^2 gate width, as indicated in Fig. 2. This device can be well pinched off with a threshold voltage of −0.7 V. Additionally, a relatively high drain current density of 430 mA/mm and a transconductance of 1120 mS/mm were observed at a low V_{DS} of 0.4 V, primarily due to the superior electron transport properties in the InAs channel.

The S-parameter of the 2 × 50 μm^2 device was measured using a Cascade Microtech™ on-wafer probing system with a vector network analyzer from 2 to 80 GHz. A standard load-reflection-reflection-match (LRRM) calibration method was used to calibrate the measurement system. Current gain ($|h_{21}|^2$), Mason's unilateral gain (U_g), and MAG/MSG as a function of frequency are plotted in Fig. 3. The intrinsic f_T and f_{max} of the 2 × 50 μm^2 device are 310 and 330 GHz at $V_{DS} = 0.7$ V, respectively. This same device exhibits a peak cutoff frequency f_T of 120 GHz and an f_{max} of 157 GHz at a drain voltage of 0.2 V with the corresponding dc power consumption as low as 1.2 mW as shown in Fig. 4. Such high-gain and high-frequency responses indicate the potential of the InA-channel HEMT for ultralow-power and high-frequency applications. Figure 5 shows the capability of the InAs-channel HEMT technology for low power applications and the f_T/f_{max} plot with the measured maximum available gain/maximum stable gain (MAG/MSG) at 40 GHz as a function of total dc power consumption. Note that the saturation in performance is observed at higher drain bias levels, possibly caused by the occurrence of impact ionization for small-energy-bandgap materials. The minimum noise figure and associated gain of the InAs-channel HEMT from 2 to 18 GHz at a V_{DS} of 0.2 V with a dc power dissipation of 1.2 mW are shown in Fig. 6. The device

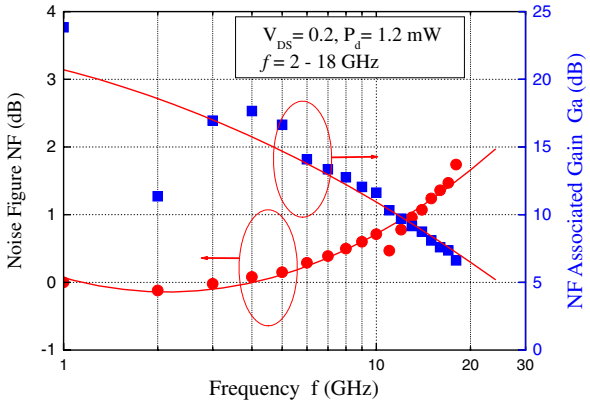

Fig. 6. (Color online) Measured minimum noise figure and associated gain of a 0.08 x 100 μm^2 InAs-channel HEMT from 2 to 18 GHz at V_{DS} of 0.2 V with a dc power dissipation of 1.2 mW.

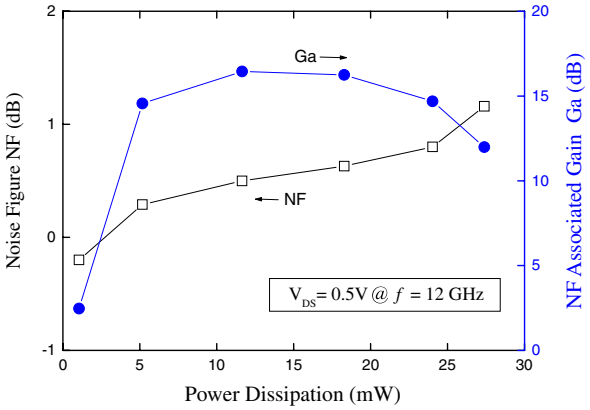

Fig. 7. (Color online) Measured minimum noise figure and associated gain of a 0.08 x 100 μm^2 InAs-channel HEMT at 12 GHz as a function of dc power consumption at a higher V_{DS} of 0.5 V.

demonstrated a typical associated gain of 9.7 dB with a noise figure of less than 0.8 dB at 12 GHz. The same device shows a higher gain of 14.7 dB and a lower minimum noise figure of 0.29 dB at 12 GHz when biased at a higher V_{DS} of 0.5 V as shown in Fig. 7. Operations at different low bias voltages with different total dc power dissipations are also shown in Fig. 8, where possible tradeoffs between the performance and the dc power consumption can be made depending on the applications.

4. Conclusions

In this study, a promising candidate for ultralow-power and high-frequency applications has been demonstrated. A high f_T of 120 GHz and an f_{max} of 157 GHz were obtained at a very low bias of 0.2 V V_{DS} and a low dc power consumption of 1.2 mW. At such a low bias, the device achieved a 9.7 dB associated gain and a noise figure of less than 0.8 dB at 12 GHz. With the high gain and low noise figure at an extremely low dc power consumption, the InAs-channel

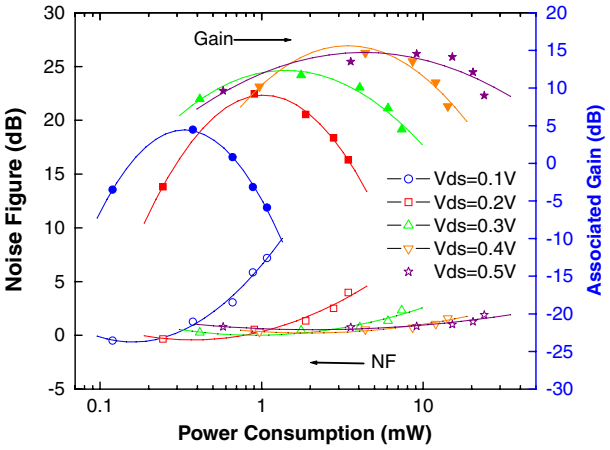

Fig. 8. (Color online) Measured minimum noise figures and associated gains of a 0.08 x 100 μm^2 InAs-channel HEMT at different V_{DS} from 0.1 to 0.5 V with different total dc power dissipations at 12 GHz.

HEMTs showed tremendous potential for low-power and low-noise applications.

Acknowledgements

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