Brief Papers

A Floating Well Method for Exact Capacitance-Voltage Measurement of Nano Technology

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***Abstract*—Small gate area with short gate length reduces the C–V distortion of ultrathin oxide devices, but results in high parasitic capacitance/total capacitance ratio. The floating well method can exclude the parasitic capacitance to obtain accurate inversion oxide thickness without using any dummy pattern. It is suitable for nano technology.**

***Index Terms*—Capacitance-voltage, electrical oxide thickness, floating well, nano technology, ultrathin oxide.**

I. Introduction

In nano technology, the oxide thickness is scaled down to meet the performance requirements [1]. The capacitance-voltage (C–V) curve of ultra-thin oxide is distorted due to large gate leakage current [2]. The distortion of high-frequency C–V curve of ultra-thin oxide has been characterized by circuit approach by considering the gate leakage current and channel resistance [3]–[6]. The smaller pattern area (25 μm^2) with lower channel resistance is used in this paper to minimize the high frequency C–V distortion. Hence, since the bonding pad area is restricted by bonding and probing technology, the parasitic capacitance C_P contributed by bonding pad can not be reduced with the capacitance of test pattern. Hence, larger EOT extraction error can be induced by parasitic capacitance when smaller pattern area is employed. In this paper, a C–V measurement method with floating well proposed this paper enables to measure the gate-to-channel capacitance C_{GC} between source-drain and gate electrode in order to suppress the offset capacitance when measured the gate-to-body capacitance C_{GB}. The accurate EOT of nano technology can be extracted by inversion capacitance measured with floating well method without any dummy pattern.

II. Experiments

The devices used in this study are polysilicon-gate MOS capacitors with cobalt salicide process. All C–V measurements are carried out with HP 4284 LCR meter. The signal frequency and level are 1 MHz and 30 mV, respectively. Oxide with thickness varying from 2 to 1.4 nm is used to show the thickness dependence of C–V distortion phenomenon. The MOS device areas varying from 400 to 25 μm^2 are used to study the area dependence of C–V distortion phenomenon and the impact of parasitic capacitance. The C–V measurements of both floating well and grounded well methods are used in this paper to extract the parasitic capacitance without using any calibration pattern.

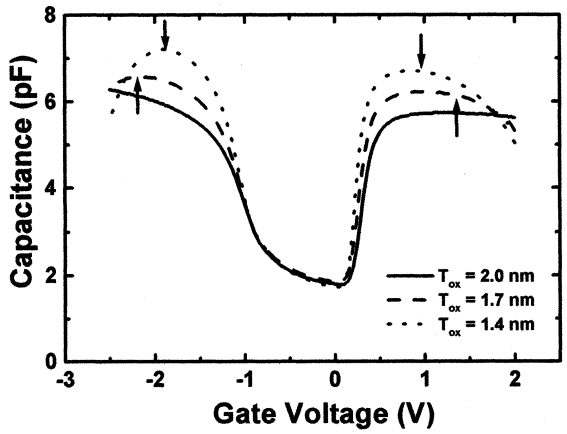

Fig. 1. Oxide thickness dependence of device C–V curves. Arrows indicate the occurrence of C–V distortion, i.e., $V_G > 1.3$ V or $V_G < -2.2$ V for $T_{OX} = 1.7$ nm; $V_G > 0.9$ V or $V_G < -1.8$ V for $T_{OX} = 1.4$ nm.

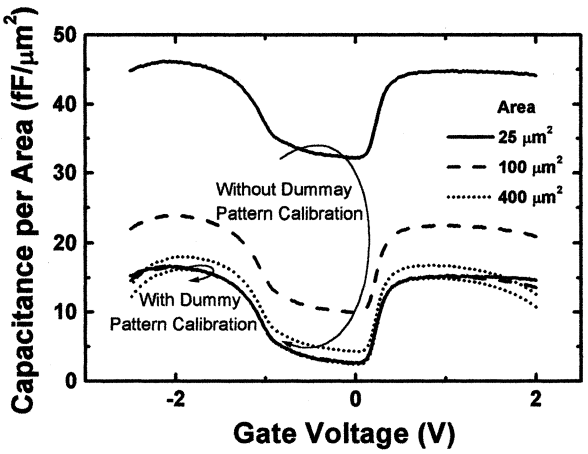

Fig. 2. Pattern area dependence of device C–V curves with and without dummy pattern calibration.

III. Results and Discussion

The oxide thickness dependence of device C–V curves of capacitors with 400 μm^2 area are shown in Fig. 1. No C–V distortion is found in C–V curve of capacitors with 2 nm oxide thickness. Distortion occurs when oxide thickness is scaled down, as observed in Fig. 1. Hence, the electrical oxide thickness (EOT) can not be extracted from the C–V curve accurately when oxides are very thin. The root cause of C–V curve distortion of ultrathin oxide is the large gate leakage current and series resistance [3]–[6]. The pattern area dependence device C–V curves with 1.4 nm oxide thickness are shown in Fig. 2. Two parallel capacitors contribute to the measured capacitance value. One is test pattern that consists of gate-to-channel capacitor C_{GC}, the other is parasitic capacitor C_P contributed by bonding pad and inter-connection metal line. In traditional C–V test, the dc bias and small ac

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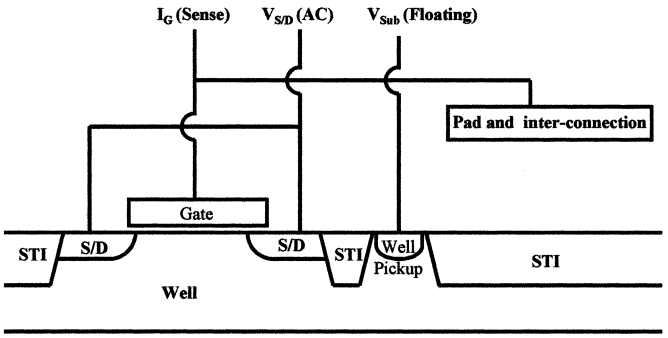

Fig. 3. Schematic illustration of the C–V measurement with floating well method.

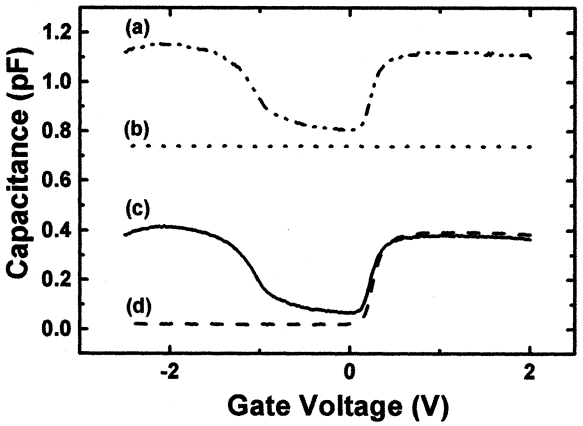

Fig. 4. C–V curves comparison between traditional method with dummy pattern calibration and floating well method. Curve (a) ($-\cdot\cdot-\cdot\cdot$) is C–V curve measured by traditional method without dummy pattern calibration. Curve (b) ($\cdot\cdot\cdot\cdot\cdot\cdot$) is C–V curve of dummy pattern. Curve (c) (——) is C–V curve measured by traditional method with dummy pattern calibration. Curve (d) (- - -) is C–V curve measured by floating well method without dummy pattern calibration.

signal are applied to source, drain, and well. The small signal is produced and extracted in polysilicon-gate, inter-connection metal line and bonding pad during C–V measurement. Thus, the gate-to-body capacitance C_{GB} measured by traditional method is the sum of C_{GC} and C_P. C_{GC} is proportional to the area of polysilicon-gate MOS capacitor (A_{MOS}). Hence, C_{GC}/A_{MOS} is independent of A_{MOS}. When interconnect and bonding pad layouts are fixed, C_P is constant. Hence, C_P/A_{MOS} increases with decreasing A_{MOS}, and the total capacitance per area (C_{GB}/A_{MOS}) increases with decreasing A_{MOS} (Fig. 2). The capacitance of dummy pattern C_D that consists of parasitic capacitors only is measured and used for calibration. C_D equals to C_P. Thus, C_{GC} can be obtained by subtracting C_D from C_{GB}. Device C–V curve calibrated with dummy capacitance, i.e., C_{GB}–C_D, is also shown in Fig. 2 where smaller C–V distortion for capacitors with smaller areas is observed, presumably due to the lower gate and channel resistance. Hence, it is desirable to minimize the C–V test pattern to reduce the gate and channel resistance. The pattern area of the polysilicon-gate MOS capacitor needs to be shrunk when technology progresses due to C–V distortion by increasing gate tunneling current with scaled oxide thickness. But the area of parasitic capacitors, i.e., the bonding pad and inter-connect routing area, can not be decreased as much as that of the polysilicon-gate MOS capacitors. The parasitic capacitance/total capacitance ratio will increase with the scaling down of oxide thickness. Hence, parasitic capacitance compensation becomes more important for exact C–V measurement of nano technology.

The schematic illustration of C–V measurement with floating well method is shown in Fig. 3. In floating well method, the dc bias and small ac signal are only applied to source and drain, the well is floating during C–V test. When poly-silicon gate MOS device operates at inversion mode, the dc bias and ac signal is not only applied to source and drain regions but also propagates into channel region through inversion layer. Hence, the gate-to-channel capacitance C_{GC} of polysilicon-gate MOS capacitor measured by floating well method is the same as that measured by traditional method. Since no ac signal is applied to well during C–V test, and no ac signal produced in inter-connection metal line and bonding pad with well floating. The parasitic capacitance when measuring the gate to body capacitance C_{GB} is negligible in C–V measurement with the floating well method proposed in this study. The inversion capacitance of 1.4 nm oxide with 25 μm^2 area measured by floating well method is the same as that measured by traditional method with dummy pattern calibration as shown in Fig. 4. When poly-silicon gate MOS device operates at accumulation mode, the dc bias and ac signal are only applied to source and drain and can not propagate into channel region. Thus, only the capacitance of source-drain and gate overlap regions is measured in C–V measurement by floating well method. Thus, the accumulation capacitance is not measured by floating well method as shown in Fig. 4. But the parasitic capacitance C_P can be extracted by subtracting the inversion capacitance C_{GC} measured by floating well method from the inversion capacitance C_{GB} measured by traditional method. Thus, the exact C–V curve can be deduced by parasitic capacitance compensation without any dummy pattern calibration by combining both floating and conventional methods.

IV. Conclusion

The C–V distortion becomes more severe when gate oxide is thinner. While the C–V curve distortion can be minimized by pattern area reduction. The parasitic capacitance/total capacitance ratio increases with decreasing pattern area. The parasitic capacitance can be neglected with floating well method. Exact inversion C–V curve can be measured by floating well method without any dummy pattern calibration for capacitors with 1.4 nm oxide thickness. Hence, the accurate EOT of nano technology can be extracted by inversion capacitance measured with floating well method. Correct C–V curves can be deduced by parasitic capacitance compensation without using calibration patterns by combining both floating well and conventional methods.

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