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# Growth of High-Quality Ge Epitaxial Layers on Si (100)

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A method of growing high-quality epitaxial Ge layers on a Si(100) substrate is reported. In this method, a 0.8 μm $Si_{0.1}Ge_{0.9}$ layer was first grown. Due to the large lattice mismatch between this layer and the Si substrate, many dislocations form near the interface and in the lower part of the $Si_{0.1}Ge_{0.9}$ layer. A 0.8 μm $Si_{0.05}Ge_{0.95}$ layer and a 1.0 μm top Ge layer were subsequently grown on the $Si_{0.1}Ge_{0.9}$ layer. The formed interfaces of $Si_{0.05}Ge_{0.95}/Si_{0.1}Ge_{0.9}$ and $Ge/Si_{0.05}Ge_{0.95}$ can bend and terminate the upward-propagated dislocations very effectively. The *in situ* annealing process was also performed for each individual layer. Experimental results show that the dislocation density in the top Ge layer can be greatly reduced, and the surface is very smooth, while the total thickness of the structure is only 2.6 μm. [DOI: 10.1143/JJAP.42.L517]

KEYWORDS: Ge, SiGe, UHV/CVD, dislocation, heterostructure, TEM

Heterostructures of SiGe and Ge epitaxial layers on Si substrates have attracted considerable attention due to their potential device applications and compatibility with Si-based technology. In particular, strain-relaxed SiGe and Ge layers provide a virtual substrate for the growth of high-electron-mobility structures[1,2] and for the integration of III-V devices on Si.[3] In addition, the integration of Ge with Si is of much importance for the application of Ge photo-detectors.[4] The major problems of these relaxed layers are the high density of threading dislocations and the high surface roughness arising from the 4.2% lattice mismatch between Ge and Si. Various growth techniques and treatments have been developed to solve these problems. It has been reported that the compositionally graded buffer (CGB) layers,[5] low-temperature Si buffer layers,[6] compliant silicon-on-insulator (SOI) substrate,[7] two-step procedure,[8] and selective area growth combined with thermal cycle annealing[9] can be used to grow high-quality strain-relaxed SiGe and Ge layers. Among them, the CGB layers are the most practically and widely used ones today. However, the CGB layers still have two major challenges. First, these CGB layers often suffer from a thickness of approximately 10 μm with a Ge composition ranging from zero to 1.0, which makes the integration of devices on the Si-based circuits difficult. Second, the CGB layers often exhibit a cross-hatch pattern, which makes the surfaces very rough.[10]

In this letter, we report an alternative approach to obtaining a high-quality Ge layer. The total thickness of all epitaxial layers is only 2.6 μm. The threading dislocation density in the top Ge layer can be reduced to approximately $3 \times 10^6$ cm$^{-2}$. The Ge surface roughness is only 32 Å. The procedure mainly involves growing three epitaxial layers (see Fig. 1). The first layer is the $Si_{0.1}Ge_{0.9}$ layer, the second is the $Si_{0.05}Ge_{0.95}$ layer, and the third is the Ge layer. After the growth of each individual layer, *in situ* 750°C annealing for 15 min was performed. Due to the large lattice mismatch at the interface between $Si_{0.1}Ge_{0.9}$ and Si layers, many close small islands are formed during growth at low temperatures. As growth proceeded, these islands quickly coalesced into a continuous film.[11] At the same time, many dislocations generated and interacted with each other to form closed nonpropagating loops and networks near the interface. A small portion of the dislocations that did not have the chance to pair up continued to propagate upward. A similar technique has been widely used in growing highly mismatched heterostructures, for example, GaN on Sapphire.[12] Due to the proper lattice mismatch strains at the upper interfaces of $Si_{0.05}Ge_{0.95}/Si_{0.1}Ge_{0.9}$ and $Ge/Si_{0.05}Ge_{0.95}$, the upward-propagated dislocations can be bent sideward and terminated effectively. Details of the behavior of dislocations at the mismatched interfaces can be seen in refs. 13 and 14. Additionally, the thermal annealing process, which was performed after growing each individual layer, can further reduce dislocation density in the epitaxial layers. The mechanism of threading dislocation reduction employed in this work is shown schematically in Fig. 1.

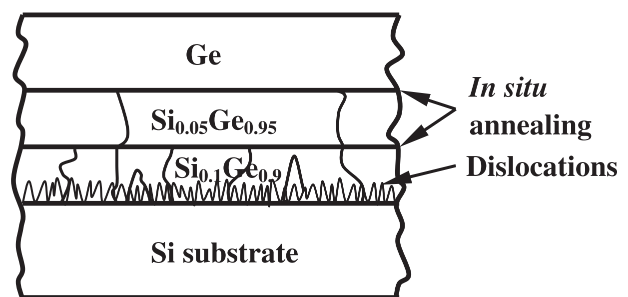


Fig. 1. Mechanism of reducing threading dislocations.

Growth of SiGe and Ge layers was carried out using an ultra-high vacuum chemical vapor deposition (UHV/CVD) system with a base pressure of less than $2 \times 10^{-8}$ Torr.[15] First, a 4-inch Si(100) substrate wafer was cleaned by 10% HF dipping and high-temperature baking at 800°C in the growth chamber for 5 min. Then, a 0.8 μm $Si_{0.1}Ge_{0.9}$, a 0.8 μm $Si_{0.05}Ge_{0.95}$, and a 1.0 μm Ge layer were grown at 400°C in sequence. Between successive layers, growth was interrupted for an *in situ* 15 min 750°C annealing. Transmission electron microscopy (TEM) was used to observe the thickness of the epitaxial layers and the dislocation distribution, and to estimate the threading dislocation density. The Ge surface morphology was analyzed by Nanoscope III atomic force microscopy (AFM) in the

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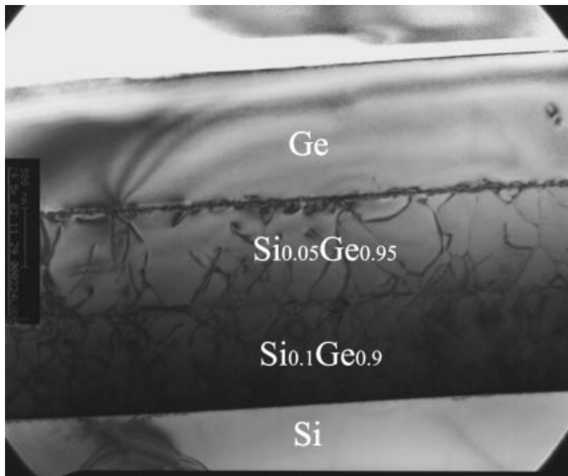


Fig. 2. Cross-sectional TEM image of the epitaxial structure.

contact mode.

Figure 2 shows the cross-sectional TEM image of the sample. There are a large number of dislocations located near the $Si_{0.1}Ge_{0.9}$/Si interface and at the lower part of the $Si_{0.1}Ge_{0.9}$ layer. The upward propagated dislocations are bent sideward and terminated very effectively by the $Si_{0.05}Ge_{0.95}$/$Si_{0.1}Ge_{0.9}$ and Ge/$Si_{0.05}Ge_{0.95}$ interfaces. Almost no threading dislocation can propagate into the top Ge layer. The image shows that the total thickness of the three epitaxial layers is only approximately 2.6 μm, which is much smaller than that of CGB layers reported earlier. In this study, the Ge composition variation at the two strained interfaces is set at 0.05. We found that if the Ge composition variation is larger than 0.05, new dislocations will generate from the interfaces due to the relatively large lattice mismatch. On the contrary, if the Ge composition variation is less than 0.05, the mismatch strain formed at the interfaces is too small to terminate the dislocations effectively. The thickness of each SiGe layer in the sample may not be optimum. Further experiments are required to investigate the effects of changing the thickness.

A plan-view TEM image of the sample surface is shown in Fig. 3. There is no dislocation in this image. By analyzing several plan-view TEM images, the threading dislocation density is estimated to be about $3 \times 10^6$ cm$^{-2}$.

Fig. 3. Plan-view TEM image of the top Ge layer.

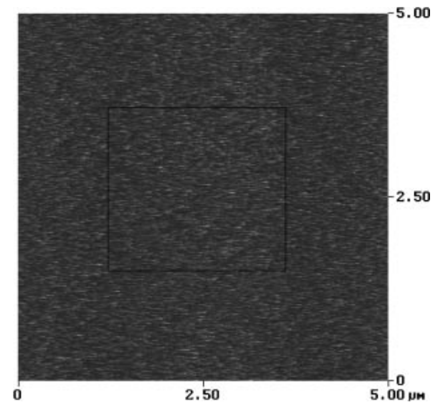


Fig. 4. AFM image of the surface of the top Ge layer.

The surface roughness was measured by AFM (see Fig. 4). No cross-hatch pattern was observed. The root mean square (RMS) of the surface is only 32 Å, which is also much smaller than that of the CGB layers reported earlier. This smooth surface is useful for fabrication of devices and growth of III-V materials.

In summary, we have designed a method of growing high-quality Ge epitaxial layers on a Si substrate. The method mainly involves: (1) growth of three layers consisting of a 0.8 μm $Si_{0.1}Ge_{0.9}$ layer, a 0.8 μm $Si_{0.05}Ge_{0.95}$ layer, and a 1.0 μm top Ge layer, and (2) *in situ* 750°C annealing for 15 min performed on each individual layer. By this procedure, many dislocations were formed at the $Si_{0.1}Ge_{0.9}$/Si interface and at the lower part of the $Si_{0.1}Ge_{0.9}$ layer. Moreover, the upward propagated dislocations can be bent and terminated effectively by the interfaces of $Si_{0.05}Ge_{0.95}$/$Si_{0.1}Ge_{0.9}$ and Ge/$Si_{0.05}Ge_{0.95}$. The top Ge layer exhibits a low threading dislocation density and a smooth surface, while the total thickness of the epitaxial structure is relatively small. It is shown that this method is very practical for growing of high-quality Ge epitaxial layers on Si substrates.

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