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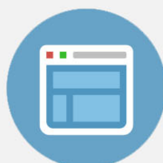
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Metal drift induced electrical instability of porous low dielectric constant film

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Nano-porous carbon doped oxide (CDO) is one of the potential low dielectric constant (low-*k*) materials that can achieve a dielectric constant as low as 2.2 and is expected to be suitable for the next generation multilevel interconnection. However, the electrical stability of CDO in contact with metal has not been addressed. In this work, metal ions' drift into nano-porous CDO is investigated. It is observed that both the Al and Cu ions can be driven into porous CDO film easily by applying electric field or thermal treatment. This results in a severe flat band voltage shift of the metal/CDO/Si capacitor structure. It is hypothesized that the lacking formation of self-limited aluminum oxide between Al and CDO film make Al ions drift into CDO. The adhesion of Al and Cu to CDO is also very poor. A physical model, combining weak dielectric polarization and metal ions drift, was proposed to explain the observed electrical instability. The inconsistent results regarding the Al/porous low-*k*/Si structure reported in the previous literatures can also be explained with this proposed model. Fortunately, TaN, as a common diffusion barrier material for Cu interconnect structure, is proved to have good adhesion to CDO. Negligible metal ions would drift in CDO during electrical stress. It is concluded that with a suitable diffusion barrier, such as TaN, CDO is still a very promising material for next generation Cu-interconnect technology. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1563292]

INTRODUCTION

As in ultra-large scale integrated circuits generations, the implementation of copper-interconnect structures with low-*k* materials is the only solution to reduce overall signal delay in several technology nodes in the future.[1,2] Since Cu is the metal with the second lowest resistivity, adopting lower dielectric constant materials is the only method to further improve the resistance-capacitance time delay. According to the *International Technology Roadmap for Semiconductor* published in 2001, the bulk dielectric constant of low-*k* material must be reduced to lower than 2.4 by 2006.[3] In the past 10 years, lots of varieties of low-*k* materials are being developed with different chemical composition. By changing film polarity, changing chemical bonds, or inserting lower weighted molecular atoms, one can intrinsically reduce the *k* value to about 2.7.[4] In order to further reduce dielectric constant, there is an unavoidable trend of developing porous type low-*k* films. With the free air volume pore structures in bulk low-*k* film, a very low dielectric constant could be reached.[5–8]

Among the nano-porous low-*k* materials, nano-porous carbon-doped oxide (CDO) is one of the most promising porous low-*k* materials to date.[9–12] CDO could be deposited in a plasma-enhanced chemical vapor deposition (PECVD) system with additional curing process to produce a stable state. A very low dielectric constant of 2.2 has been achieved. It is reported that CDO exhibits a very low leakage current (<1 nA/cm^2 at 2.5 MV/cm), a very high thermal stability ($>600\,^\circ$C in N_2 ambient), and strong electrical strength (>5 MV/cm at $200\,^\circ$C). It has been demonstrated successfully integrating with Cu in a full dual damascene structure.[13] The above information indicates that CDO is a very potential material for next generation intermetal dielectric (IMD).[14] But, not many electrical properties have been discussed in previous literatures.

On the other hand, Cu shows many advantages in comparison with Al[15] but also new problems appear. The drift of Cu ions into IMD is one of the most important issues that should be carefully studied. Cu mobile ions in IMD would always induce defect traps and cause reliability issues and even degrade lifetime of the devices. To understand the Cu drift in IMD is meaningful for not only academic interest but also practical application. A bias temperature stress (BTS) test on a Cu/Low-*k* film/Si sandwiched capacitor structure is always employed to study Cu drift behavior in low-*k* thin

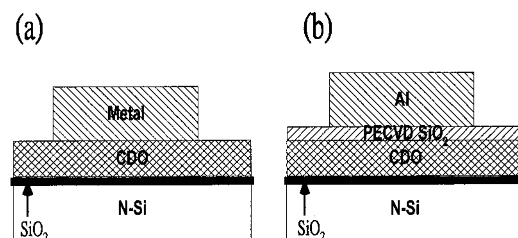

FIG. 1. Schematic drawing of the MIS structures used in this work: (a) Metal-MIS (Al-MIS, Cu-MIS and TaN-MIS): Metal/CDO(200 nm)/SiO_2(10 nm)/Si. (b) Al-MIS-2: Al/PECVD SiO_2(30 nm)/CDO(200 nm)/SiO_2(10 nm)/Si.

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TABLE I. Flat band voltage shift of MIS structures with various metal gate materials after BTS test at 0.6 MV/cm for 30 min.

Temperature (°C)	Al (V)	Cu (V)	TaN (V)	Al-MIS-2 (V)
30 °C	−7.48	−3.2	−2.74	−0.07
150 °C	<−40	∼−40	−9.6	−5.12

film. Aluminum, being a very stable interconnection metal, was used as a reference to distinguish Cu drift and the other issues. Recently, some unusual phenomenon happened to these recently developed porous low-*k* materials. Al gated capacitor structures exhibit an unaccustomed V_{fb} shift after positive electric-field stress. Quite different explanations were proposed in those literatures.[16–18] All of these proposed models: interface-related charges, instabilities occurred when Al came in contact with low-*k* film, charges injects and trapped inside low-*k* film, and Al ions drift in low-*k*, are not consistent with each other. Besides, all these models were proposed on the basis of electrical analysis data without any material analysis evidences.

The significance of studying metal drift in low-*k* material is manifold. At first, integration scheme is dependent on metal drift in low-*k* material. Second, interconnect reliability is strongly affected by metal ions in low-*k* dielectric. Third, to monitor Cu contamination, metal drift behavior must be known in advance. Therefore, we investigated the drift of metal ions in a nano-porous low-*k* film and studied the metal ions induced electrical instability in this work. A metal ions drift model in porous CDO is also proposed.

EXPERIMENTAL PROCEDURE

A simple metal-insulator-silicon (MIS) capacitor structure was used in this work. The starting material was (100)-oriented *n*-type silicon wafer. A 10 nm thick oxide was thermally grown before CDO deposition to minimize the insulator/silicon interface state density. CDO film was deposited in a plasma-enhanced chemical vapor deposition (PECVD) system using Trikon Technologies Planar 300 PECVD system named Orion™. The total thickness of CDO is 200 nm. Various metals, Al, Cu, and TaN were deposited through a metal mask to form gate electrodes. Samples are referred as Al-MIS, Cu-MIS, and TaN-MIS. Al was deposited in a thermal evaporation system while Cu and TaN were deposited in a sputtering deposition system. The structure of the MIS capacitor is then formed metal/CDO(200 nm)/SiO_2(10 nm)/Si. A thin Si_3N_4 layer of 30 nm thickness was deposited to passivate the MIS structure. Al deposition at backside and 400 °C annealing in N_2 ambient for 30 min were performed before electrical measurement. Some Al-gate capacitors (referred to as Al-MIS-2 sample) with a 30 nm thick PECVD oxide on CDO were also fabricated. Figure 1 shows the schematic drawings of the two sample structures. Unpatterned metal/CDO/SiO_2/Si and Al/SiO_2/Si structures were also prepared for nonelectrical analysis.

Capacitance-voltage ($C-V$) electrical measurements were performed to evaluate the CDO film stability using a

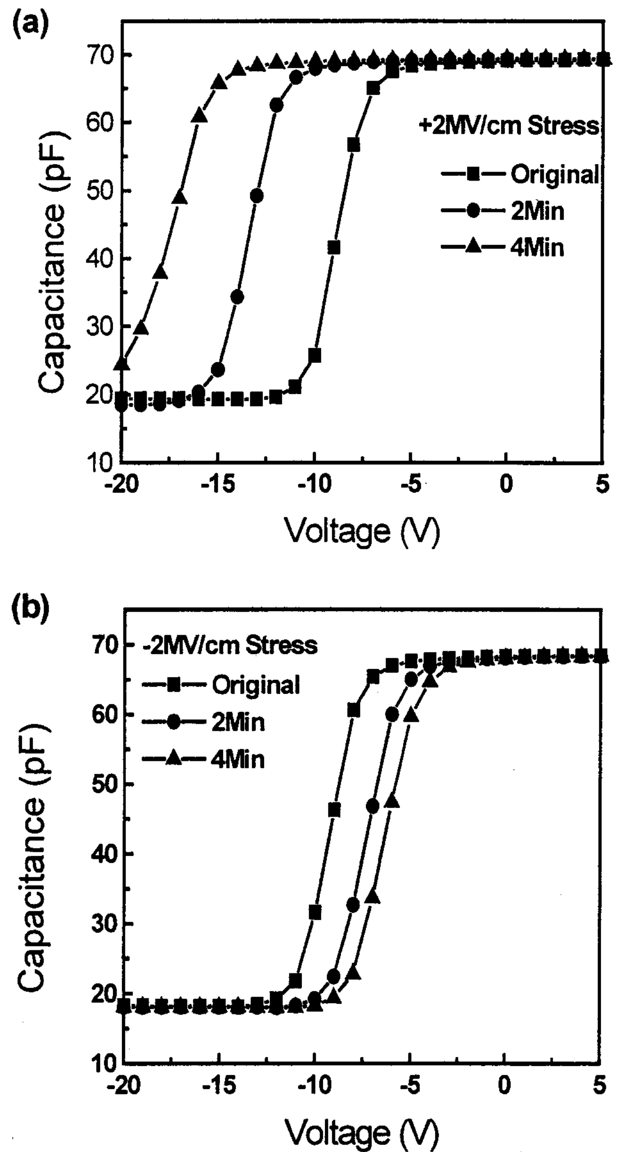

FIG. 3. Capacitance-voltage curves of Al-MIS samples after electrical stress at (a) +2 MV/cm and (b) −2 MV/cm for various time periods at room temperature.

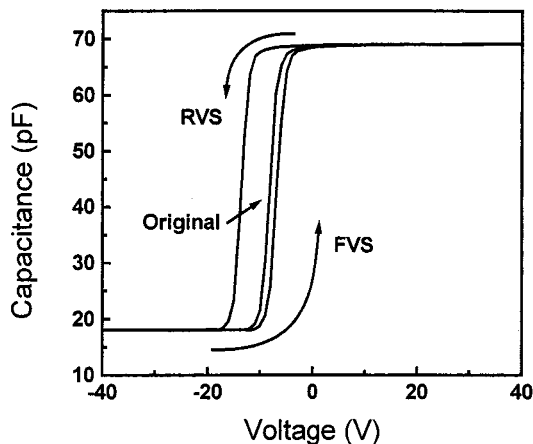

FIG. 2. Capacitance-voltage curves of Al-MIS sample measured from inversion mode to accumulation mode (FVS) and from accumulation mode to inversion mode (RVS).

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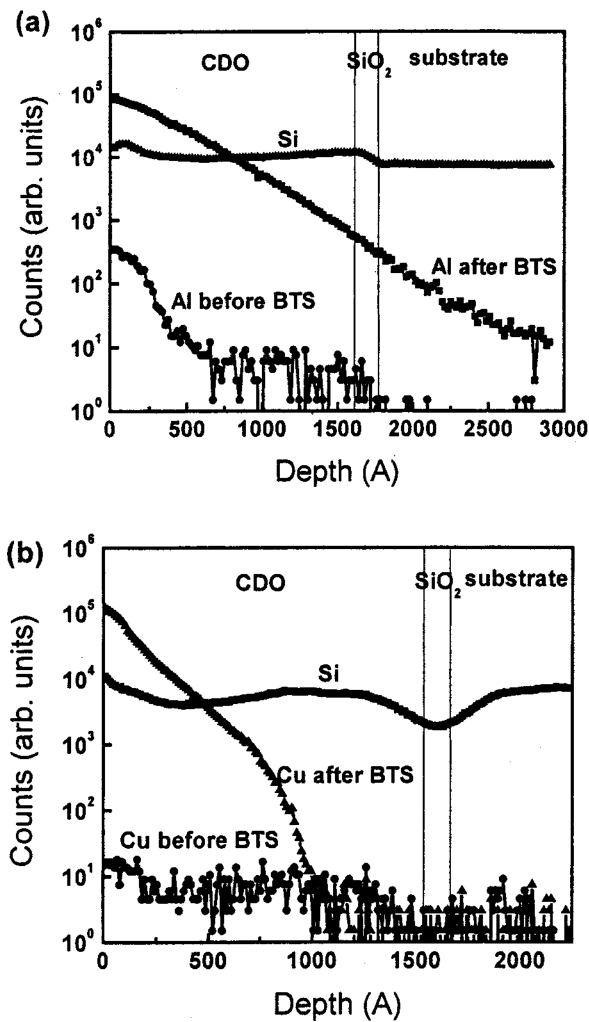

FIG. 4. SIMS depth profiles of (a) Al-MIS sample and (b) Cu-MIS sample before and after the BTS test at +1 MV/cm and 200 °C for 60 min.

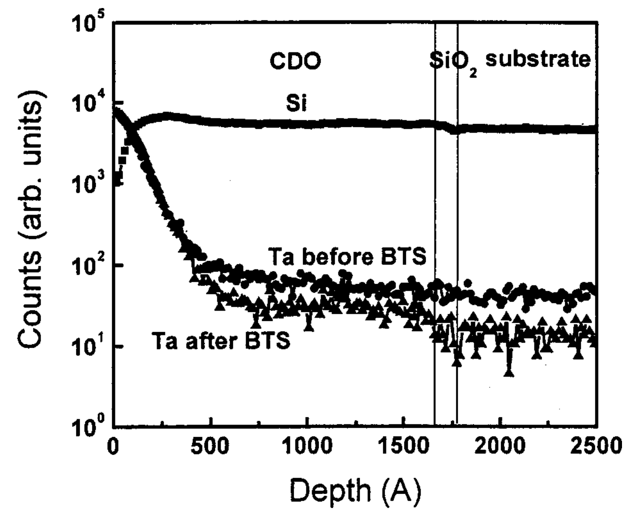

FIG. 5. SIMS depth profiles of TaN-MIS sample before and after the BTS test at +1 MV/cm and 200 °C for 60 min.

precision impedance meter of model Agilent 4284A. A bias-temperature stress test on MIS samples was performed at various temperatures and electric fields to evaluate the behavior of metal ion drift in CDO film. Flat band voltages before and after BTS were extracted from high frequency (100 KHz) $C-V$ characteristic with voltage sweep either from inversion mode to accumulation mode (forward voltage sweep, FVS) or from accumulation mode to inversion mode (reverse voltage sweep, RVS). Secondary ion mass spectroscopy (SIMS) analysis was performed on MIS capacitors before and after the BTS test to determine the depth distribution of metal in CDO film.

RESULT AND DISCUSSION

Table I summarizes the value of V_{fb} shift of Al-MIS, Cu-MIS, and TaN-MIS samples after the BTS test at 0.6 MV/cm for 30 min. The magnitudes of V_{fb} shift of the MIS capacitors are Al-MIS, Cu-MIS, and TaN-MIS in the sequence from high to low. The lowest V_{fb} shift of TaN-MIS sample is as expected because TaN is stable and acts as very good diffusion barrier of metals. The negative V_{fb} shift of the Cu-MIS sample is always explained by Cu drift in dielectric. What is unexpected is that the magnitude of the V_{fb} shift of Al-MIS sample is larger than that of the Cu-MIS sample.

By repeating the $C-V$ measurement on the Al-MIS capacitor from inversion mode to accumulation mode (FVS) and then from accumulation mode to inversion mode (RVS), the $C-V$ shift with respect to the original $C-V$ curve was found. As shown in Fig. 2, the $C-V$ curve shifts toward the right-hand side under FVS, while it shifts toward the left-hand side under RVS. The shifts under FVS and RVS are asymmetric and a net left shift was observed. Figures 3(a) and 3(b) show the $C-V$ curves of the Al-MIS sample after continuous electrical stress at +2 and −2 MV/cm, respectively. It is was also found that the magnitude of the V_{fb} shift under positive electric-field stress is larger than that under negative electric-field stress. Because of the asymmetric shift, the $C-V$ instability cannot be simply explained with the dielectric polarization[19] and further investigations were made to find out the root cause of instability.

It is well known that Al is quite stable in contacting with SiO_2 because a very thin self-limiting Al_2O_3 forms between Al and SiO_2 and acts as a good diffusion barrier.[16–17] The negligible V_{fb} shift of the Al-MIS-2 sample at 30 °C indicates that CDO itself is electrically stable at room temperature. Therefore, the −7.48 V V_{fb} shift of the Al-MIS sample implies that Al ions can be driven into CDO at room temperature. It is well known that Al ions do not enter SiO_2 under the BTS test; the V_{fb} shift of Al-MIS-2 capacitor after BTS at 150 °C would be attributed to the intrinsic instability of CDO, i.e., dielectric polarization.[19] But as Al contacts with the CDO film directly, the V_{fb} shift is well beyond −40 V (see Table I). The magnitude of the V_{fb} shift of the Al-MIS

TABLE II. Results of pull-stud adhesion test of different metal/CDO interface and Al/SiO_2 interface.

	Al/CDO	Cu/CDO	TaN/CDO	Al/SiO_2
Average (MPa)	16.82	19.1	51.92	47.02
Standard deviation (MPa)	5.62	9.53	11.46	7.37

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TABLE III. Flat band voltage shift of Al-MIS sample after annealing at 400 °C for various time periods.

CDO	0 h	2 h	8 h
Average (V)	−1.59	−2.73	−3.52
Standard deviation (V)	0.24	0.31	0.33

sample excludes the CDO instability effect [V_{fb}(Al-MIS) subtracts V_{fb}(Al-MIS-2)] is still very large, and thus the possible cause of this severe instability might be Al ions drifting into CDO film. Figure 4(a) compares the distribution of Al atoms in CDO before and after the BTS test at 150 °C. It is apparent that Al ions were driven throughout the whole CDO. Figure 4(b) shows that, similar to Al, Cu can be easily driven into CDO with the same BTS test. It is well known that Cu is a fast diffuser in most of the dielectric materials. This observation confirms that the V_{fb} shift of the Cu-MIS sample is due to Cu drift.

TaN is known to be inert in comparison with Al and Cu and is used as a barrier metal between metal interconnect and dielectric thin film. It is not expected to inject ions into dielectric electrical stress. The Ta profiles of the TaN-MIS sample are almost identical before and after BTS at 150 °C as shown in Fig. 5. This result implies that the V_{fb} shift of the TaN-MIS capacitor listed in Table I is not due to metal ions. Actually, a slight distortion of $C-V$ curve was observed on the BTS tested TaN-MIS sample. The slightly larger V_{fb} shift of the TaN-MIS sample than that of the Al-MIS-2 sample is thus attributed to the dielectric polarization together with process damage during TaN deposition.

The apparent Al diffusion into CDO implies the lack of Al_2O_3 formation at the Al/CDO interface.[16–17] Table II lists the results of pull-stud adhesion test of different metal/CDO and Al/SiO_2 interfaces. As expected, Al shows good adhesion to oxide dielectric thin film, while both Al and Cu show very poor adhesion to CDO. The poor adhesion between Al and CDO is another side evidence that no interfacial reaction

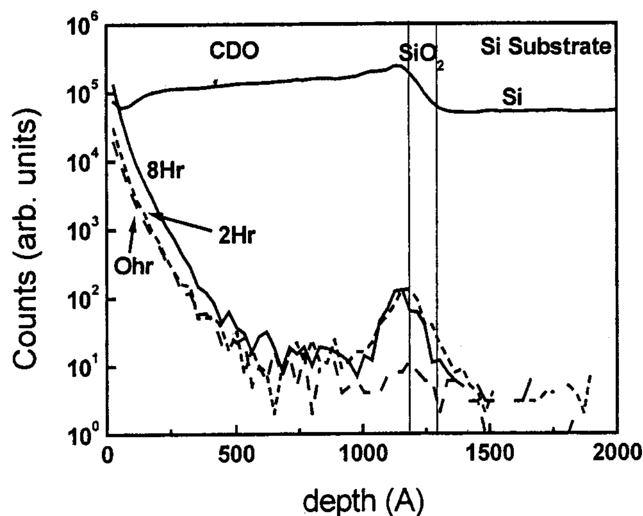

FIG. 6. SIMS depth profiles of Al-MIS samples after annealing at 400 °C for various time periods.

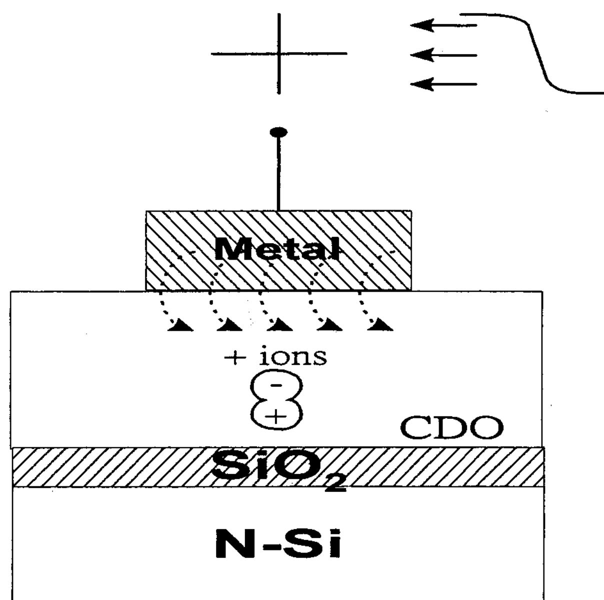

FIG. 7. Schematic illustration of the proposed model to explain the electrical instability of Metal/CDO system.

between Al and CDO occurs. Fortunately, TaN, as a common diffusion barrier material for Cu, is proved to have good adhesion to CDO.

The lacking formation of self-limited aluminum oxide between Al and CDO film allow Al ions to be driven into CDO film. Besides, the porous structure of CDO film contains nano-pores. Al ions can easily be driven into a deep portion of CDO along with these pores. Table III lists the V_{fb} values of just fabricated Al-MIS samples after annealing in N_2 ambient at 400 °C for various time periods. The V_{fb} shifts toward negative voltage with the increase of annealing time. This result means that more Al ions diffuse into CDO film under long-time thermal anneal. Figure 6 shows the Al depth profile of Al-MIS sample after annealing. The Al metal gate had been removed before SIMS analysis. It is confirmed that Al atoms did diffuse into CDO film after 8 h annealing. Besides, Al atoms piled up at CDO/SiO_2 interface and cannot diffuse though the SiO_2 layer. This phenomenon is consistent with our hypothesis that the lacking of alumni oxide layer between Al and CDO leads to the drift and/or diffusion of Al into CDO.

Now the electrical instability of the metal/CDO/Si structure can be understood with the model proposed in Fig. 7. Weak polarization occurs under electric field at high-temperature stress for all Metal-MIS capacitor and this is what we have named as CDO intrinsic instability that causes V_{fb} to shift left. As the gate is positively biased, some kinds of metal ions (Al or Cu) may be driven from the gate into CDO and move quickly along nano-pore structures into deeper bulk dielectric. This phenomenon would cause metal/CDO/Si structure to be electrically unstable.

CONCLUSIONS

Our investigation discovered that the lacking formation of Al_2O_3 interfacial layer caused Al ions to migrate into

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CDO film and the CDO porous structure would enhance metal ions movement in it. An electrical instability model combining weak dielectric polarization and metal ions drift was proposed to explain the instability observed on the porous CDO film. This model may be applied to the instability phenomenon observed on the other porous low-k materials where inconsistent explanations were proposed in previous literatures.

Although both Al and Cu ions can be driven into CDO under electrical stress, no metal ions are observed in CDO with TaN gate. Furthermore, TaN shows excellent adhesion to CDO. Combining with those good properties reported previously, CDO is still a very promising material for next generation Cu-interconnect technology.

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