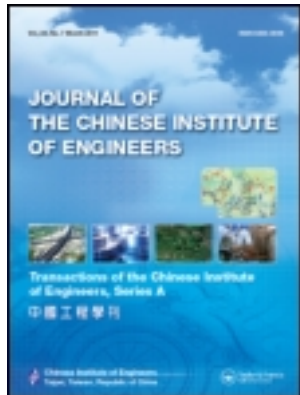


This article was downloaded by: [National Chiao Tung University 國立交通大學]

On: 27 April 2014, At: 20:04

Publisher: Taylor & Francis

Informa Ltd Registered in England and Wales Registered Number: 1072954 Registered office: Mortimer House, 37-41 Mortimer Street, London W1T 3JH, UK



Journal of the Chinese Institute of Engineers

Publication details, including instructions for authors and subscription information:

<http://www.tandfonline.com/loi/tcie20>

Design and implementation for the prototype of a microstimulator

Cheng-Ta Chiang ^a

^a Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan 30050, R.O.C. Phone: 886-3-5712121 ext. 54215 Fax: 886-3-5712121 ext. 54215 E-mail:

Published online: 03 Mar 2011.

To cite this article: Cheng-Ta Chiang (2003) Design and implementation for the prototype of a microstimulator, Journal of the Chinese Institute of Engineers, 26:3, 361-365, DOI: [10.1080/02533839.2003.9670788](https://doi.org/10.1080/02533839.2003.9670788)

To link to this article: <http://dx.doi.org/10.1080/02533839.2003.9670788>

PLEASE SCROLL DOWN FOR ARTICLE

Taylor & Francis makes every effort to ensure the accuracy of all the information (the "Content") contained in the publications on our platform. However, Taylor & Francis, our agents, and our licensors make no representations or warranties whatsoever as to the accuracy, completeness, or suitability for any purpose of the Content. Any opinions and views expressed in this publication are the opinions and views of the authors, and are not the views of or endorsed by Taylor & Francis. The accuracy of the Content should not be relied upon and should be independently verified with primary sources of information. Taylor and Francis shall not be liable for any losses, actions, claims, proceedings, demands, costs, expenses, damages, and other liabilities whatsoever or howsoever caused arising directly or indirectly in connection with, in relation to or arising out of the use of the Content.

This article may be used for research, teaching, and private study purposes. Any substantial or systematic reproduction, redistribution, reselling, loan, sub-licensing, systematic supply, or distribution in any form to anyone is expressly forbidden. Terms & Conditions of access and use can be found at <http://www.tandfonline.com/page/terms-and-conditions>

Short Paper

DESIGN AND IMPLEMENTATION FOR THE PROTOTYPE OF A MICROSTIMULATOR

Cheng-Ta Chiang

ABSTRACT

In this paper, the first domestic implementation of an implantable microstimulator utilizing HDL and ASIC methodologies is presented. We implement the digital part of the microstimulator by writing the hardware description language for the digital circuits, synthesizing them and downloading them into a field programmable gate array. The analog part is designed by using full-custom IC design flow, implemented by CMOS 0.35 μm technology, and fabricated by TSMC. It generates a maximum current of 2.77 mA through 1 k Ω load while the stimulation frequency is 20Hz and the stimulation current pulse width is 300 μs , and the maximum power consumption is evaluated at 14 mW based on a 5 V voltage supply.

Key Words: microstimulator, functional neuromuscular stimulation, IC design.

I. INTRODUCTION

Over the years, researchers and clinicians have used electrical stimulation in many applications, such as providing controllable limb function for paraplegics and quadriplegics and sensations of sound for the profoundly deaf (Hambrecht and Reswick, 1997; Buckett *et al.*, 1988). When electrical stimulation is used to simulate motor neurons and elicit controllable muscle contraction, it is called functional neuromuscular stimulation (FNS). These electrical stimuli are applied to various muscle groups through appropriate electrodes that are connected to stimulator circuitry.

The early FNS systems utilized discrete devices for constructing the stimulator circuitry, which were too heavy to carry around and not suitable for implantation. With the advancement of VLSI techniques, totally implanted FNS systems have become feasible in recent years (Ziaie *et al.*, 1997). In general, an implantable stimulator must satisfy the following requirements: 1) long life time, 2) high reliability, 3)

small size and 4) high degree of reprogrammability (Arabi and Sawan, 1999). Although we must comply with all requirements, in this prototype design, we focus on a system design based on requirements 3) and 4) above. Requirement 3) is for an analog part and requirement 4) is for a digital part of the microstimulator. In this paper, we do not integrate all the circuits onto a single chip immediately. And we propose prototype designs for implantable stimulators for different neuro-prosthesis applications, for example, a retinal prosthetic device and a bladder controller.

In our prototype design, we use a 5 V voltage supply and generate maximum stimulus current of 2.77 mA. Therefore, the maximum power consumption of the current stimulation module is evaluated at 14 mW according to the equation ($P=I*V$). In this paper, the first domestic implementation of an implantable microstimulator utilizing HDL and ASIC methodologies is presented. The digital part of the stimulator is implemented by field programmable gate array (FPGA), and the analog part is implemented with CMOS 0.35 μm technology and fabricated by TSMC. It generates a maximum stimulus current of 2.77 mA through 1 k Ω load while the stimulation frequency is 20Hz and the stimulation current pulse

The author is with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan 30050, R.O.C. (Tel: 886-3-5712121 ext. 54215; Fax: 886-3-5715412; E-mail: p9011838@alab.ee.nctu.edu.tw)

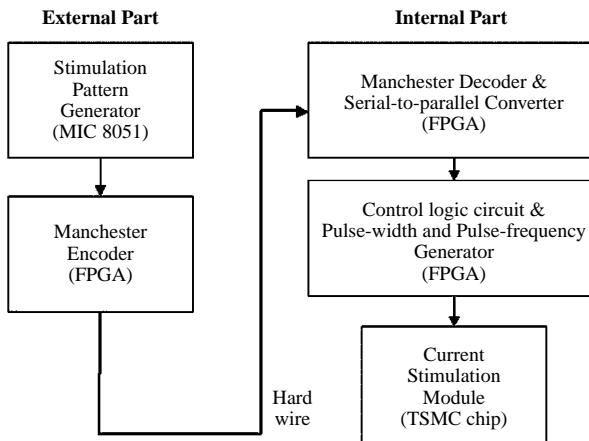


Fig. 1 Block diagram of prototype of the complete stimulation system

width is 300 μ s.

The paper is organized as follows. In Section II, the whole stimulation system is introduced briefly. Implementation of the stimulation system is described in detail in Section III. Section IV describes the simulation results. The conclusion is provided in Section IV.

II. SYSTEM DESCRIPTION

One of the current trends for implanted systems is to utilize wireless communication for data and power transmission (Arabi and Sawan, 1999). In the prototype, we plan to use real wires instead of wireless RF. Therefore, we use a 5 V battery to supply the whole circuit. Fig. 1 shows the block diagram of the prototype of the complete stimulation system. Here, one transmission wire and UART serial transmission protocol are adopted to mimic the function of RF design. Since unsuitable stimulation frequency and current pulse width would make muscles fatigued quickly, we have to carefully design the stimulation channel (Hambrecht and Reswick, 1997). In our specification of FNS, first, the stimulation frequency is about 20Hz and the stimulation current pulse width is about 300 μ s. Second, the maximum amplitude of current intensity is about 3.5 mA. Third, the finite state machine should be easily programmed from the input data. Hence, we adopt the specifications in the design. In the following section, we will describe the implementation in detail.

III. IMPLEMENTATION

1. External Controller

Generally speaking, in an implanted system we

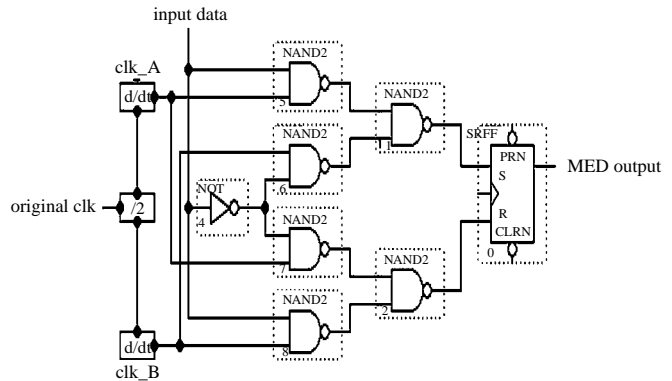


Fig. 2 Block diagram of Manchester encoder

need the same time base for both the transmitter and the receiver to avoid errors due to sampling of the data at the wrong time. Hence, data and clock are usually combined at the transmitter and are sent to the internal stimulator. Based on this consideration, we construct a flexible and programmable external controller. The controller consists of two components: the stimulation-pattern generator and the Manchester encoder. Each of them is described in the following.

(i) Stimulation-pattern Generator

The stimulation-pattern generator is designed to generate stimulation patterns suitable for selective stimulation strategies. To make our design more flexible, the generator is realized using the 8051 microcontroller. Using the programmability provided by the MIC 8051, the generator can implement different stimulation algorithms and generate various stimulation patterns. Thus, the physician or the patient can tune and select suitable stimulation strategies and patterns easily.

(ii) Manchester Encoder

If the timing for the transmitter and the receiver is independent, a small difference can cause big errors due to sampling the data at the wrong time. In the design, we adopt Manchester coding, an efficient technique to combine data and clock together, to solve the problem. Fig. 2 shows the block diagram for a Manchester encoder. The serial output of the encoder, named Manchester-encoded data (MED), has the property of bit-center transition. In Fig. 2, the RS flip-flop must be satisfied (Harold, 1998):

$$Set = clock_A \cdot data + clock_B / data \quad (1)$$

$$Reset = clock_A / data + clock_B \cdot data \quad (2)$$

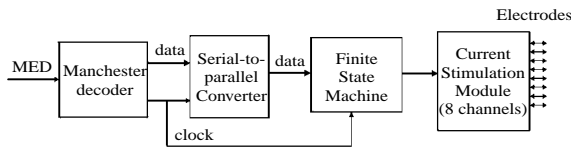


Fig. 3 Block diagram of implantable stimulator

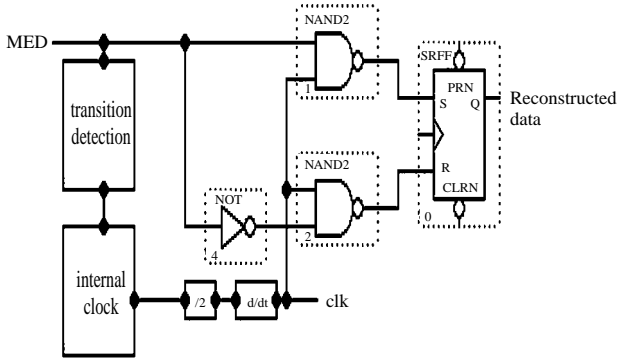


Fig. 4 Block diagram of Manchester decoder

where $clock_A$ and $clock_B$ are all clock signals, and $clock_B$ is slower than $clock_A$ for a half period of time.

2. Implantable Stimulator

Figure 3 shows the block diagram of the implantable stimulator. The first three components are grouped in digital circuits, and the last component is implemented with analog circuits. Each of them is described in the following.

(i) Manchester Decoder

The main function of the Manchester decoder is to decode the MED and to synchronize data and clock. Fig. 4 shows the block diagram of the Manchester decoder in the design. In Fig. 4, the RS flip-flop must be satisfied (Harold, 1998):

$$\text{/Set} = \text{clock} \cdot \text{MED} \quad (3)$$

$$\text{/Reset} = \text{clock} \cdot \text{/MED} \quad (4)$$

where MED is the input signal, and clock is extracted from MED signal.

(ii) Serial-to-parallel Converter

The data extracted by the Manchester decoder is in serial sequence, but parallel data is more convenient for further use. Therefore, we use a converter to transform data from serial sequence to parallel

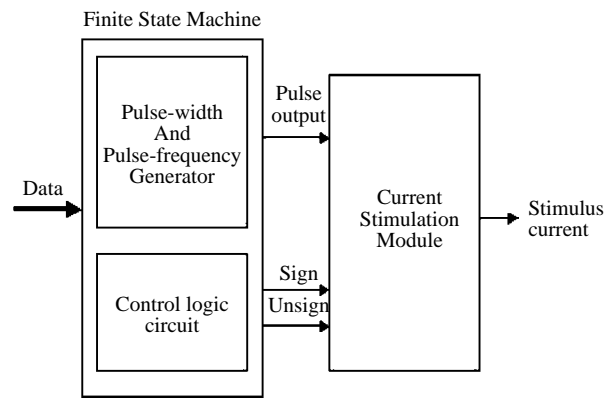


Fig. 5 Block diagram of finite state machine

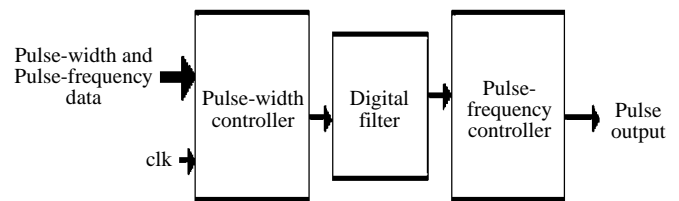


Fig. 6 Block diagram of pulse-width and stimulation frequency generator

sequence.

(iii) Finite State Machine

The function of reprogrammability is achieved by the finite state machine. Fig. 5 shows the block diagram of the finite state machine. The first function of the finite state machine is to determine the proper stimulation channel and the scale of stimulation current. The second function of the finite state machine is to generate desired pulse-width and pulse-frequency. In Fig. 6, it is composed of three main blocks: 1) pulse-width controller, 2) digital filter, 3) pulse-frequency controller. The techniques for this function block are based on the principles of pulse-width modulation, digital signal processing and digital logic design.

(iv) Current Stimulation Module

According to the finite state machine, the stimulus channel can output constant current to the corresponding electrode. In addition, the typical impedance of a nerve is $1 \text{ k}\Omega$, so the proposed stimulation channel is designed to generate a maximum current of 3.5 mA through $1 \text{ k}\Omega$ load (Bourret *et al.*, 1997).

In our design, the current stimulation module is composed of three components, current-mode

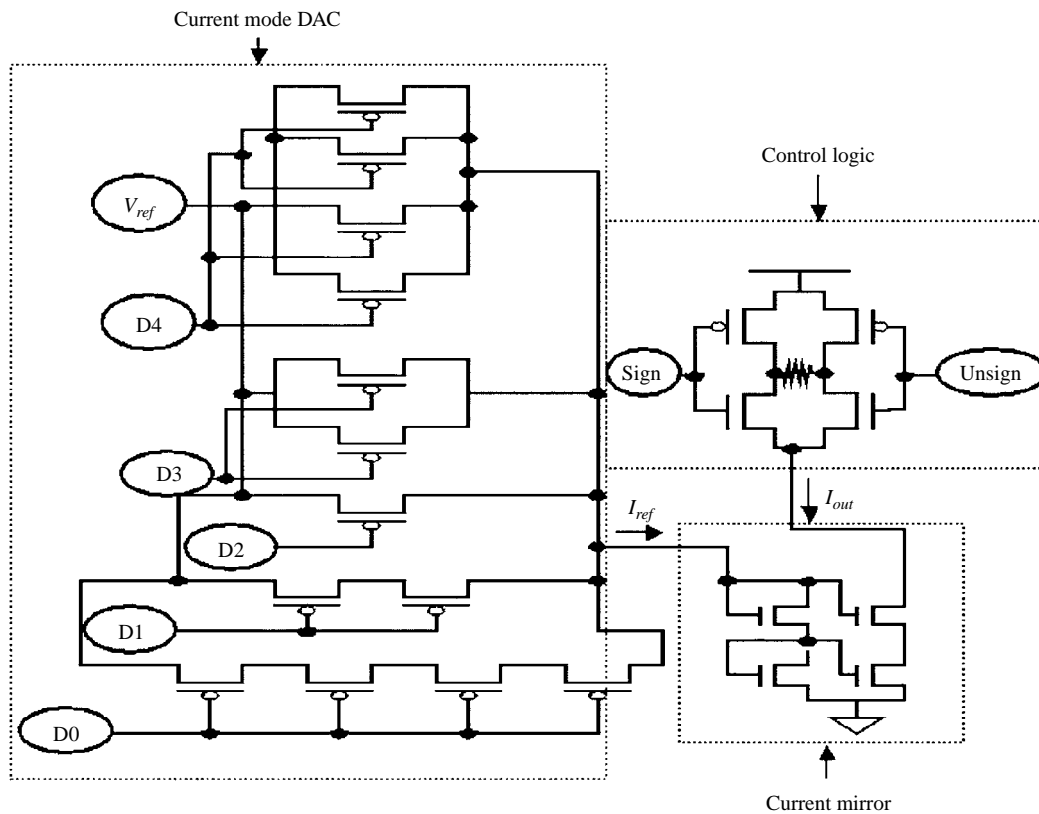


Fig. 7 Circuit diagram of the stimulation module

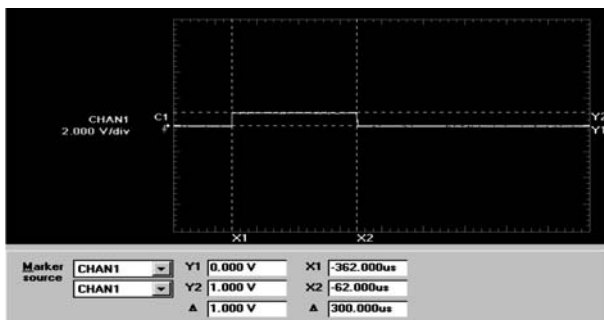
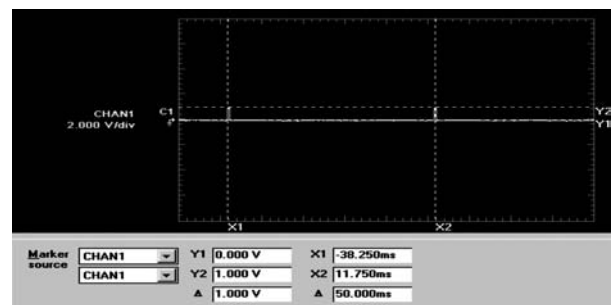
Fig. 8 Pulse width 300 μ s

Fig. 9 Stimulation frequency 20Hz

digital-to-analog converter (DAC), current mirror, and control logic, as shown in Fig. 7. The output current of DAC can be varied into 32 different levels ranging from 0 to 3.5 mA, thus the difference of each level is about 108 μ A. The reason for choosing 5-bit DAC is that we must be concerned with the sensitivity of nerves. The transistors of DAC are operated in the triode region. Therefore, we have to adjust the dimensions of the transistors so that they can provide the appropriate reference current, denoted as I_{ref} . Then, I_{ref} is amplified by the following current mirror (Amand *et al.*, 1995). It consists of two input signals, SIGN and UNSIGN, to determine the current direction through the nerve. With the switching

between SIGN and UNSIGN, the bi-direction current can flow through one side of the P transistor to the other side of the N transistor.

IV. SIMULATION RESULTS

The current stimulator is implemented by using TSMC 0.35 μ m CMOS technology. With hardware verification, the output current could be up to 2.77 mA with approximately 87 μ A for each level. The maximum power consumption of the current stimulator is around 14 mW based on a 5 V voltage supply according to the equation ($P=I*V$). Figs. 8 and 9 show the verification of pulse width 300 μ s and

stimulation frequency 20Hz according to a transmission code, respectively. Besides, the output current intensity is about 1mA through 1 k Ω load.

V. CONCLUSIONS AND PROSPECTS

The prototype of an implantable microstimulator is proposed for functional neuromuscular stimulation in this paper. The digital circuits are implemented by the field programmable gate array. The analog circuits are implemented with CMOS 0.35 μ m technology and fabricated by TSMC. The current stimulator can generate a maximum current of 2.77 mA through 1 k Ω load while the stimulation frequency is 20Hz and the stimulation current pulse width is 300 μ s, and provide constant output current with relative linearity. Due to process variation, the linearity of DAC and maximum current intensity are affected. That means that we should consider more matching techniques of DAC to reduce current variation for the next version of the current stimulator.

The proposed designs for different blocks of the microstimulator could be used as building blocks to realize other implantable devices. The Manchester code has been proved to be a good choice for transmission of implantable systems. And the prototype stimulation system could achieve the general specification of FNS (stimulation frequency 20Hz and stimulation current pulse width 300 μ s).

The RF module is still in progress. In the future, we will design other components of the microstimulator, including RF-AM modulator, and RF-AM demodulator, etc. We expect to implement and test all these function blocks individually. With the mixed-mode VLSI design, we will finally integrate these components in a single chip FNS experiments in animals.

ACKNOWLEDGEMENTS

Author would like to acknowledge the support of the National Science Council (NSC) and the National Health Research Institutes (NHRI).

NOMENCLATURE

ASIC application specific integrated circuit

HDL	hardware description language
Hz	hertz
k Ω	kiloohm
mA	milliampere
mW	milliwatt
μ A	microampere
μ s	microsecond
μ m	micrometer
V	volt

REFERENCES

- Arabi, K., and Sawan, M. A., 1999, "Electronic Design of a Multi-channel Programmable Implant for Neuromuscular Electrical Stimulation," *IEEE Transactions on Rehabilitation Engineering*, Vol. 7, pp. 204-214.
- Amand, R. S., Savaria, Y., and Sawan, M., 1995, "Design Optimization of a Current Source for Microstimulator Applications," *Proceedings of IEEE Circuits and Systems Society*, Vol. 1, pp. 129-132.
- Bourret, S., Sawan, M., and Plamondon, R., 1997, "Programmable High-amplitude Balanced Stimulus Current-source for Implantable Microstimulators," *Proceedings of IEEE Engineering in Medicine and Biology Society*, Vol. 5, pp. 1938-1941.
- Buckett, J. R., Peckham, P. H., and Thrope, G. B., 1988, "A Flexible, Portable System for Neuromuscular Stimulation in the Paralyzed Upper Extremity," *IEEE Transactions on Biomedical Engineering*, Vol. 35, No. 11, pp. 897-904.
- Hambrecht, F. T., and Reswick, J. B., 1997, *Functional Electrical Stimulation Application in Neural Prosthesis*, Marcel Dekker, New York.
- Harold, B. K., 1998, *Fiber Optic Communication*, Prentice Hall, N.J.
- Ziaie, B., Nardin, M. D., Coghlan, A. R., and Najafi, K., 1997, "A Single-channel Implantable Microstimulator for Functional Neuromuscular Stimulation," *IEEE Transactions on Biomedical Engineering*, Vol. 44, No. 10, pp. 909-920.

Manuscript Received: Dec. 13, 2001

Revision Received: Sep. 19, 2002

and Accepted: Nov. 11, 2002