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Nanoscale Multigate TiN Metal Nanocrystal Memory Using High-*k* Blocking Dielectric and High-Work-Function Gate Electrode Integrated on Silicon-on-Insulator Substrate

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In this study, a charge-trapping-layer-engineered nanoscale n-channel trigate TiN nanocrystal nonvolatile memory was successfully fabricated on silicon-on-insulator (SOI) wafer. An Al_2O_3 high-*k* blocking dielectric layer and a P^+ polycrystalline silicon gate electrode were used to obtain low operation voltage and suppress the back-side injection effect, respectively. TiN nanocrystals were formed by annealing TiN/Al_2O_3 nanolaminates deposited by an atomic layer deposition system. The memory characteristics of various samples with different TiN wetting layer thicknesses, post-deposition annealing times, and blocking oxide thicknesses were also investigated. The sample with a thicker wetting layer exhibited a much larger memory window than other samples owing to its larger nanocrystal size. Good retention with a mere 12% charge loss for up to 10 years and high endurance were also obtained. Furthermore, gate disturbance and read disturbance were measured with very small charge migrations after a 10^3 s stressing bias. © 2009 The Japan Society of Applied Physics

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1. Introduction

Since Kahng and Sze invented the first floating gate nonvolatile memory (NVM) at Bell Lab. in 1967,[1] various kinds of floating gate memories have been proposed and the process technology progressed rapidly. Floating-gate NVM has the following advantages: large memory window, high program/erase (P/E) speed, and good reliability for commercial applications. In recent years, flash memories have become one of the fastest growing semiconductor technologies and provide hundreds of portable electronic products. However, the International Technology Roadmap for Semiconductors (ITRS) forecasts that the scaling limitation of conventional floating gate memories is around the 40 nm node[2] and some challenges would be encountered in the near future. The main issue is unscalable tunneling oxide thickness for maintaining acceptable retention performance; therefore, a high operation voltage is needed, which is predicted to be around 17 V for the 40 nm node. An increased floating gate coupling effect is another issue for continuously closing floating gate memory cells. Therefore, NAND technology is projected to migrate to charge trapping devices with discrete traps for charge storage, such as silicon/oxide/nitride/oxide/silicon (SONOS) and nanocrystal (NC) structures.[2]

SONOS-type memories which store charges in a discrete trap node of their silicon nitride layer, exhibit improved retention performance so that the tunneling oxide thickness can be reduced to increase P/E speed and decrease operation voltage.[3–8] Besides, some advanced SONOS memories such as bandgap-engineered SONOS (BE-SONOS) and TANOS have demonstrated a high P/E speed and have attracted much attention for application in future NVM.[9,10] Unfortunately, all SONOS-type memories have unwanted migration of stored charges in the nitride layer. Nanocrystal memories, which use various materials as the storage node such as Si, Ge, HfO_2, Pt, Ag, Au, Ni, and TiN, have been proposed and have become another possible solution for future NVM applications.[11–26] Nanocrystal memories may have better charge storage ability than SONOS-type memories owing to the fact that each nanocrystal in them is theoretically isolated by the surrounding dielectric. Therefore, a thinner tunneling oxide can be used to improve P/E speed and reduce P/E operation voltage without degrading retention performance. Moreover, metal nanocrystals have better work function engineering ability and higher density of state around the Fermi level than semiconductor nanocrystals. Although much literature has been reported on proposals concerning various techniques for forming nanocrystals, one of the main challenges of nanocrystal memories is their storage node property, which means that nanocrystal quality parameters including density, size, and distribution should be improved in nanocrystal formation.[21–26]

Recently, multigate field-effect transistors (MuGFETs) have been predicted as one of the most potential solutions for the NAND Flash beyond the 25 nm node, and various SONOS-type and nanocrystal memories have been fabricated with multigate structure.[2] It has been reported that the multigate memory cell can achieve excellent short-channel effect controllability, high driving current, low leakage current, good programming inhibition, and a large number of nanocrystals in one cell.[3–6,11–13] Furthermore, the potential of a floating fin-type body is modulated in the multigate structure, differently from that in the single gate structure, and exhibits a longer charge retention time.[12]

Moreover, TiN nanocrystal memories with a higher density of TiN nanocrystals can be formed in the surrounding Al_2O_3 dielectric and these memories can exhibit a larger hysteresis memory window that has the potential to be used in future nanoscale multilevel flash memory device applications.[20,24] In this work, an n-channel multigate metal NC memory using TiN nanocrystals, an Al_2O_3 high-*k* blocking dielectric layer, and a P^+ polycrystalline silicon (poly-Si) gate electrode was fabricated on a silicon-on-insulator (SOI) wafer. The work function of TiN is extracted at around 4.6 eV;[20,27] it is expected to provide a level 0.6 eV deeper than that of Si nanocrystals to improve retention performance. The high-*k* dielectric, Al_2O_3, has an energy bandgap similar to that of SiO_2, but has a higher gate-to-channel coupling efficiency. Therefore, using Al_2O_3 as a blocking

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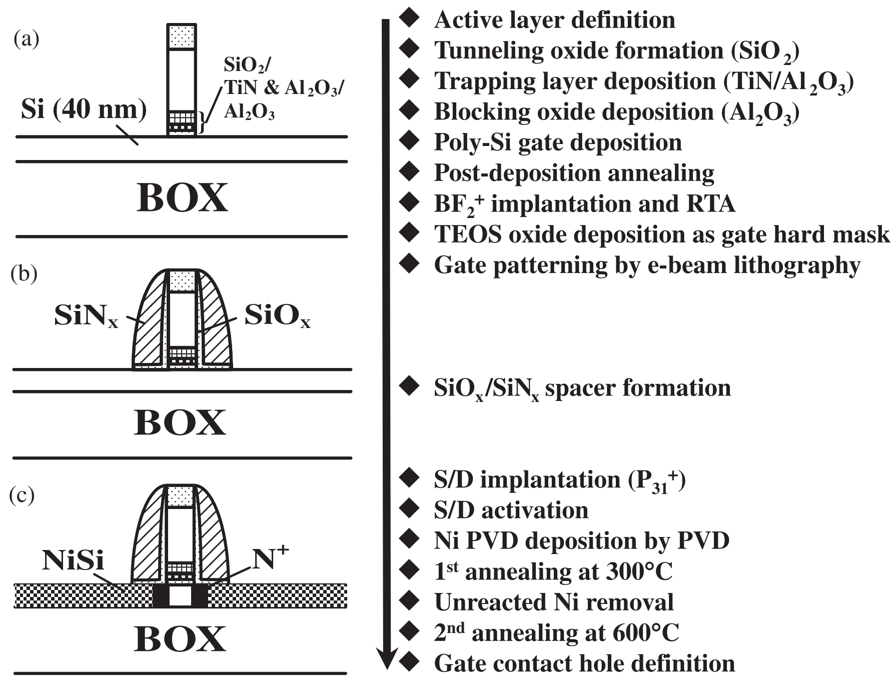

Fig. 1. Process flow of n-channel MuGFET TiN nanocrystal NVM on SOI substrate.

dielectric layer can lower P/E operation voltage. In addition, using a high-work-function gate electrode can enhance the erase characteristics by suppressing the unwanted back-side injection effect.[6] Moreover, the nanocrystal size effects on memory window, P/E speed, and retention property are also be discussed.

2. Experimental Procedure

Figure 1 shows the main process flow of the n-channel multigate TiN nanocrystal memory cell. The starting material is a 6 in. separation-by-implanted-oxygen (SIMOX) SOI wafer with a 40-nm-thick SOI layer and a 150-nm-thick buried oxide layer. The SOI layer is lightly boron-doped and the doping concentration is around 1×10^{15} cm^{-3}. The Si fins in the $\langle 110 \rangle$ direction were patterned by e-beam lithography and plasma dry etching. Next, a 3.6 nm-thick-tunneling oxide layer was thermally grown using a furnace system at 800 °C. Then, in order to provide a material for forming nanocrystals and its surrounding material, a TiN wetting layer of 0.5 or 0.7 nm thickness and an Al_2O_3 layer of 1 nm thickness were sequentially deposited with seven periods in a PEALD/ALD clustered system and a 15- or 20-nm-thick Al_2O_3 layer was deposited consecutively as the blocking dielectric layer in the same ALD system followed by a 150-nm-thick amorphous Si deposition at 545 °C as the gate electrode. The TiN layers were deposited with $TiCl_4$ as a precursor at 350 °C in N_2/H_2 gas ambience and the Al_2O_3 layers were deposited with trimethylamine (TMA) and H_2O as precursors at 300 °C. Next, post-deposition annealing (PDA) was performed at 900 °C for 10 or 40 s in nitrogen gas ambience to provide sufficient surface mobility to transform the TiN wetting layer into nanocrystals.[16]

In order to estimate the effect of charge trapping layer engineering, a set of devices with various TiN wetting layer thicknesses, blocking dielectric thicknesses, and PDA times were fabricated. The sample ID and process parameters are listed in Table I. The TiN wetting layer thickness of sample A (0.7 nm) is larger than that of the other samples (0.5 nm). Sample B has the longest PDA time (40 s) among all the samples. Moreover, sample D has the smallest blocking dielectric thickness (15 nm). The poly-Si gate was doped by BF_2^+ ion implantation at 40 keV up to a dose of 5×10^{15} cm^{-3} followed by activation at 900 °C for 20 s in nitrogen gas ambience. Before gate definition by e-beam lithography and dry etching, a thick TEOS oxide layer was deposited by low-pressure chemical vapor deposition (LPCVD) at 695 °C as a hard mask to prevent the antidoping of the poly-Si gate during n$^+$ source/drain (S/D) doping. The device structure in this process step is shown in Fig. 1(a).

Table I. Gate stacks conditions of samples A–D.

Sample	Tunneling oxide (nm)	TiN/Al_2O_3 (seven periods) (nm/nm)	Blocking oxide (nm)	PDA time at 900 °C (s)
A	4	0.7/1	20	10
B	4	0.5/1	20	40
C	4	0.5/1	20	10
D	4	0.5/1	15	10

Next, a SiO_x (10 nm)/SiN_x (40 nm) stack layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 300 °C and dry-etched to form a composite spacer as shown in Fig. 1(b). Then, P_{31}^+ ions were implanted in S/D areas at 20 keV up to a dose of 5×10^{15} cm^{-3} and rapid thermal annealing (RTA) at 900 °C for 20 s was performed to activate the S/D dopants. Then, a TEOS hard mask and a native oxide were selectively etched using HF solution and a 25-nm-thick Ni layer was deposited by e-gun evaporation followed by a two-step self-aligned Ni-silicide process to obtain better controllability of Ni silicide

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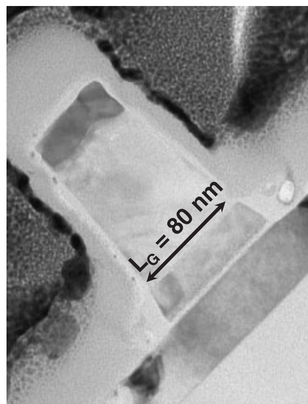

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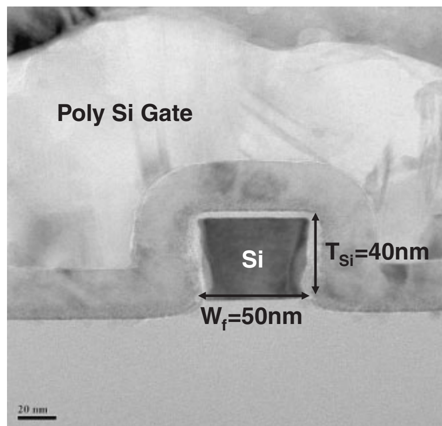

(b)

Fig. 2. High-resolution X-TEM images of the fabricated MuGFET TiN nanocrystal memory with (a) gate length of 80 nm and (b) fin width of 50 nm.

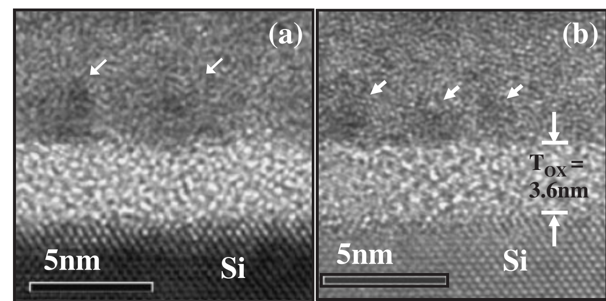

Fig. 3. High-resolution X-TEM images of samples A–B. The thickness of SiO_2 as the tunneling oxide is 3.6 nm. Nanocrystals with diameter of around (a) 3 nm in sample A and (b) 1–2 nm in sample B were embedded by Al_2O_3.

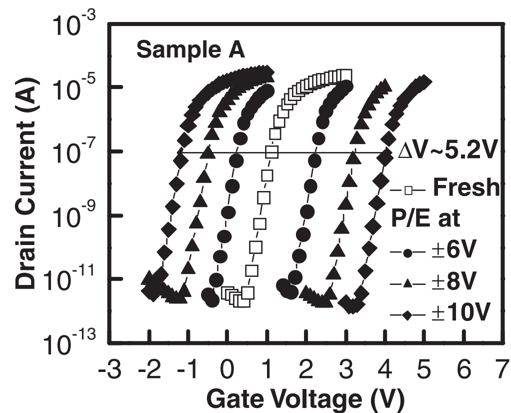

Fig. 4. Transfer characteristics of sample A after various P/E bias for 0.1 s.

lateral formation. The first silicidation step was vacuum annealing at 300 °C for 45 min and the Ni silicide was formed in the Ni_2Si phase. After removing unreacted Ni film by $H_2SO_4 : H_2O_2$ (3 : 1) solution at 75 °C, the second silicidation step was performed at 600 °C for 30 s to transform the $NiSi_2$ phase to the NiSi phase. The S/D region was converted into a full NiSi structure, as shown in Fig. 1(c). The gate electrode became a polycide structure after the silicidation.

All the measured cells have the same device dimensions of $W/L = 50\,\text{nm}/80\,\text{nm}$. The cross-sectional transmission electron microscopy (X-TEM) images of the fabricated tri-gate nanocrystal memory (sample B) with a gate length of 80 nm and a fin width of 50 nm are shown in the Figs. 2(a) and 2(b), respectively. Moreover, Ni silicides are formed in the S/D region and the top of the gate electrode. Figure 3 shows high-resolution X-TEM images of samples A and B to magnify the charge trapping layer. The tunneling oxide thickness is around 3.6 nm and TiN nanocrystals embedded in Al_2O_3 can be observed. Note that the diameter of TiN nanocrystal in sample A is around 3 nm, which is larger than that in sample B of about 1–2 nm because sample A has a thicker TiN wetting layer and could provide more material to form larger TiN nanocrystals than sample B. In the next section, we will show that NC size has a marked effect on memory performance as previously reported.[18,29)]

3. Results and Discussion

3.1 P/E speed and memory window

Figure 4 shows the transfer characteristics of sample A with various P/E biases for 0.1 s. For the fresh device, the threshold voltage is 1 V, the driving current capability is 236 μA/μm at $|V_{GS} - V_{TH}| = V_{DS} = 1$ V, and on/off current ratio is larger than 10^7. Moreover, sample A exhibits a memory window as large as 5.2 V after P/E at ±10 V for 0.1 s and has the potential of multilevel operation by choosing P/E bias carefully. Figure 5 shows the P/E speeds of samples A–D with the same pulse bias at ±10 V and different pulse widths. All the devices utilized Fowler–Nordheim (FN) tunneling for P/E operations and both source and drain terminals were grounded during the biasing pulse. In either the programming properties shown in Fig. 5(a) or the erasing properties shown in Fig. 5(b), sample A has the largest V_{TH} shift at the same P/E time, which indicates that charges are stored in the TiN nanocrystals but not in Al_2O_3. Because sample A utilized a thicker TiN wetting layer (0.7 nm) than the other samples (0.5 nm), the larger nanocrystals, shown in Fig. 3(a), enhance storage capability. As device dimensions continually shrink, small NCs provide more trapping sites and are beneficial for three-dimensional integration. However, some reports proposed that the diameter of nanocrystals has a marked effect on programming and retention characteristics and the optimal nanocrystal size is around 5 nm.[18,29,30)] In

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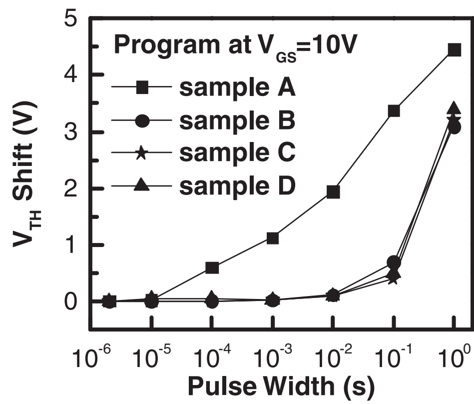
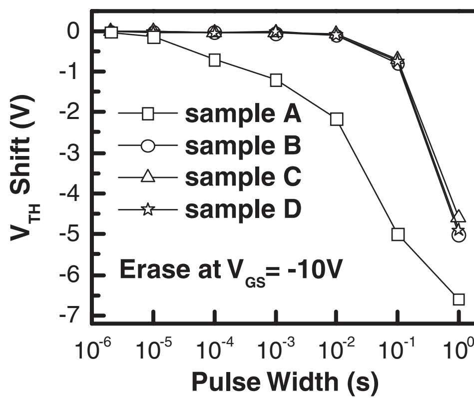


(a)



(b)

Fig. 5. (a) Programming speeds and (b) erasing speeds of samples A–D with same pulse bias at ±10 V and different pulse width.

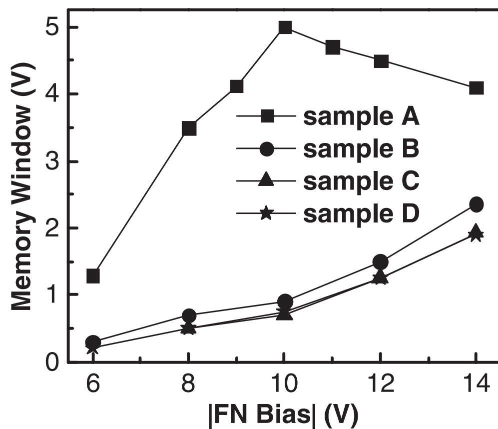
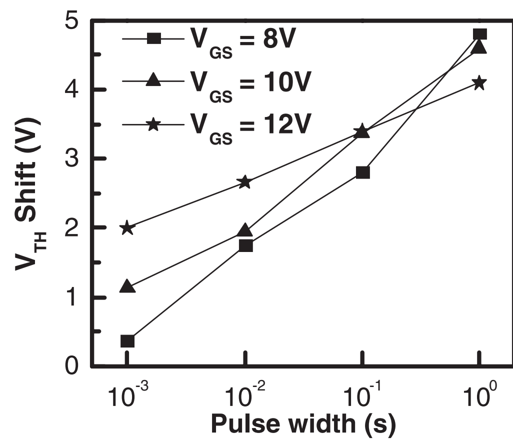


Fig. 6. Memory windows of samples A–D after various P/E biases for 0.1 s. The P/E operations utilized FN tunneling, and both source and drain terminals were grounded during the biasing pulse.

our samples, the nanocrystal sizes of samples A (~3 nm) and B (1–2 nm) are so small that pronounced critical quantum confinement and coulomb blockade effects occur to degrade the charge trapping efficiency, which may decrease the program speed.

Figure 6 shows the memory windows of samples A–D after various P/E biases for 0.1 s. Sample A has the largest memory window under all biases among the other samples owing to the large NC size. On the other hand, because



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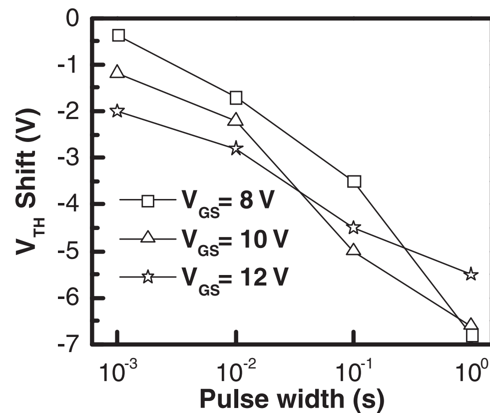

(b)

Fig. 7. (a) Programming speed and (b) erasing speed of sample D with various pulse biases and pulse widths.

sample B has the longest PDA time (40 s), a slightly larger memory window is obtained in sample B than in samples C–D. This implies that a moderately longer annealing time helps the formation of TiN nanocrystals. However, total TiN mass has much more significant effects on TiN nanocrystal size. Moreover, the device with a thinner blocking dielectric of 15 nm thickness (sample D) has almost the same memory window as the device with thicker blocking dielectric of 20 nm thickness (sample C), which indicates that the back-side electron injection is quite negligible under these FN bias conditions.

The memory windows of samples B–D increased monotonically with increasing FN bias. However, the memory window of sample A increases to its largest value at ±10 V and then decreases as P/E bias increases further. The degradation of the memory window in the strong P/E electrical field is usually attributed to the back-side electron injection effect. Figure 7 shows the P/E speeds of sample A under various bias conditions. The V_{TH} values in both the programmed and erased states were affected at a high P/E voltage. Because of the larger hole/electron injection rate from the gate electrode to nanocrystals during higher-P/E bias operations, these injected carriers from the gate would recombine with the electrons/holes injected from the Si channel.[28] Therefore, smaller V_{TH} shifts or the so-called saturation phenomenon of the V_{TH} shift is observed in both

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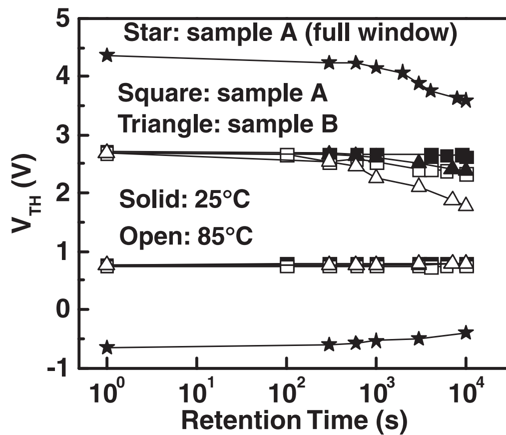


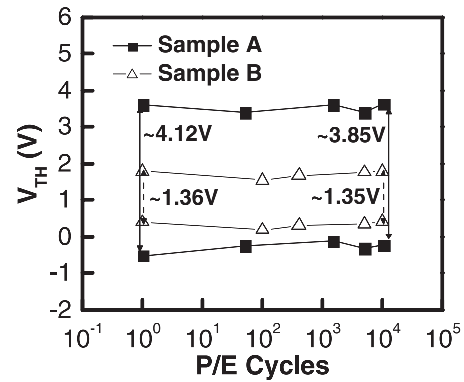
Fig. 8. Retention characteristics of trigate TiN nanocrystal memory devices of samples A–B at room temperature ($T = 25\,°C$) and high temperature ($T = 85\,°C$).

the program and erase states at P/E biases higher than $\pm 10\,V$ for larger pulse width. In Fig. 7, the V_{TH} shift increases with increasing pulse width and pulse bias when the pulse width is shorter than 0.1 s. However, as the pulse width increases to 1 s, the V_{TH} shift decreases in both the programmed and erased states with increasing FN bias and the maximum memory window is obtained at $\pm 8\,V$. This phenomenon indicates again that as the amount of stored carriers increases to a certain value in the nanocrystals, the degradation of the memory window occurs. Hence, memory window degradation should also occur in samples B–D after a much larger P/E bias or pulse width is achieved.

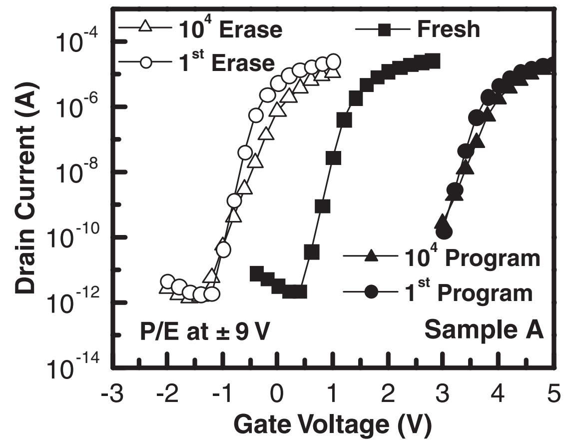
3.2 Retention performance

Figure 8 shows the retention characteristics of samples A and B at temperatures $T = 25$ and $85\,°C$. In order to compare charge loss rate, sample A, which has the maximum memory window, was programmed and erased at $\pm 10\,V$ for 0.01 s to reach a similar programmed state and the erased state of sample B, which was programmed and erased at $\pm 12\,V$ for 0.1 s. In this case, the memory window for both samples is about 1.95 V, which is close to the maximum memory window of sample B. It can be observed that sample A has a lower charge loss rate than sample B either at $T = 25$ or $85\,°C$ because the nanocrystal size of sample A (~3 nm) is larger than that of sample B (~1 to 2 nm). The 3 nm nanocrystal is still too small to be affected by the Coulomb repulsive force and quantum confinement effect. The Coulomb repulsive force would discharge trapped carriers more quickly in the nanocrystals and increase charge loss rate.[29,30] Moreover, the quantum confinement effect in nanocrystals would split the energy level and raise trap energy so that stored charges can escape more easily. At a similar initial memory window of around 2 V, charges stored in the nanocrystals of sample A have not reached saturation and more carriers can be stored in sample A with a lower Coulomb repulsive force and a smaller quantum confinement effect. On the other hand, there exist stronger Coulomb repulsive force and quantum confinement effect for degrading the retention performance more critically in sample B. At room temperature, only a 6% charge loss after 10^4 s in sample A and an 18% charge loss after 10^4 s in sample B were observed. Moreover, a mere 12% charge loss up to 10 years in sample A at room temperature was observed. Both the charge losses of samples A and B are more serious at higher temperature than at room temperature owing to the more energetic trapped carriers that can escape easily from TiN nanocrystals.

In order to compare the retention performance of samples A and B at the maximum initial memory window, the retention property of sample A with a full memory window is also measured. The initial memory window is around 5 V and has a 21% charge loss after 10^4 s, which is about the same charge loss in sample B, indicating that although the quantum confinement effect is one of the reasons for the enhancement of charge loss, Coulomb repulsive force is the main reason for the degradation of the retention performance at various initial memory windows in the TiN metal nanocrystals with diameters in the 1–3 nm range. However, the quantum confinement effect has an important role in the retention performance of semiconductor nanocrystal memories.[29)]



(a)



(b)

Fig. 9. (a) Endurance characteristics of samples A and B. The P/E bias conditions are $\pm 9\,V$, 0.1 s for sample A and $\pm 12\,V$, 0.1 s for sample B. (b) Transfer characteristics after first and 10^4 P/E cycle operations of sample A.

3.3 Endurance and disturbance

Figure 9(a) shows the endurance characteristics of samples A and B with P/E at $\pm 8\,V$, 0.1 s and P/E at $\pm 12\,V$, 0.1 s, respectively. Because the FN tunneling mechanism was used for P/E operations, the injected electrons and holes have a

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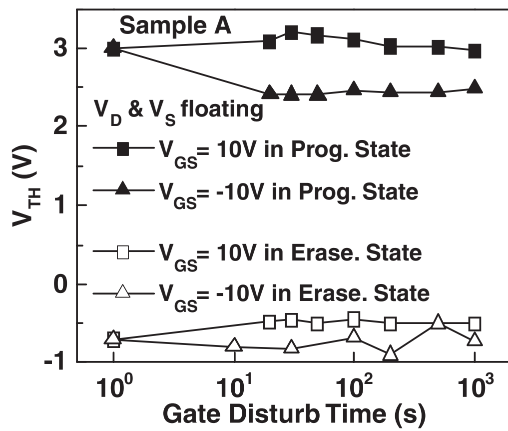

Fig. 10. Gate disturbance characteristics of sample A in four different states.

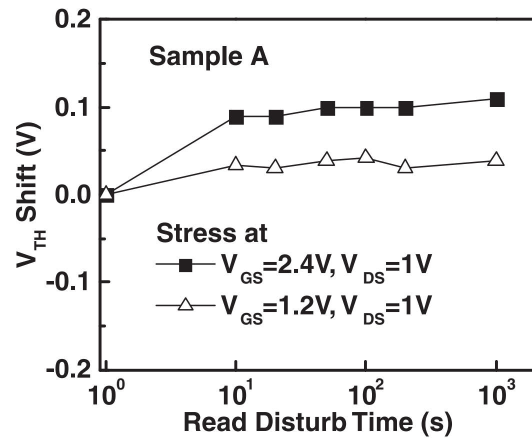

Fig. 11. Read disturbance of sample A in erase state for 10^3 s stressing bias.

uniform distribution. The distribution mismatch is negligible and neither electrons nor holes would be hard to erase after the P/E cycles.[9,31,32] Therefore, an invisible shift in the programmed and erased states can be observed and the memory window is kept at about 93% for sample A and at 97% for sample B after 10^4 P/E cycles. Figure 9(b) shows the transfer characteristics of sample A after the first and 10^4 P/E cycle operations. A small deterioration of the subthreshold swing and driving current after 10^4 P/E cycles means that a small amount of interface state was generated during the P/E cycles. For the multigate device structure, charges stored in each nanocrystal may not be identical. For example, for the nanocrystals located near the top corner of the active layer, more charges can be injected owing to a stronger electric field. This phenomenon may also result in the deterioration of the subthreshold swing.

Gate disturbance occurs when the neighboring cells, which share the same word line, are biased by programming or erasing pulses. Therefore, the gate disturbance characteristics of sample A under four situations for 1000 s are shown in Fig. 10. It can be observed that after stress at $V_{G} = \pm 10$ V for 10^3 s, the device in the erase state has a negligible V_{TH} shift, which is due to the decreased electric field in the multigate structure on the SOI wafer. In the multigate structure, the body, source and drain terminal potentials are all floating. Therefore, we suspect that the electric field between the trapping nodes and the Si body is reduced to suppress unwanted carrier migration or charge loss. However, after $V_{G} = \pm 10$ V for 10^3 s stressing in the programmed state, the device with an erased bias has a more pronounced V_{TH} shift than that with a programmed bias because the repulsive force and floating body can block the extra injected electrons in the programmed state but some stored electrons are detrapped by higher negative erased voltage. Note these disturbance properties both saturate after 10–20 s and are not critical issues. Figure 11 shows the read disturbance of sample A in the erase state for 10^3 s stressing bias. A very small variation can be observed indicating insignificant carrier migrations, injection or de-trapping during read operations.

4. Conclusions

In this work, an n-channel trigate metal nanocrystal memory using TiN nanocrystals as discrete storage nodes, a high-*k* blocking dielectric layer and a p^+ poly-Si gate was successfully fabricated. The effects of charge trapping layer thickness and post-deposition annealing time are investigated. It is observed that the memory window is determined by the size of nanocrystals. Although a longer annealing time could help the growth of TiN nanocrystals and slightly enhance the memory window, an adequate mass is the key factor for forming larger TiN nanocrystals and obtaining larger memory window. The phenomenon of the turn-down memory window as FN bias increases is observed and explained by the back-side injection effect.

In addition, the charge loss rates of samples with different nanocrystal sizes are similar when the devices are programmed and erased at the maximum initial memory window. Retention performance was mainly affected by the Coulomb repulsive force but not by the quantum confinement effect. This observation implies that the quantum confinement effect in the metal nanocrystal is not as critical as that in the semiconductor nanocrystal. Finally, the FN tunneling mechanism has a uniform injection profile to avoid unwanted charge migration, and the multigate structure on an SOI wafer with a floating body can reduce inner electric field to suppress trapped charge migration. Therefore, good endurance and disturbance performance can be obtained in multigate nanocrystal memories.

Acknowledgements

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