# Process Sensitivity and Robustness Analysis of Via-First Dual-Damascene Process

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***Abstract*—Sacrificial layer (SACL) coating had been proposed to protect the sealing layer of underlying copper lines during trench etching as via-first scheme is employed for dual-damascene patterning. Because the coated SACL thickness depends on via size and via density, the process window is hard to identify. In this paper, the criteria for a successful SACL process are derived. A four-step procedure for SACL process developing is also proposed. It is suggested that shallow trench depth and medium etch rate selectivity between inter-metal-dielectric and SACL material are preferred. The SACL thickness in via can be adjusted by adjusting the overetching percentage at the SACL breakthrough step so that the criteria are satisfied. The validity of the proposed criteria is proved by the very high yield of via chains with via size ranging from 0.27 to 0.16 $\mu$m. It is concluded that the SACL process can be robust and can be employed to reduce the thickness of the capping layer effectively even beyond the 0.13-$\mu$m technology node.**

***Index Terms*—Copper, dual-damascene, interconnections.**

## I. Introduction

As ULTRALARGE scale integrated (ULSI) back-end-of-line (BEOL) wiring is continuously scaled to narrower than a subquarter micron, copper (Cu) wiring is expected to be eventually required in the sub-0.13-$\mu$m technology node independent of products [1]. Because Cu is hard to be etched by a plasma system, a damascene process had been developed as the patterning method. Several schemes to form dual-damascene structures, such as via-first (VF), trench first, and embedded hard mask, etc., have been proposed [2]–[6]. The advantages and disadvantages of these schemes had been reviewed by Verove [7]. Among these schemes, VF scheme had been suggested as the best one due to its scalability and its tolerance to misalignment [7], [8].

The VF scheme consists of three main process steps: 1) via patterning through the whole inter-metal-dielectric (IMD) to stop on the capping layer of the underlying Cu lines; 2) trench patterning without etching through the capping layer at the via bottom; and 3) soft-etch to remove the capping layer at via bottom. Since the capping layer at via bottom is exposed to plasma during the whole trench-etching period, the capping layer must be thick enough and a high-etch rate selectivity between IMD and capping layer is required. However, the capping layer always has a dielectric constant higher than IMD, and the increase of a capping layer thickness will inevitably degrade the interconnect performance. Verove *et al.* proposed a method to protect the capping layer at via bottom by coating a sacrificial layer (SACL) before trench patterning [9]. An organic-type bottom antireflection coating (BARC) is often used for this purpose because it can be integrated with the photo-resist (PR) coating and it can be used to reduce the surface reflection. But, materials other than BARC can also be adapted. In the SACL process, the SACL thickness in via is important. If the SACL is too thin, the capping layer is not well protected. If the SACL is too thick, the so-called "fence" forms because of the masking effect of the SACL as shown in Fig. 1. Because of the characteristics of the spin-coating process, the SACL thickness in via depends on via size and via density [7]. Therefore, the SACL process must be controlled very carefully. Otherwise, the process window may be diminished [7], [9]–[11].

In this work, the robustness of the SACL process was studied comprehensively. The criteria for a successful SACL process are proposed in Section II. In Section III, following the proposed criteria, the process window sensitivity of each process parameter can be evaluated and the robustness of a SACL process can be examined. In Section IV, two double-metal examples for global wiring and local wiring were presented to demonstrate the validation and application of the proposed criteria. Via chains with low via resistance and very high yield were obtained for both examples. Since the minimum via size is only 0.16 $\mu$m, these examples also demonstrate the scalability of the SACL process to beyond 0.13-$\mu$m technology node. A conclusion is then given in Section V.

## II. Criteria for Successful SACL Process

The SACL thickness in via after trench etching for a successful SACL process must satisfy the following two criteria:

$$\text{Criterion 1: } \Delta L = T_{\mathrm{SAC,min}} > 0$$
$$\text{Criterion 2: } \Delta H = T_{\mathrm{SAC,max}} - H_{\mathrm{VIA,min}} < 0$$

where $T_{\mathrm{SAC,min}}$ and $T_{\mathrm{SAC,max}}$ are the thinnest and the thickest SACL thickness that remain in via after trench etching, respectively, and $H_{\mathrm{VIA,min}}$ is the minimum via height after trench etching. Criterion 1 asks that the SACL still remains in via after trench etching in the worst case such that the capping layer at via bottom can be well protected. Criterion 2 guarantees "fence free" because once the SACL is lower than via height, no masking effect will occur. In the VF scheme, facet always occurs

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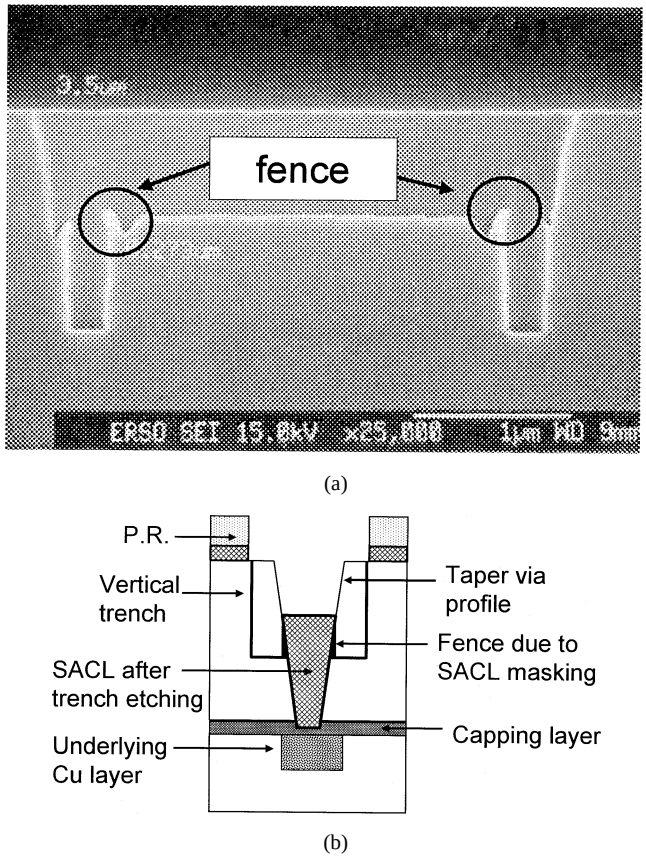


(a)

(b)

Fig. 1. (a) Cross-sectional scanning electron microscope (SEM) micrograph of the so called "fence." (b) Schematic drawing of the "fence" formation due to the masking effect of SACL.

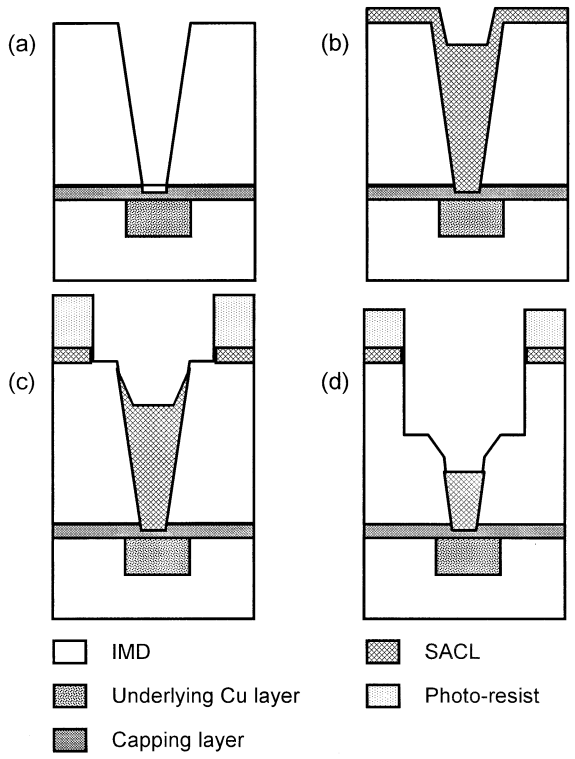


Fig. 2. Schematic drawing of the process steps of a successful SACL process: (a) after via patterning, (b) after SACL coating; (c) after trench photo-resist patterning and SACL breakthrough; and (d) after trench etching. It should be noted that the SACL must remain in via but its thickness must be lower than via height.

at the top corner of the via no matter if etch-stop-layer is used or not and the $H_{\mathrm{VIA,min}}$ should be calculated from via bottom to the lower corner of the facet.

Several processes, including SACL coating, SACL breakthrough, trench etching, and IMD thickness, affect the values of $T_{\mathrm{SAC,min}}$, $T_{\mathrm{SAC,max}}$, and $H_{\mathrm{VIA,min}}$. To link these processes to the criteria, the effect of these processes on the SACL thickness must be considered step by step. Fig. 2 shows the schematic drawing of the process steps of the VF scheme. After via etching, the SACL layer is spin coated on the wafer followed by the photo-resist coating and patterning. The as-coated thickness of SACL in the via depends on via size and via density. Although the dependence is a function of SACL material and coating condition, the thinnest SACL thickness $(T_{\mathrm{SAC},L0})$ and the thickest SACL thickness $(T_{\mathrm{SAC},H0})$ always occur at the most isolated via and the densest via, respectively. Therefore, only these two extreme cases have to be considered.

Before the etching of IMD, the SACL on IMD at the trench area must be removed at first. It can be done by a blanket SACL etch-back step before PR coating or by an SACL breakthrough step after PR developing. The maximum thickness $(T_{\mathrm{SAC}})$ occurs at the region which is free of via and is equal to the thickness on the blanket wafer. Let the etch rate uniformity of the SACL remove step be $U_{\mathrm{SR}}$ and the overetching percentage be $\mathrm{OE}_{\mathrm{SR}}$, the thinnest and the thickest SACL thickness of SACL in the via after the SACL remove can be expressed as

$$T_{\mathrm{SAC},L1} = T_{\mathrm{SAC},L0} - T_{\mathrm{SAC}}(1+\mathrm{OE}_{\mathrm{SR}}) * (1+U_{\mathrm{SR}})$$

and

$$T_{\mathrm{SAC},H1} = T_{\mathrm{SAC},H0} - T_{\mathrm{SAC}}(1+\mathrm{OE}_{\mathrm{SR}}) * (1-U_{\mathrm{SR}})$$

respectively.

During the trench-etching step, the SACL in via will be recessed continuously. Let $\mathrm{ER}_{\mathrm{TR}}$, $\mathrm{ER}_{\mathrm{SAC}}$, $U_{\mathrm{TR}}$, $U_{\mathrm{SAC}}$ be the etch rate of IMD, the etch rate of SACL, the etch rate uniformity of IMD, and the etch rate uniformity of SACL at the trench-etching step, respectively. Assuming the thickness of IMD is $T_D$ and the uniformity is $U_D$, the time to reach the targeted trench depth $T_{\mathrm{TR}}$ is $t_{\mathrm{TR}} = T_{\mathrm{TR}}/\mathrm{ER}_{\mathrm{TR}}$. The thinnest and the thickest SACL thickness in the via after trench etching become

$$T_{\mathrm{SAC,min}} = T_{\mathrm{SAC},L1} - t_{\mathrm{TR}} * \mathrm{ER}_{\mathrm{SAC}} * (1+U_{\mathrm{SAC}})$$

and

$$T_{\mathrm{SAC,max}} = T_{\mathrm{SAC},H1} - t_{\mathrm{TR}} * \mathrm{ER}_{\mathrm{SAC}} * (1-U_{\mathrm{SAC}})$$

respectively. It should be noted that the trench width ranges from the minimum design rule to several tens of microns; the three uniformity parameters, $U_{\mathrm{SR}}$, $U_{\mathrm{TR}}$, and $U_{\mathrm{SAC}}$, must take the microloading effect and the aspect-ratio-dependent-etching effect into consideration. The via height after trench etching depends on the IMD thickness and the trench depth. Because these two processes are performed in different tools, the within wafer uniformity map of both processes must be known to determine the minimum via height after trench etching. For the single wafer deposition tool and dry etching tool, the within uniformity always shows a radioactive pattern. Two possible combinations are considered. In the first case, a high IMD deposition rate re-

TABLE I
PROCESS PARAMETERS USED IN THE PROPOSED CRITERIA. VALUES LISTED IN THE FIRST ROW ARE USED AS THE CENTRAL CONDITION FOR PROCESS SENSITIVITY ANALYSIS (SECTION III). VALUES LISTED IN THE SECOND ROW AND THIRD ROW ARE USED IN DEVELOPING THE GLOBAL WIRING AND LOCAL WIRING PROCESSES, RESPECTIVELY (SECTION IV). TBA: PARAMETERS TO BE ADJUSTED SUCH THAT THE CRITERIA ARE SATISFIED

| | $T_{SAC,L0}$ (nm) | $T_{SAC,H0}$ (nm) | $T_{SAC}$ (nm) | $OE_{SR}$ (%) | $U_{SR}$ (%) | $T_D$ (nm) | $U_D$ (%) | $T_{TR}$ (nm) | $ER_{TR}$ (nm/min) | $U_{TR}$ (%) | $ER_{SAC}$ (nm/min) | $U_{SAC}$ (%) | $T_{FA}$ (nm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Sensitivity Analysis | TBA | TBA | 140 | 20 | 10 | 1500 | 10 | 750 | 800 | 10 | 160 | 10 | 150 |
| Global Wiring | 456 | 755 | 140 | TBA | 12 | 1550 | 9 | 810 | 750 | 13 | 167 | 12 | 240 |
| Local Wiring | 257 | 446 | 60 | TBA | 12 | 820 | 9 | 380 | 750 | 9 | 167 | 10 | 100 |

gion is in conjunction with a low IMD etch rate region and the low IMD deposition rate region is in conjunction with the high IMD etch rate region. The two processes are with negative association and the lowest via occurs at the region of the thinnest IMD region. The minimum via height can be expressed as

$$H_{\mathrm{VIA,min}} = T_D(1-U_D) - T_{\mathrm{TR}}(1+U_{\mathrm{TR}}) - T_{\mathrm{FA}} \quad (1)$$

where $T_{\mathrm{FA}}$ is the facet height at the via corner.

Another possible combination is that the high IMD deposition rate region is in conjunction with the high IMD etch rate region and the low IMD deposition rate region is in conjunction with the low IMD etch rate region. The two processes are in positive association now. Although the lowest via in this case depends on the actual maps of both processes, it can be estimated to be the lower value of the following two regions:

1) high deposition rate and high etch rate

$$H_{\mathrm{VIA,min}} = T_D(1+U_D) - T_{\mathrm{TR}}(1+U_{\mathrm{TR}}) - T_{\mathrm{FA}} \quad (2a)$$

and

2) low deposition rate and low etch rate

$$H_{\mathrm{VIA,min}} = T_D(1-U_D) - T_{\mathrm{TR}}(1-U_{\mathrm{TR}}) - T_{\mathrm{FA}}. \quad (2b)$$

The criteria are now expressed as

$$\begin{aligned}\text{Criterion 1: } T_{\mathrm{SAC},L0} >& T_{\mathrm{SAC}}(1+\mathrm{OE_{SR}})*(1+U_{\mathrm{SR}}) \\ &+ t_{\mathrm{TR}}*\mathrm{ER_{SAC}}*(1+U_{\mathrm{SAC}}) \\ &>0\end{aligned}$$

$$\begin{aligned}\text{Criterion 2: } T_{\mathrm{SAC},H0} <& T_{\mathrm{SAC}}(1+\mathrm{OE_{SR}})*(1-U_{\mathrm{SR}}) \\ &+ t_{\mathrm{TR}}*\mathrm{ER_{SAC}}*(1-U_{\mathrm{SAC}}) \\ &- H_{\mathrm{VIA,min}}\end{aligned}$$

or

$$\begin{aligned}\text{Criterion 1: } \Delta L =& T_{\mathrm{SAC},L0} - T_{\mathrm{SAC}}(1+\mathrm{OE_{SR}}) \\ &*(1+U_{\mathrm{SR}}) - t_{\mathrm{TR}}*\mathrm{ER_{SAC}} \\ &*(1+U_{\mathrm{SAC}}) > 0\end{aligned}$$

$$\begin{aligned}\text{Criterion 2: } \Delta H =& T_{\mathrm{SAC},H0} - T_{\mathrm{SAC}}(1+\mathrm{OE_{SR}}) \\ &*(1-U_{\mathrm{SR}}) - t_{\mathrm{TR}}*\mathrm{ER_{SAC}} \\ &*(1-U_{\mathrm{SAC}}) - H_{\mathrm{VIA,min}} < 0.\end{aligned}$$

These two criteria link all of the process parameters related to the SACL process together.

## III. PROCESS SENSITIVITY ANALYSIS

The criteria $\Delta L > 0$ and $\Delta H < 0$ can be used to analyze the sensitivity of process parameters on the process window of the VF scheme. They can also be used to determine the most critical parameters to improve the process window. The central condition of all of the process parameters used in this section is listed in the first row of Table I. In this analysis, positive association between IMD thickness and trench-etch rate are assumed. Therefore, the $H_{\mathrm{VIA,min}}$ is obtained by the smaller value of (2a) and (2b). Because the $T_{\mathrm{TR}}$ is around half of the $T_D$, the $H_{\mathrm{VIA,min}}$ is usually determined by (2b).

The impact of the targeted trench depth was examined at first. In this examination, the targeted trench depth was changed from 650 to 900 nm, while the other parameters were kept at the central condition. Fig. 3 shows the calculated $T_{\mathrm{SAC},L0}$ and $T_{\mathrm{SAC},H0}$ as a function of the ratio of the targeted trench depth to the IMD thickness ($T_{\mathrm{TR}}/T_D$) such that the criteria are satisfied. The $R_{\mathrm{SAC}}$, which is defined as $T_{\mathrm{SAC},H0} - T_{\mathrm{SAC},L0}$, is also shown in the figure. It is observed that the $T_{\mathrm{SAC},L0}$ increases and the $T_{\mathrm{SAC},H0}$ decreases as the $T_{\mathrm{TR}}/T_D$ ratio increases. The $R_{\mathrm{SAC}}$ decreases from 550 to 310 nm as the $T_{\mathrm{TR}}/T_D$ ratio increases from 0.47 to 0.60, respectively. This result indicates that the process window can be greatly improved by reducing the trench depth to the IMD thickness ratio. It is known that the design rule of trench depth is determined mainly by the electrical performance and the metal reliability. The above indication suggests that under the circumstance that electrical considerations are satisfied, a thinner metal layer results in a wider SACL process window. In fact, a thinner metal layer is also preferred to lower the intraline capacitance.

Fig. 4 shows the $T_{\mathrm{SAC},L0}$ and $T_{\mathrm{SAC},H0}$ as a function of the etch rate selectivity of IMD to SACL ($\mathrm{SE} = \mathrm{ER_{TR}}/\mathrm{ER_{SAC}}$) during the IMD etching step. The other parameters were kept at the central condition. It is observed that by decreasing the SE from 6 to 3, both $T_{\mathrm{SAC},L0}$ and $T_{\mathrm{SAC},H0}$ were reduced by a similar amount such that the $R_{\mathrm{SAC}}$ is decreased a little bit. As the SE approaches one, the required SACL thickness increases and the $R_{\mathrm{SAC}}$ decreases dramatically. One may expect a low SE such that the possibility of fence formation is lower. However, a lower SE requires thicker SACL in via and a smaller SACL thickness difference between isolated via and dense via; otherwise, the capping layer at the bottom of the dense via may be

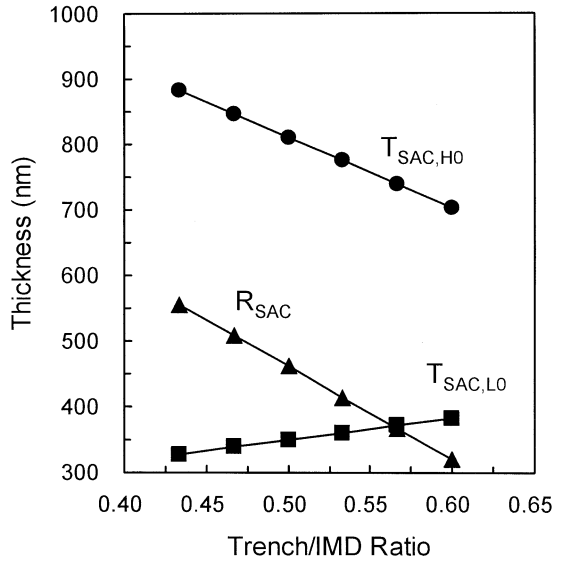


Fig. 3. The calculated $T_{\mathrm{SAC},L0}$, $T_{\mathrm{SAC},H0}$, and $R_{\mathrm{SAC}}$ as a function of the ratio of the targeted trench depth to the IMD thickness $(T_{\mathrm{TR}}/T_D)$. The other process parameters are listed in the first row of Table I.

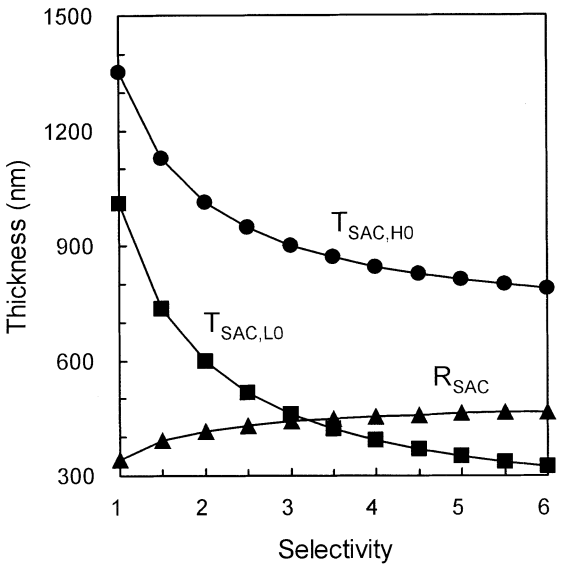


Fig. 4. The calculated $T_{\mathrm{SAC},L0}$, $T_{\mathrm{SAC},H0}$, and $R_{\mathrm{SAC}}$ as a function of the etch rate selectivity between IMD and SACL at trench-etch step (SE). The other process parameters are listed in the first row of Table I.

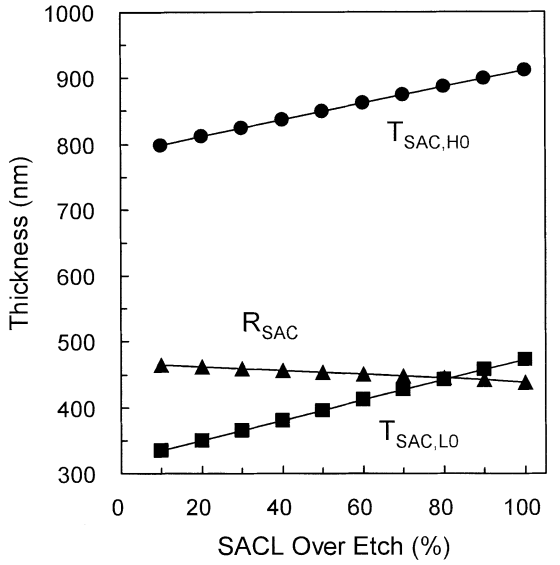


Fig. 5. The calculated $T_{\mathrm{SAC},L0}$, $T_{\mathrm{SAC},H0}$, and $R_{\mathrm{SAC}}$ as a function of the overetching percentage at the SACL breakthrough step $(\mathrm{OE}_{\mathrm{SR}})$.

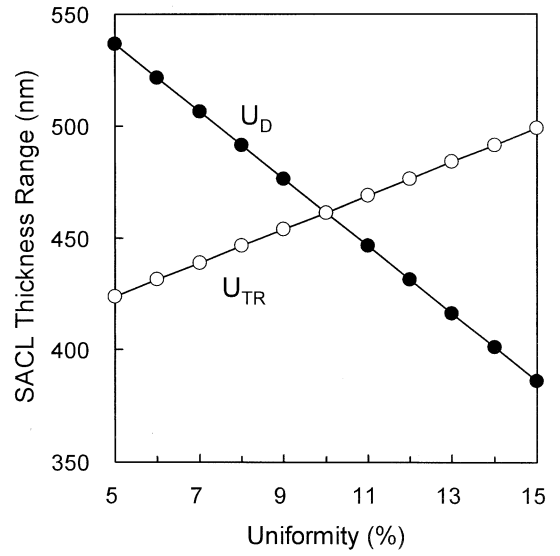


Fig. 6. Calculated $R_{\mathrm{SAC}}$ as a function of the IMD deposition rate uniformity $(U_D)$ or the trench-etch rate uniformity $(U_{\mathrm{TR}})$.

etched through. This means that low SE is not necessarily the best choice to expand the SACL process window.

The effect of $\mathrm{OE}_{\mathrm{SR}}$ is shown in Fig. 5. The $T_{\mathrm{SAC},L0}$ and $T_{\mathrm{SAC},H0}$ increase with the increase of $\mathrm{OE}_{\mathrm{SR}}$, while the $R_{\mathrm{SAC}}$ is almost unchanged. This feature implies that if the SACL thickness in via is too thick, a suitable $\mathrm{OE}_{\mathrm{SR}}$ can be adapted to reduce the SACL thickness such that the criteria are satisfied as long as the SACL thickness between isolated and dense vias is smaller than the $R_{\mathrm{SAC}}$. Any SACL process resulting in a suitable thickness range with sufficient SACL thickness can be used for the SACL process. Since higher SE results in a thinner $T_{\mathrm{SAC},L0}$ and $T_{\mathrm{SAC},H0}$ as shown in Fig. 4, medium SE combined with suitable $\mathrm{OE}_{\mathrm{SR}}$ allows more SACL materials and wider SACL coating conditions.

Fig. 6 shows the effect of $U_D$ and $U_{\mathrm{TR}}$ on the $R_{\mathrm{SAC}}$. In our experience, these two parameters ranges from 5% to 15% and depend on equipment and recipe. It is known that $U_D$ affects the criterion of $\Delta H < 0$ through the $H_{\mathrm{VIA,min}}$ but does not affect the criterion of $\Delta L > 0$. Therefore, poor $U_D$ results in higher $H_{\mathrm{VIA,min}}$ which in turn results in smaller $R_{\mathrm{SAC}}$ assuming (2b). On the contrary, poor $U_{\mathrm{TR}}$ results in lower $H_{\mathrm{VIA,min}}$ and larger $R_{\mathrm{SAC}}$. These results indicate that from the viewpoint of SACL process window, the $U_D$ is more important than the $U_{\mathrm{TR}}$ because poor $U_D$ reduces the SACL process window but poor $U_{\mathrm{TR}}$ increases the SACL process window. Certainly, poor $U_{\mathrm{TR}}$ is not preferred because it will result in higher trench depth variation. The effect of $U_{\mathrm{SR}}$ and $U_{\mathrm{SAC}}$ is shown in Fig. 7. The $R_{\mathrm{SAC}}$ decrease with the increase of $U_{\mathrm{SR}}$ and $U_{\mathrm{SAC}}$. However, the decrease of $R_{\mathrm{SAC}}$ is only 30 nm. It is thus determined that the $U_{\mathrm{SR}}$ and $U_{\mathrm{SAC}}$ are not important in the SACL process.

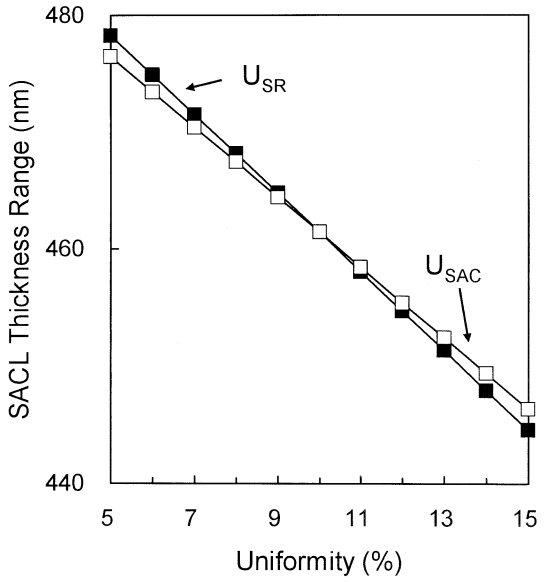


Fig. 7. Calculated $R_{\mathrm{SAC}}$ as a function of the SACL etch rate uniformity $(U_{\mathrm{SR}})$ at SACL breakthrough or the SACL etch rate uniformity at trench-etch step $(U_{\mathrm{SAC}})$.

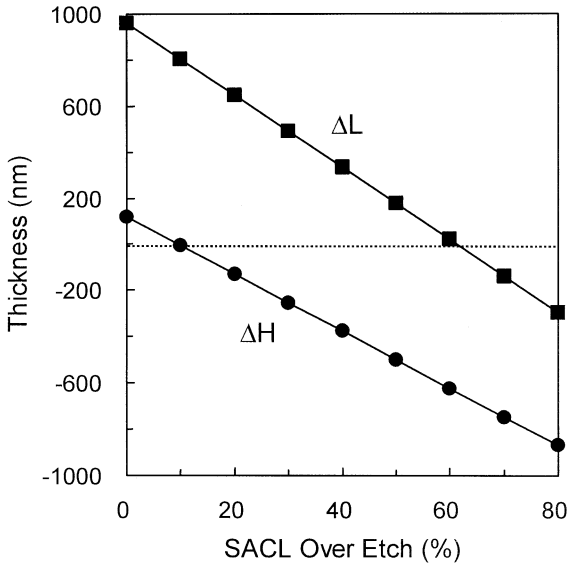


Fig. 8. Calculated $\Delta H$ and $\Delta L$ of the example of global wiring as a function of the overetching percentage at the SACL breakthrough step $(\mathrm{OE_{SR}})$. The other process parameters are listed in the second row of Table I.

Since the SACL layer is used temporarily and it does not affect the remaining processes after trench etching, there is a wide freedom to adjust the thickness of SACL in via ($T_{\mathrm{SAC},L0}$ and $T_{\mathrm{SAC},H0}$) by choosing suitable SACL material and/or by tuning the coating recipe such that the above criteria ($\Delta L > 0$ and $\Delta H < 0$) are satisfied. On the other hand, an acceptable trench-etching recipe must satisfy many requirements other than those considered in the criteria—dimension control, profile control, etch rate, and good uniformity for example. Minimizing the microloading effect and the aspect-ratio-dependent-etching effect is another requirement in the case of without etch-stop-layer. Therefore, the flexibility to change the trench-etching recipe is much lower than that to change the SACL coating recipe. Based on these concepts, a four-step procedure is proposed to develop

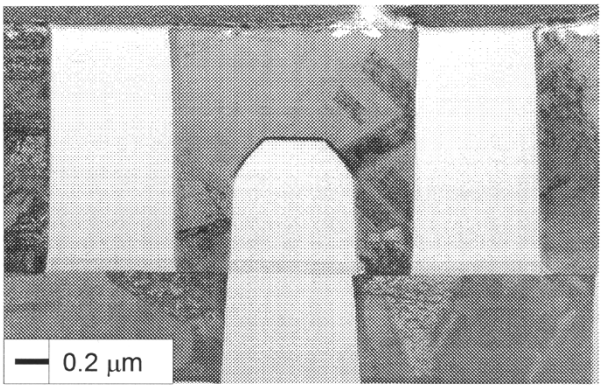


Fig. 9. Cross-sectional TEM micrograph of the global wiring via chain fabricated by the VF scheme with SACL process. The via diameter is 0.27 $\mu$m at via bottom. The "fence" free profile was obtained.

the SACL process: 1) to find an acceptable trench-etching recipe which satisfies all of the specification of trench etching; 2) to characterize the parameters related to the SACL process; 3) to calculate the lower bound and upper bound of SACL thickness in via; and 4) to find the suitable SACL material, coating recipe, and $\mathrm{OE_{SR}}$ such that the criteria are satisfied.

## IV. Applications of the Criteria

Two examples are presented in this section to demonstrate the application of the proposed criteria. The first example is a double-layer global wiring process with 0.7-$\mu$m metal pitch and 0.27-$\mu$m via diameter. The second example is a double-layer local wiring process with 0.36-$\mu$m metal pitch and 0.16-$\mu$m via diameter. Both processes were developed for the multilevel interconnect at the 0.13-$\mu$m technology node and beyond. The design rules and the characterized process parameters used in these two examples are listed in the second and third rows of Table I for global wiring and local wiring, respectively.

### *A. Global Wiring: 0.70-$\mu$m Metal Pitch/0.27-$\mu$m Via*

After the CMP of the underlayer Cu interconnect, an 85-nm-thick SiN layer was deposited as a dielectric barrier of the underlying Cu wires. It also serves as an etch-stop layer of via patterning. Fluorinated silica glass (FSG) of 1.55 $\mu$m thick was deposited in an HDPCVD system as the IMD followed by a 56-nm-thick dielectric antireflection layer (DARL) deposition. No etch-stop-layer for trench etching was used. The via was patterned through the whole IMD at first. The via diameter is 0.27 $\mu$m at via bottom. The SACL was then spin coated to a thickness of 140 nm at the blanket area. The thickest and the thinnest SACL in vias determined by scanning electron microscope (SEM) inspection are 755 and 456 nm, respectively. Since all parameters except the $\mathrm{OE_{SR}}$ are fixed, the only adjustable parameter is the $\mathrm{OE_{SR}}$. Fig. 8 shows the calculated $\Delta H$ and $\Delta L$ as a function of $\mathrm{OE_{SR}}$. It is observed that both criteria can be satisfied as the $\mathrm{OE_{SR}}$ ranging from 10% to 60%. Therefore, the $\mathrm{OE_{SR}}$ is determined to be 30% in real process. Fig. 9 shows the cross-sectional transmission electron microscope (TEM) micrograph of this double metal structure. Perfect dual damascene profile without "fence" was achieved. The cumulative probability of via resistance measured on via chain with 20 000 vias

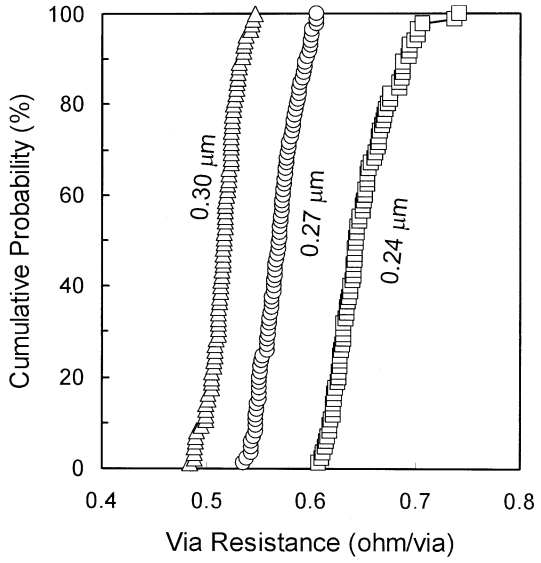


Fig. 10. The cumulative probability distribution of via resistance of the global wiring via chain with via diameters of 0.24, 0.27, and 0.30 $\mu$m. The low resistance, high yield, and tight distribution indicate that the process is well controlled.

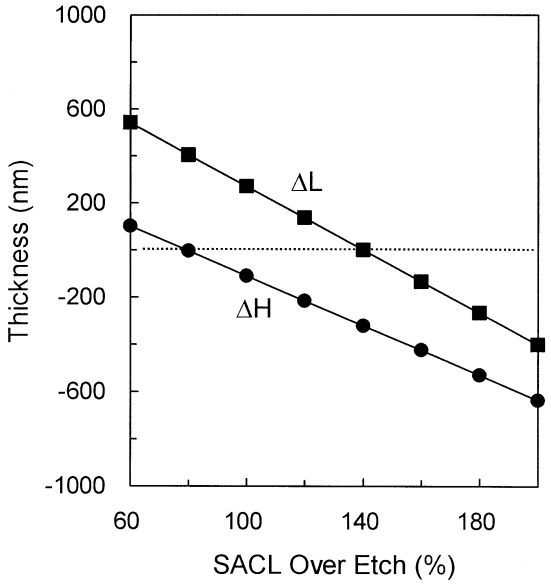


Fig. 11. Calculated $\Delta H$ and $\Delta L$ of the example of local wiring as a function of the overetching percentage at the SACL breakthrough step $(\mathrm{OE_{SR}})$. The other process parameters are listed in the second row of Table I.

is shown in Fig. 10. The low via resistance, 100% yield, and tight distribution indicate the process is well controlled.

### *B. Local Wiring: 0.36-$\mu$m Metal Pitch/0.16-$\mu$m Via*

The SiN capping layer on the underlying Cu wires is 50 nm thick. The IMD is still FSG but the thickness is 820 nm thick now. A 56-nm-thick DARL was still used to reduce the reflectivity. No etch-stop-layer for trench etching was used again. The diameter of via at bottom is 0.16 $\mu$m. The SACL was spin coated to a thickness of 60 nm at the blanket area. The thickest and the thinnest SACL in via determined by SEM inspection are 446 and 257 nm, respectively. Fig. 11 shows the calculated $\Delta H$ and $\Delta L$ as a function of $\mathrm{OE_{SR}}$. It is observed that an $\mathrm{OE_{SR}}$ of more than 80% is required to let $\Delta H < 0$, while an $\mathrm{OE_{SR}}$ of less than 140% is required to keep $\Delta L > 0$ . Because the etch rate of PR is close to that of SACL, it is impossible to breakthrough the SACL after PR patterning with such a heavy overetching. A blanket etching back of SACL to a 100% $\mathrm{OE_{SR}}$ was chosen. Fig. 12 shows the cross-sectional TEM micrograph of this double metal structure. Perfect dual damascene profile without "fence" was achieved again. The cumulative probability of via resistance measured on via chain with 20 000 vias was shown in Fig. 13. The via resistance is lower than 1.5 ohm/via and the yield is 100%. These results not only confirm the validity of the proposed criteria but also indicate that the SACL process can be used with the VF scheme even beyond 0.13-$\mu$m technology node.

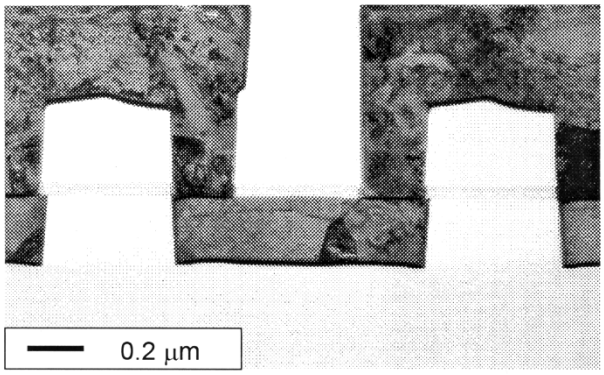


Fig. 12. Cross-sectional TEM micrograph of the local wiring via chain fabricated by the VF scheme with SACL process. The via diameter is 0.16 $\mu$m at via bottom. The "fence" free profile was obtained.

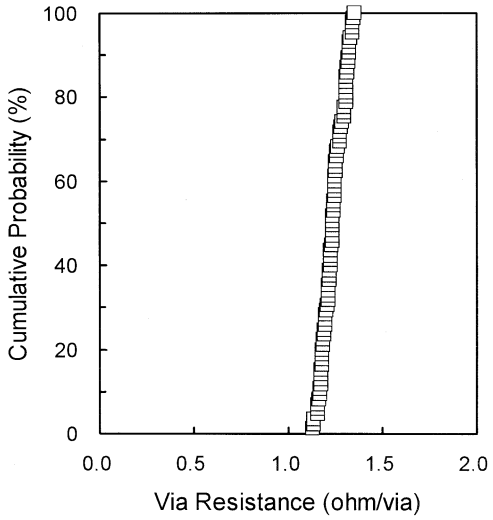


Fig. 13. Cumulative probability distribution of via resistance of the local wiring via chain. The low resistance, high yield, and tight distribution indicate that the process is well controlled.

## V. Conclusion

The SACL process had been proposed to be used in the VF scheme to protect the capping layer at the via bottom during trench etching for several years. It is usually criticized that the process window is hard to identify. In this work, we proposed two criteria to link all process parameters related to the SACL

process. According to the criteria, process parameters sensitivity to the SACL process window can be evaluated. It is suggested that the combination of shallow trench depth and medium etch rate selectivity between IMD and SACL material is preferred. The SACL thickness in via can be adjusted by adjusting the overetching percentage at the SACL remove step such that the criteria are satisfied. The validity and the application of the proposed criteria are verified by two double metal examples. Via chains with via size of 0.27 and 0.16 $\mu$m at via bottom were fabricated. Perfect profile and yield were achieved.

To conclude, the process window of the SACL process can be evaluated accurately. A robust SACL process can be designed even beyond 0.13-$\mu$m technology node.

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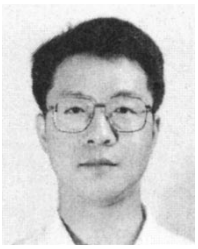

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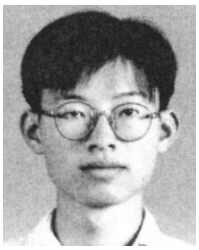

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