Methodology on Extracting Compact Layout Rules for Latchup Prevention in Deep-Submicron Bulk CMOS Technology

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***Abstract*—An experimental methodology to find area-efficient compact layout rules to prevent latchup in bulk complimentary metal–oxide–semiconductor (CMOS) integrated circuits (ICs) is proposed. The layout rules are extracted from the test patterns with different layout spacings or distances. A new latchup prevention design by adding the additional internal double guard rings between input/output cells and internal circuits is first reported in the literature, and its effectiveness has been successfully proven in three different bulk CMOS processes. Through detailed experimental verification including temperature effect, the proposed methodology to extract compact layout rules has been established to save silicon area of CMOS ICs but still to have high enough latchup immunity. This proposed methodology has been successfully verified in a 0.5-μm nonsilicided, a 0.35-μm silicided, and a 0.25-μm silicided shallow-trench-isolation bulk CMOS processes.**

***Index Terms*—Design rule, guard ring, I/O cell, latchup, pickup.**

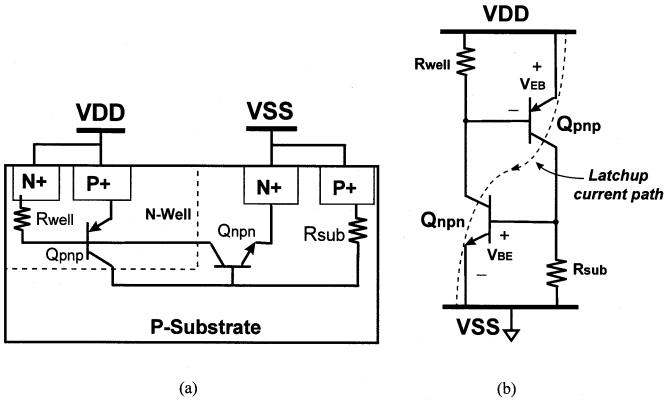

Fig. 1. (a) Device cross-sectional view and (b) equivalent circuit of latchup structure in a p-substrate bulk CMOS technology.

I. Introduction

LATCHUP in bulk complimentary metal–oxide–semiconductor (CMOS) integrated circuits (ICs) is formed by the parasitic p–n–p–n structure between V_{DD} and V_{SS} of CMOS circuits [1]–[3]. This parasitic structure inherently exists in the bulk CMOS technology. When the parasitic p–n–p–n structure is triggered to cause latchup, it generates a low-impedance path from V_{DD} to V_{SS} and a high current to often burn out the chip. The device cross-sectional view of a latchup path in a p-substrate bulk CMOS technology is shown in Fig. 1(a), where the first-order equivalent circuit of a latchup path is illustrated in Fig. 1(b). The latchup equivalent circuit is formed by a vertical p–n–p bipolar junction transistor (BJT) (Qpnp) coupled with a lateral n–p–n BJT (Qnpn). When one of the BJTs is turned on, the mechanism of positive feedback regeneration in the latchup structure will be initiated [4], [5]. If the product of beta gains of these two BJTs can be kept greater than one, the p–n–p–n structure will hold in a stable latching state [1]–[5]. To prevent the occurrence of latchup in CMOS ICs, some advanced process technologies (such as the epitaxial substrate [6], retrograde well [7], trench isolation [8], or silicon-on-insulator) have been reported to increase holding voltage of the parasitic p–n–p–n structures. Although such advanced techniques can effectively solve the latchup issue in CMOS ICs, the production cost of CMOS ICs with such advanced techniques becomes more expensive. Thus, the most consumer IC products are still manufactured by bulk CMOS processes. In the bulk CMOS processes, the latchup issue is mainly prevented by guard rings which have been specially specified in the design rules of a CMOS process. The wider guard rings used to surround the input/output (I/O) devices in I/O cells of CMOS ICs generally cause a higher latchup immunity, but they also occupy a larger layout area.

With more complex functions and circuit blocks integrated into a single chip, a high-integration CMOS IC often has the pin count of several hundreds. In the communication ICs or chip set ICs, more I/O pins are designed to provide the desired system connections for function applications. In such high-pin-count ICs, the whole chip size is often decided by the pad-limited effect but no longer the core-limited effect [9]. Therefore, the pad pitch of I/O cells is critically limited to reduce the total chip size of a high-pin-count CMOS IC. To further reduce the pad pitch for high-pin-count CMOS ICs, the staggered bond pad has been widely used in CMOS ICs to reduce the whole chip size [9]. With the staggered bond pad design, layout pitch for a corresponding I/O cell has been scaled down to only $\sim$50 μm.

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With such a narrow layout pitch, the cell height of an I/O cell including output buffer circuits (or ESD protection circuits) and latchup guard rings becomes much longer. The much longer cell height of the I/O cells causes an increase on the whole chip size. Therefore, compact layout rules for I/O cells to prevent latchup are highly demanded by high-pin-count CMOS ICs.

In this paper, a brief overview on the traditional methods to find design rules for latchup prevention in CMOS technology and the latchup test standards are described in Section II. In Section III, a new methodology to extract compact layout rules for latchup prevention is therefore proposed to save chip size [10], [11]. More than ten testchips with different latchup test structures have been drawn and fabricated in 0.5-μm nonsilicided, 0.35-μm silicided, and 0.25-μm silicided shallow-trench-isolation (STI) bulk CMOS processes. These testchips are assembled within the DIP-40-pin package for experimental measurement. These latchup test structures to extract compact layout rules are designed with consideration on real circuit operating conditions in CMOS ICs. The experimental results have been measured and compared in Section IV. An experimental setup to observe latchup occurrence in time domain, during the triggering of the applied trigger current, is also first demonstrated in this work.

II. Design Rules and Latchup Test

In CMOS circuits, the latchup p–n–p–n path exists from the source (p+ diffusion connected to V_{DD}) of a PMOS, through the n-well and p-substrate, to the source (n+ diffusion connected to V_{SS}) of an NMOS. Therefore, there are many parasitic p–n–p–n paths existing in CMOS circuits, because CMOS logics always have many PMOS devices connected to V_{DD} and NMOS devices connected to V_{SS}. If one of such parasitic p–n–p–n path between V_{DD} and V_{SS} is firing, it causes the latchup problem to burn out the CMOS IC. Latchup can occur at I/O cells or at internal circuits of a CMOS IC because the parasitic latchup p–n–p–n paths exist in both I/O cells and internal circuits of a CMOS IC. In bulk CMOS technology, latchup immunity can be improved by some advanced CMOS processes [1]–[3], [6]–[8]. But, with consideration of fabrication cost, latchup prevention in most commercial IC products is achieved by adding the guard rings in I/O cells and placing the substrate/well pickups in internal circuits. For a given CMOS process, the spacing or distance on the latchup guard rings and pickups has to be specified in the design rules.

A. Latchup in Internal Circuits

A typical layout example of an inverter in digital internal circuits is shown in Fig. 2, where the n-well and p-substrate pickups are added into the layout to increase latchup immunity of CMOS circuits. The latchup path, from the source (p+ diffusion) of PMOS to the source (n+ diffusion) of NMOS, is also indicated in Fig. 2 by an arrow. The n-well pickups are formed by the n+ diffusions drawn in n-well and directly connected to V_{DD}. The p-substrate pickups are formed by the p+ diffusions drawn in p-substrate and directly connected to V_{SS}. Such n-well (p-substrate) pickups are often placed under V_{DD} (V_{SS}) power rail of a core cell to save cell layout area.

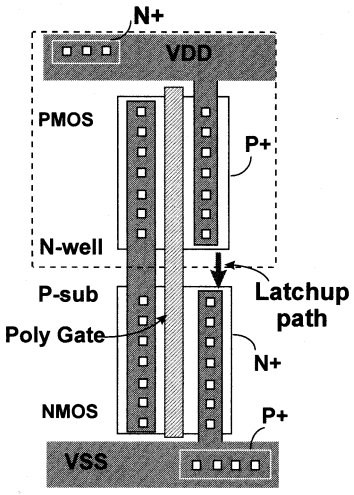


Fig. 2. Layout example of an inverter in internal circuits of a CMOS IC by using the n-well or p-substrate pickups to prevent latchup.

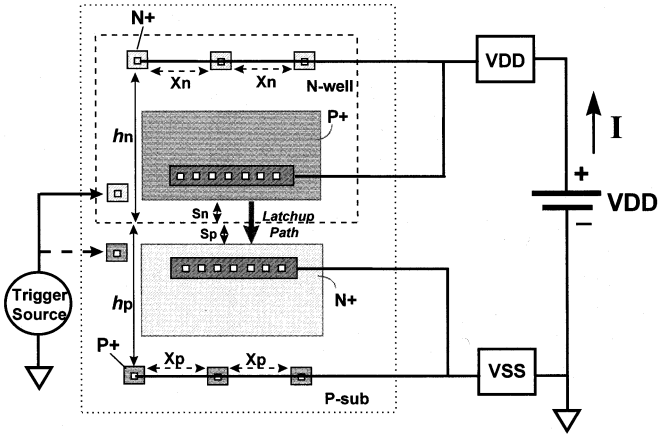


Fig. 3. The typical latchup test structure to find the layout rules on the substrate and well pickups for use in the layout of internal circuits of CMOS IC.

To define the latchup layout rules in a CMOS process, some test structures with different layout spacings have been used to investigate latchup immunity [12]–[17]. The typical latchup test structure to define layout rules on the n-well or p-substrate pickups for internal core circuits is shown in Fig. 3 [12], where the trigger nodes are drawn in the p-substrate or the n-well of the test structure. The test structures are drawn with different distances (Xp, Xn) between two adjacent pickups, or with different distances (hp, hn) from the pickups to the n-well edge. By applying different trigger current or voltage into the trigger nodes of test structure, where the p–n–p–n path is biased at a desired V_{DD} voltage level, the threshold trigger current to initiate latchup occurrence in the test structure can be found. When latchup is firing by the trigger current at the trigger node, the V_{DD} voltage level will be pulled down to near the holding voltage of p–n–p–n path. To avoid the test structure being burned out by the high latchup current during latchup triggering test, a resistor of $\sim$100 Ω is suggested for between V_{DD} and the anode of p–n–p–n path. In general, a trigger current of only several hundreds of microamperes can trigger on latchup path in such test structures in a bulk CMOS process. Although the critical (threshold) value of the trigger

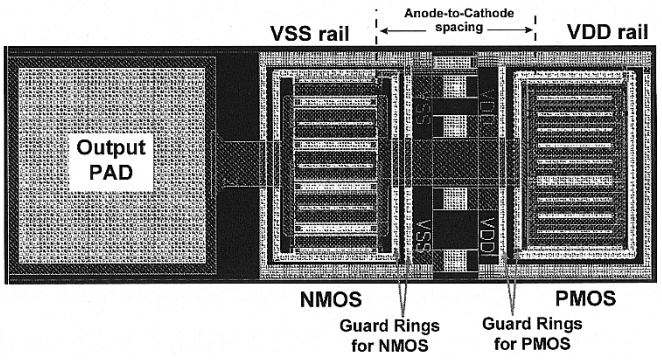


Fig. 4. Layout example of an inverter output buffer in the I/O cell with double guard rings to prevent latchup in a 0.5-μm nonsilicided bulk CMOS process.

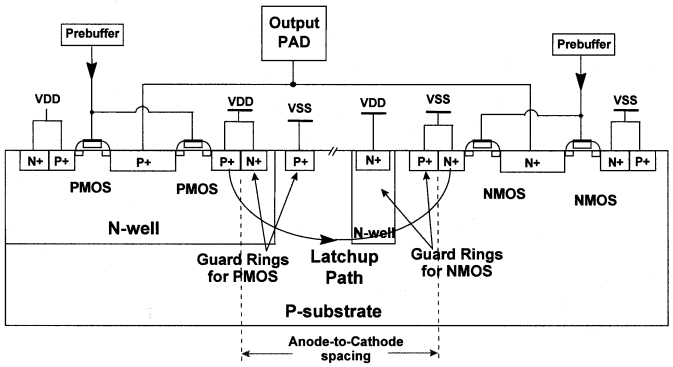


Fig. 5. Cross-sectional view of using double guard rings to block the latchup path in an I/O cell.

current to cause latchup in test structures can be found, this critical trigger current has no relation to the real substrate or well current when CMOS ICs are in the normal circuit operation. Therefore, some empirical layout rules are specified from experience to prevent latchup in the core circuits of CMOS ICs. For example, in a 0.5-μm nonsilicided (0.35-μm silicided) bulk CMOS process, the maximum distance between every two pickups in p-substrate or n-well is specified as 40 μm (20 μm). By using such pickup rules to draw the internal circuit layout, the parasitic p–n–p–n paths in internal circuits are still sensitive to latchup.

B. Latchup in I/O Cells

The I/O cells, which are connected to the bond pads in CMOS ICs, are often triggered by external overshooting or undershooting voltage/current glitches. Therefore, the double guard rings are often specified in the design rules to prevent latchup in I/O cells. A typical layout example of an inverter output buffer in I/O cell is shown in Fig. 4, where the NMOS (also PMOS) is surrounded by two guard rings in the layout to avoid latchup occurrence on I/O cell. The cross-sectional view to indicate the latchup path in I/O cell and the double guard rings to prevent latchup is shown in Fig. 5. The test structure used to investigate the layout rules of double guard rings for I/O cells is shown in Fig. 6 [14]. The first guard ring (or called as base guard ring) of an NMOS is a p+ diffusion that surrounds the source of NMOS (n+ diffusion connected to V_{SS} in Fig. 5), and the second guard ring (called the collector guard

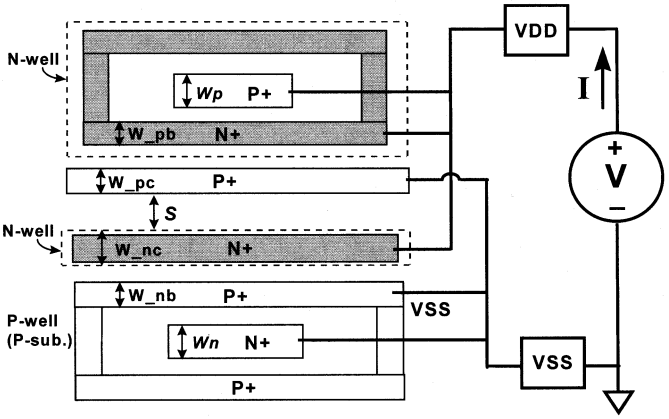


Fig. 6. Test structure to find the layout rules on the double guard rings for I/O cells in bulk CMOS processes.

ring) of the NMOS is an n+ diffusion that often surrounds the first guard ring. For an NMOS, the first guard ring is biased at V_{SS} and the second guard ring is biased at V_{DD} to prevent latchup. In the layout, an n-well region is often added under the second guard ring (n+ diffusion) of the NMOS to improve guard ring efficiency, because the n-well has a deeper junction depth ($\sim$2 μm) than that ($\sim$0.2 μm) of an n+ diffusion. The first guard ring of a PMOS is an n+ diffusion in n-well that surrounds the source of PMOS (p+ diffusion connected to V_{DD} in Fig. 5), and the second guard ring of the PMOS is a p+ diffusion in p-substrate that often surrounds the first guard ring. For a PMOS, the first guard ring is biased at V_{DD} and the second guard ring is biased at V_{SS} to prevent latchup.

The test structures, as shown in Fig. 6, are drawn with different widths of the guard rings or different distances between the guard rings to extract the layout rules for I/O cells. With suitable layout rules on the double guard rings to surround NMOS and PMOS in the I/O cell layout, the latchup p–n–p–n path in such an I/O cell is blocked by the guard rings. Therefore, the holding voltage of the parasitic p–n–p–n path in such an I/O cell can be increased up to greater than V_{DD} voltage level of the CMOS IC. With a holding voltage greater than V_{DD}, the parasitic p–n–p–n path in I/O cell becomes free to latchup. The test structures are often measured by a curve tracer to investigate the holding voltages of p–n–p–n paths, and therefore to find the suitable layout rules for I/O cells. For example, in the 0.5-μm nonsilicided and the 0.35-μm silicided bulk CMOS processes, the minimum width of the first and second guard rings to surround NMOS or PMOS was specified as 3 μm, and the maximum distance between the first and second guard rings was specified as 6 μm.

C. Latchup Test

To verify the latchup immunity of a CMOS IC, an overshooting (positive) current or undershooting (negative) current is applied to every I/O pin of a CMOS IC to investigate whether the latchup is fired, or not. The detailed latchup test procedure and specifications have been clearly specified in the EIA/JEDEC Standard no. 78 [18]. The schematic diagram to show such a latchup test on an output pin is illustrated in Fig. 7(a). If CMOS IC is fired into latchup by the trigger

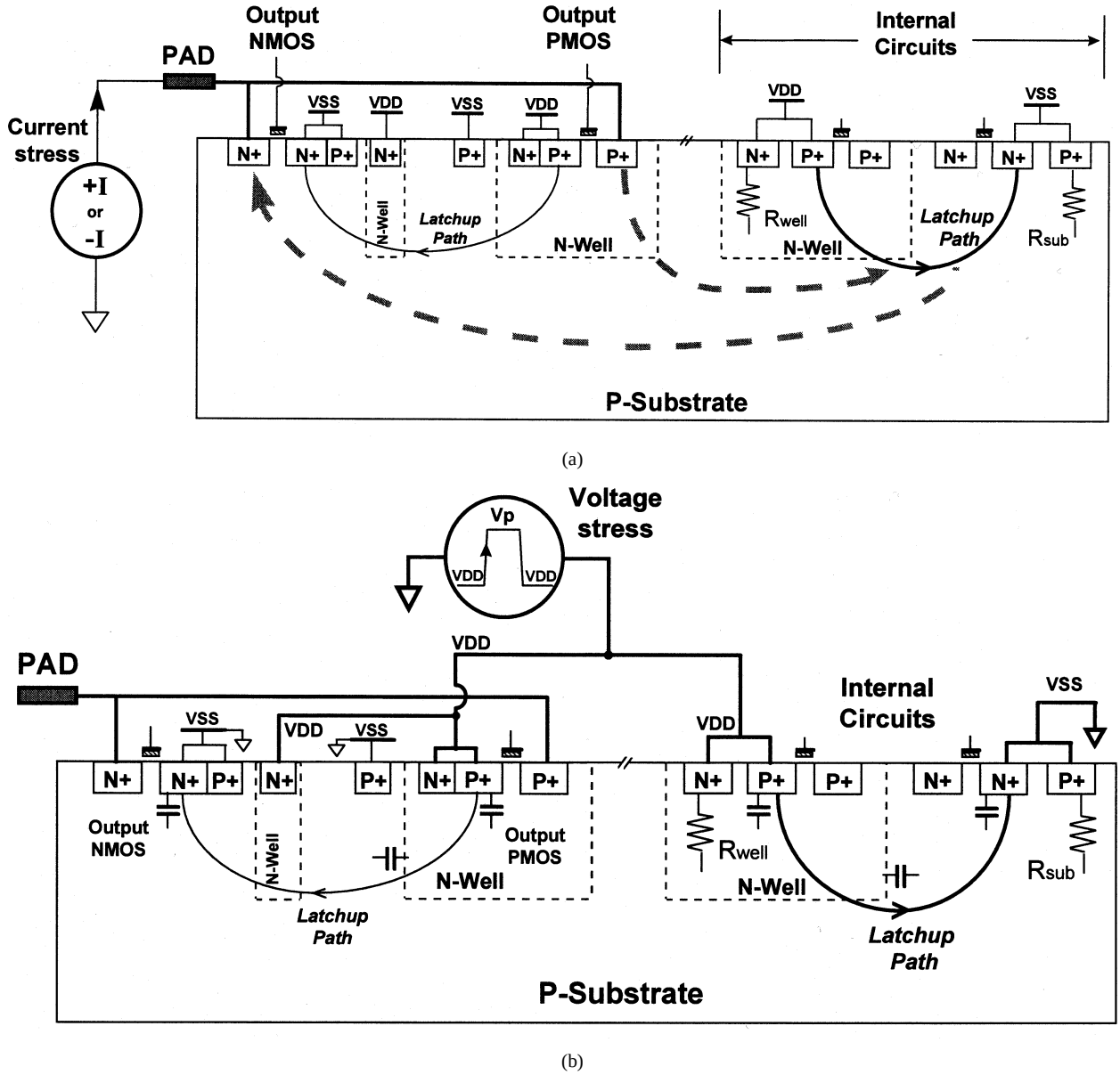


Fig. 7. Latchup test for a CMOS IC with: (a) the overshooting or undershooting trigger current at each I/O pin and (b) the voltage-transient trigger at the V_{DD} pin.

current applied on an I/O pin, the current flowing from V_{DD} power supply has an obvious increase. The obvious increase on the V_{DD} current can be detected by latchup tester to judge the occurrence of latchup.

In Fig. 7(a), the overshooting/undershooting trigger current on the pad is conducted into the drain regions of output devices. When the overshooting (undershooting) current is applied to I/O pin, the P+ drain/n-well (N+ drain/p-substrate) junction in output PMOS (NMOS) is forward biased to further generate the trigger current into the substrate. This substrate current, indicated by the gray dashed line in Fig. 7(a), can fire latchup paths in the I/O cell or in the internal circuits. To avoid latchup paths in CMOS ICs fired by the overshooting or undershooting current on the I/O pins, the double guard rings are often used to block the latchup path between output PMOS and NMOS in I/O cells, as those shown in Fig. 5.

The latchup in CMOS ICs is also sensitive to voltage transition on V_{DD} supply [19], [20]. To verify latchup immunity of CMOS ICs due to such a power-transient trigger, the test configuration is illustrated in Fig. 7(b). The trigger voltage is added onto the V_{DD} power supply of CMOS IC under test, and the current flowing from the V_{SS} pin of CMOS IC is monitored by latchup tester. The power-transition trigger voltage often generates the displacement current through junction capacitance into the n-well and p-substrate to fire latchup paths in CMOS IC. If CMOS IC is fired into latchup by the trigger voltage on V_{DD} pin, the current flowing out from V_{SS} pin has an obvious increase. The obvious increase on the V_{SS} current can be detected by a latchup tester to judge the occurrence of latchup. In general, CMOS ICs for consumer applications should not be triggered into latchup by a trigger current of ± 100 mA on the I/O pins or a trigger voltage of $1.5 \times V_{DD}$ on the V_{DD} pin [18].

III. Methodology to Extract Compact Layout Rules for Latchup Prevention

In the bulk CMOS ICs, the latchup prevention is generally achieved by adding the guard rings in I/O cells and placing the substrate/well pickups in internal circuits. However, the wider double guard rings in I/O cells and the more pickups in internal circuits often occupy more layout area in bulk CMOS IC. In this section, a new methodology to extract compact layout rules for I/O cells and the pickup rules for the internal circuits are proposed with consideration on the real circuit operations. Some test structures are therefore designed and drawn in the testchips to investigate the compact latchup rules for bulk CMOS ICs.

A. Layout Rules Design for I/O Cells

To avoid the latchup paths in I/O cells fired by the overshooting or undershooting current on I/O pins, the double guard rings are often used to block the latchup path between PMOS and NMOS in I/O cells, as in those shown in Figs. 4 and 5. One of the layout rules corresponding to the latchup immunity and the layout area of I/O cell is marked as the "anode-to-cathode spacing" between the sources of PMOS and NMOS in Figs. 4 and 5. One goal of this work is to find a compact anode-to-cathode spacing to save layout area of the I/O cell for high-pin-count CMOS ICs, but it can still sustain high latchup immunity for the CMOS ICs.

In such layout rule designs for the I/O cells, one set of I/O cells with double guard rings,a single guard ring, or no guard ring to surround the NMOS and PMOS in the I/O cells are drawn with different anode-to-cathode spacings from 5 to 60 μm to investigate latchup immunity in three different bulk CMOS processes. The CMOS processes used to fabricate latchup testchips are a 0.5-μm nonsilicided, a 0.35-μm silicided, and a 0.25-μm silicided shallow-trench-isolation (STI) bulk CMOS process. The PMOS and NMOS devices in I/O cells are drawn in the multiple-finger style with a finger length of 50 μm, and the total channel widths of NMOS and PMOS are kept at 500 μm. Each latchup guard ring (including the first or second guard rings) has a diffusion width of 3 μm to surround the device. The gate of PMOS is connected to V_{DD} and the gate of NMOS is connected to V_{SS} to turn themselves off for simplifying the current measurement during the latchup test. The layouts of I/O cells with double guard rings, a single guard ring, or no guard ring are shown in Fig. 8(a)–(c). An I/O cell with double guard rings to surround NMOS and PMOS, or with a wider anode-to-cathode spacing between NMOS and PMOS, will occupy more layout area to the I/O cell layout.

Because the I/O cells are bonded to the pins and connected to the external circuits for system applications, the overshooting or undershooting voltage/current glitches generated from system operation noise easily reach to the I/O cells. Therefore, the I/O cells need to have high latchup immunity in system applications. If the holding voltage of the parasitic p–n–p–n path in I/O cell is increased up to greater than V_{DD} by the compact guard ring design, the I/O cell can be free to latchup. In Section IV, the I–V characteristics of the latchup paths in these test structures with different guard ring designs are measured to find the holding voltage of the parasitic p–n–p–n path in I/O cells.

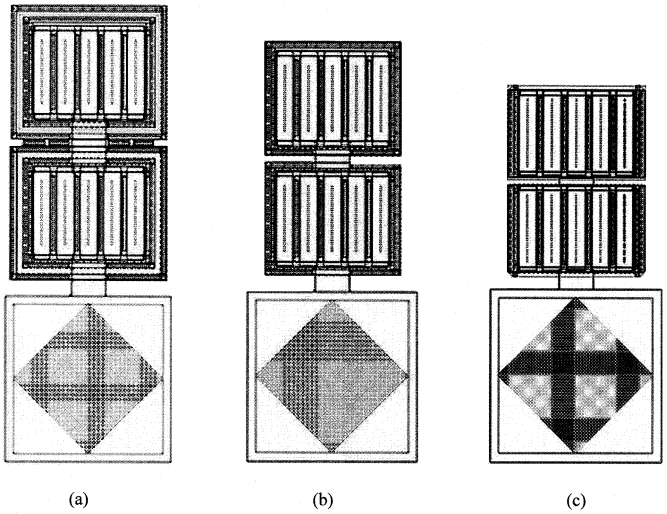


Fig. 8. The I/O cell layouts with: (a) double guard rings, (b) single guard ring, and (c) no guard ring, to investigate the compact layout rules for I/O cells.

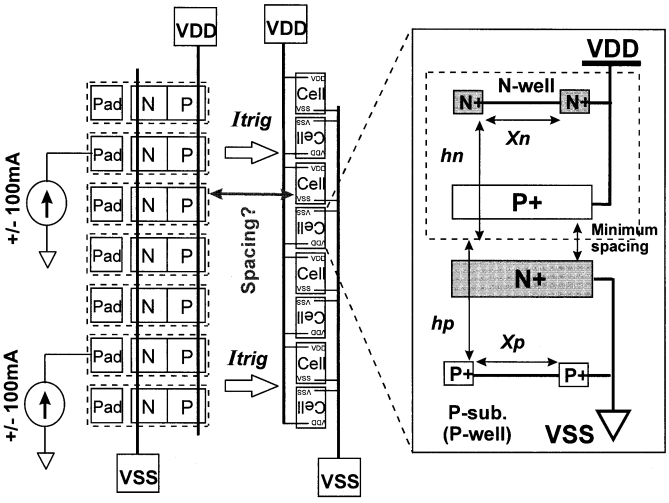


Fig. 9. New test method to find the layout spacing from the I/O cell to the internal circuits and the pickup distances in the internal circuits.

B. Layout Rules Design for Internal Circuits

The I/O cells can be free to latchup if suitable guard rings are added in I/O cells, but the internal circuits in bulk CMOS ICs are still sensitive to latchup. As shown in Fig. 7(a), the overshooting or undershooting trigger currents applied at I/O pins will generate a substrate current to cause latchup occurrence in internal circuits. To avoid the substrate current generated from I/O cells to fire latchup in internal circuits, the internal circuits should keep an enough distance away from the I/O cells. To investigate the suitable distance from the I/O cells to the internal circuits, a new test method is proposed in Fig. 9. The latchup sensor cells (enlarged in the box) are specially drawn and placed in parallel to I/O cells. The latchup sensor cells with specified pickup distances (Xn, hn, Xp, hp) are used to simulate the latchup structure in internal circuits. When the trigger current is applied at I/O pins, the V_{DD} that connected to the latchup sensor cells is monitored to judge whether latchup is triggered on, or not. The threshold trigger current applied at I/O cells to

fire latchup in internal circuits (simulated by the latchup sensor cells) can be measured by this new test method. The latchup sensor cells can be drawn with different pickup distances (Xn, hn, Xp, hp) to investigate how much trigger current at the I/O pin can fire latchup in the internal circuits under a specified distance from I/O cells to internal circuits. The latchup sensor cells, drawn with shorter distances between the n-well and p-substrate pickups, need a higher trigger current at I/O cells to cause latchup in internal circuits. By using this method, the design rules on the pickup distances (Xn, hn, Xp, hp) for internal circuits can be extracted more meaningfully to meet the real circuit operating condition in CMOS ICs.

To further reduce the distance between I/O cells and internal circuits to save layout area, the additional guard rings are proposed to be placed between the I/O cells and the internal circuits, such as those shown in Fig. 10(a) and (b). The additional p+ diffusion (n+ diffusion with n-well) guard ring is used to collect the hole (electron) currents, generated from I/O cells, in the substrate before they reach internal circuits to fire latchup. In order to find such important layout rules on the additional internal guard rings between I/O cells and internal circuits, some testchips are drawn and fabricated with different layout spacings from the I/O cells to the internal latchup sensor cells from 15 to 80 μm in bulk CMOS processes. The latchup sensor cells in these testchips are drawn with specified distances, such as the spacing from the pickups to the n-well edge of 40 (42.2) μm and the distance between two adjacent pickups of 20 (20) μm in 0.5 (0.35) μm bulk CMOS process. The I/O cells surrounded by double guard rings with an anode-to-cathode spacing of 25 μm are used in the testchips in 0.5-μm CMOS process. For the testchips in 0.35-μm CMOS process, the I/O cells are only surrounded by a single guard ring with an anode-to-cathode spacing of 14.4 μm. The width of the additional p+ internal guard ring is kept at 3 μm for the testchips in both 0.5- and 0.35-μm CMOS processes. The width of the additional n+ (with n-well) internal guard ring is drawn as 3.6 μm for the testchips in the 0.5-μm CMOS process but only 3.4 μm for the testchips in the 0.35-μm one. These I/O cells with their holding voltages larger than V_{DD} can be free to latchup (this will be proven by the measured results in Section IV). When the trigger current applied at I/O pins, the substrate current generated from I/O cells could fire latchup in internal circuits. The whole layout view of the testchips drawn in the 0.35-μm silicided bulk CMOS process are shown in Fig. 11(a) and (b). In Fig. 11(a), the testchip is used to extract the required spacing between I/O cells and internal circuits for latchup prevention without the additional internal guard ring. In Fig. 11(b), the testchip is drawn with the additional internal guard rings between I/O cells and internal circuits, which is also used to investigate the required spacing for latchup prevention. Another testchip is also drawn to investigate the width effect of the additional internal guard rings on latchup prevention.

IV. Experimental Results

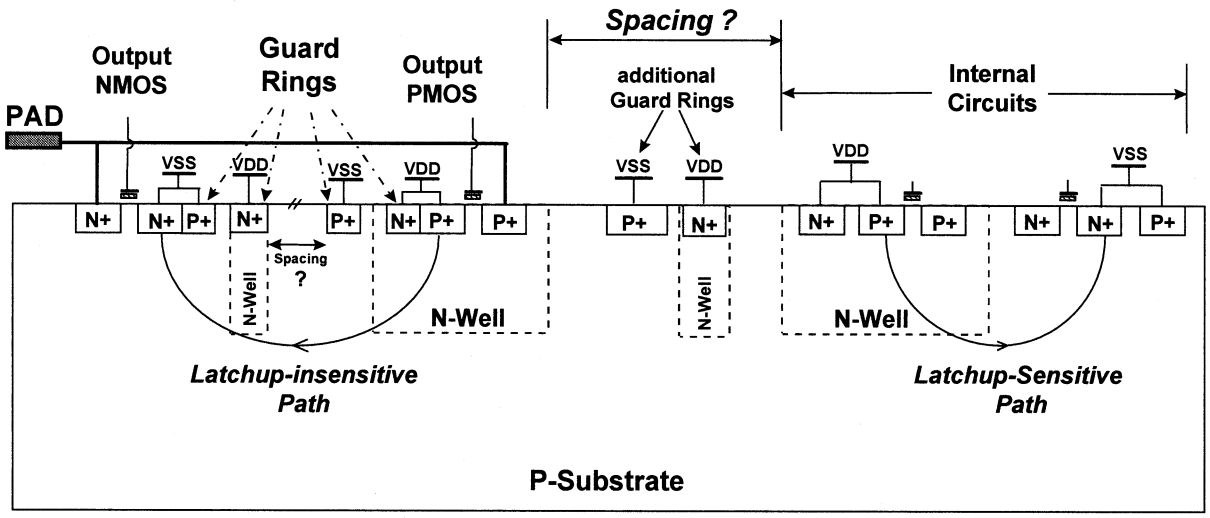
More than ten testchips including the I/O cells with double guard rings, single guard ring, or no guard ring, and the different pickup rules design for internal circuits had been fabricated in a 0.5-μm nonsilicided, a 0.35-μm silicided, and a 0.25-μm silicided STI bulk CMOS process. The I–V characteristics of these I/O cells and the trigger current to cause latchup occurrence in internal circuits are measured to investigate their latchup immunity.

A. I–V Characteristics of I/O Cells

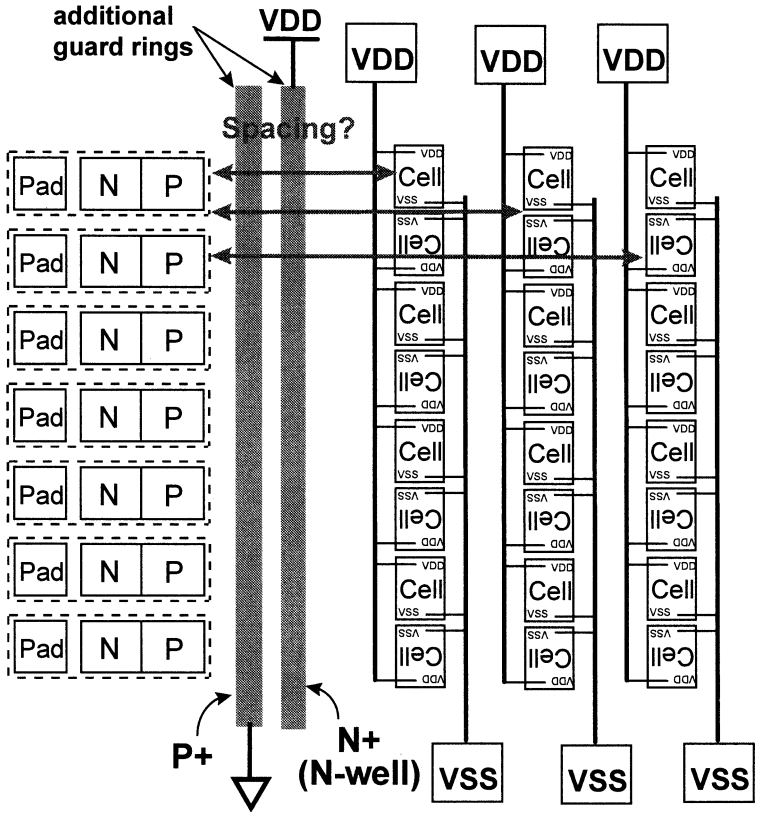
The I–V characteristics of I/O cells are measured by the *Tek*370A curve tracer. The holding voltages of these I/O cells are used to define their latchup hardness. If the holding voltage of I/O cells is greater than V_{DD}, the I/O cell is latchup-free. Moreover, a *ThermoChuck* system with a temperature range up to 200 °C and a temperature accuracy of $\pm$0.5 °C, produced by TEMPTRONIC Corporation is used to investigate latchup behaviors of the testchips in different temperatures.

1) I/O Cells in the 0.5-μm Nonsilicided Bulk CMOS Process: The latchup I–V characteristics traced from V_{DD} to V_{SS} of the I/O cell with double guard rings and an anode-to-cathode spacing of 22 μm at a temperature of 75 °C is shown in Fig. 12(a), where the I/O cell has a holing voltage of 7 V. The holding voltage is defined as the minimum voltage in the I–V curve of the holding region of latchup path [21]. The I/O cell with single guard ring and an anode-to-cathode spacing of 15 μm at a temperature of 100 °C is shown in Fig. 12(b), where the I/O cell has a holding voltage of 5 V. The I/O cell with no guard ring and an anode-to-cathode spacing of 20 μm at a temperature of 25 °C is shown in Fig. 12(c), where the I/O cell has a holding voltage of 2.5 V. In Fig. 13, the holding voltages of I/O cells with double guard rings, a single guard ring, or no guard ring under different anode-to-cathode spacings at the temperature of 25 °C are compared. The holding voltage is increased when the anode-to-cathode spacing increases. As shown in Fig. 13, the I/O cells with double guard rings or a single guard ring have holding voltages much greater than that with no guard ring, even if their anode-to-cathode spacings are much smaller than that with no guard ring. For example, the holding voltage of I/O cell with no guard ring and an anode-to-cathode spacing of 40 μm at 25 °C is 3.6 V, but the one with the single guard ring and an anode-to-cathode spacing of 15 μm is 5.5 V at the same temperature. The temperature effect on the holding voltage of I/O cells with different guard rings design is shown in Fig. 14. The increase of the operating temperature reduces the holding voltage of all I/O cells with different guard ring structures. For the I/O cell with no guard ring and an anode-to-cathode spacing (the "D" spacing in Fig. 14) of 40 μm, the holding voltage at 125 °C decreases to only 2.4 V. Thus, it will be more dangerous to suffer latchup at a high temperature in 5-V applications.

2) I/O Cells in the 0.35-μm Silicided Bulk CMOS Process: The I–V characteristics of I/O cells with double guard rings, a single guard ring, and no guard ring fabricated in 0.35-μm silicided bulk CMOS process are also measured. The measured I–V curves of I/O cells in a 0.35-μm silicided bulk CMOS process are similar to those shown in Fig. 12(a)–(c). In Fig. 15, the holding voltages of I/O cells with double guard rings, a single guard ring, and no guard ring under different anode-to-cathode spacings at a temperature of 25 °C are compared. As shown in Fig. 15, the I/O cells with double guard rings



(a)



(b)

Fig. 10. (a) Cross-sectional view and (b) schematic layout of the additional guard rings placed between I/O cells and internal circuits to avoid the trigger current applied at the I/O pins but to cause latchup in the internal circuits.

or a single guard ring have the holding voltages much greater than that with no guard ring, even if their anode-to-cathode spacings are smaller than that with no guard ring.

The relations between the holding voltage and anode-to-cathode spacing of the I/O cells with a single guard ring and no guard ring under different temperatures are shown in Figs. 16 and 17, respectively. From the above results, the I/O cell with a single guard ring and an anode-to-cathode spacing of only $\sim$10 μm can be latchup-free in the 3.3-V applications. The I/O cell with double guard rings has only a little improvement on the holding voltage than that with the single guard ring. Therefore, we suggest that the I/O cells in this 0.35-μm silicided CMOS process drawn with only a single guard ring are enough to prevent latchup in I/O cells. With only a single guard ring and a smaller anode-to-cathode spacing of 10 μm to draw the I/O cell, the layout area of such latchup-free I/O cell can be significantly reduced. In Fig. 17, where the I/O cell has no guard ring, a anode-to-cathode spacing of at least 40 μm is needed to provide a holding voltage larger than 3.3 V at a temperature of 125 °C.

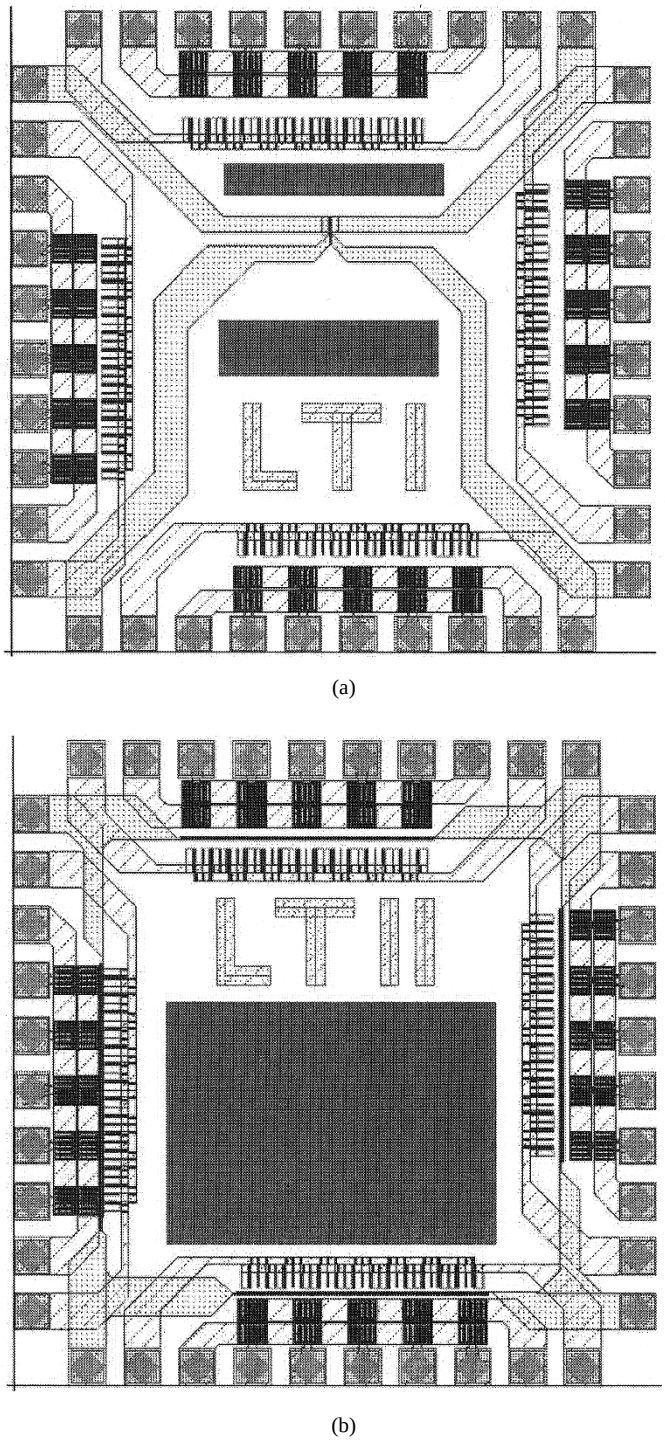


Fig. 11. Testchips drawn to investigate the required spacing between I/O cells and internal circuits for latchup prevention: (a) without and (b) with the additional internal guard rings.

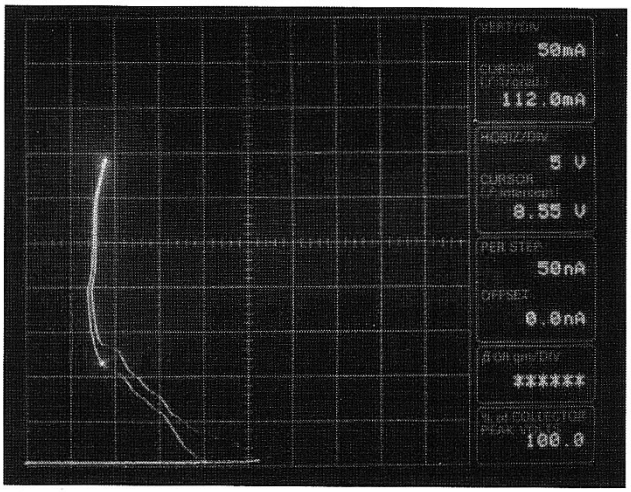
3) I/O Cells in the 0.25-μm Silicided STI Bulk CMOS Process: The I–V characteristics of I/O cells with double guard rings, a single guard ring, and no guard ring fabricated in the 0.25-μm STI silicided bulk CMOS process are also measured. The measured I–V characteristics of the I/O cell with a single guard ring at a temperature of 25 °C and a anode-to-cathode spacing of 17.7 μm is shown in Fig. 18(a), where it has a holding voltage of 13.8 V in the 0.25-μm STI silicided bulk CMOS process. The I–V characteristics of the I/O cell with no guard ring at a temperature of 125 °C and a anode-to-cathode spacing of 5 μm is shown in Fig. 18(b), where it has a holding voltage of only 2.4 V in this 0.25-μm process. The relations between the holding voltage and the anode-to-cathode spacing for I/O cells with different guard rings design at the temperature of 125 °C in 0.25-μm STI silicided bulk CMOS process are shown in Fig. 19. In Fig. 19, the I/O cell with a single guard ring and the anode-to-cathode spacing from 17.7 to 55.7 μm has a holding voltage about $\sim$13.8 V, which is much higher than V_{DD} of CMOS IC in this 0.25-μm CMOS process. The I/O cell with double guard rings has no more improvement for latchup prevention than that only with single guard ring. Therefore, the I/O cells in this 0.25-μm STI silicided bulk CMOS process drawn with only single guard ring are enough to prevent latchup and to save layout area.

From the aforementioned experimental results, the use of silicided diffusion in the 0.35-μm CMOS process causes an obvious increase on the holding voltage of latchup path in I/O cells. In the 0.25-μm CMOS process, both uses of silicided diffusion and STI further increase the holding voltage of latchup path. Therefore, the I/O cells realized in the CMOS process with silicided diffusion (or further with STI isolation) can be drawn with only a single guard ring to have high enough holding voltage to prevent latchup at the I/O circuits.

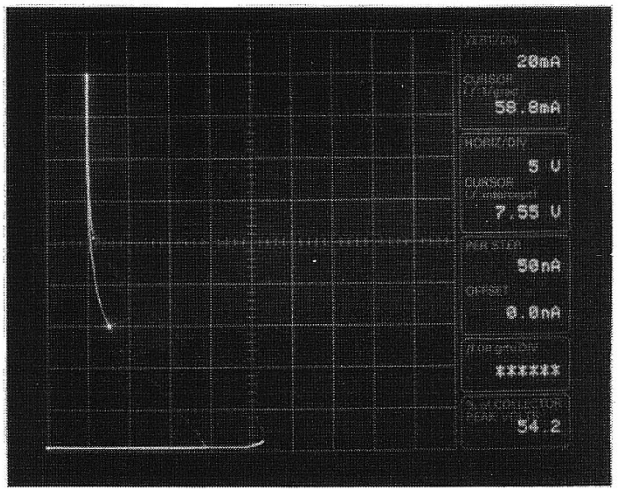
B. I–V Characteristics of the Internal Circuits

The I–V characteristics of the test structures to simulate latchup path in internal circuits with different pickups distances (Xp, Xn, hp, and hn) are measured by the *Tek*370A curve tracer with different bias currents applied to the trigger nodes in the p-substrate or in the n-well. When a positive trigger current is applied into the p+ trigger node of the p-substrate region, the latchup test structures with different pickup distances can be triggered into their latching state. When a (negative) trigger current is flowing out from the n+ trigger node of the n-well region, the latchup test structures with different pickup distances can be also triggered into their latching state. The holding voltages of latchup test structures and the relations between the trigger current and pickup distances in latchup test structures are measured to investigate the latchup immunity in internal circuits.

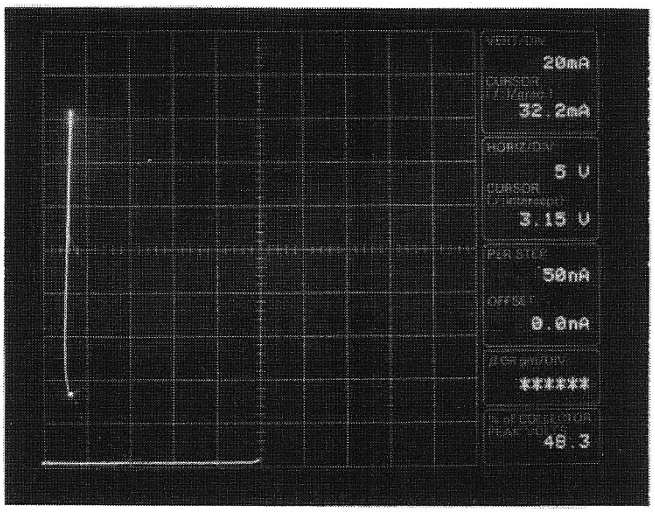
1) Pickup Test Structures in the 0.5-μm Nonsilicided Bulk CMOS Process: The typical I–V curves of latchup test structure with the distance from the n-well/p-substrate pickups to the n-well edge (hn, hp) of 40 μm and the distance between two adjacent pickups (Xn, Xp) of 20 μm under different positive (negative) trigger currents in the p-substrate (n-well) are shown in Fig. 20(a) and (b), respectively. The holding voltages of these latchup test structures with different distances from the n-well/p-substrate pickups to the n-well edge at different temperatures are shown in Fig. 21. The holding voltages of these latchup test structures with different distances between two adjacent pickups at different temperatures are shown in Fig. 22. When the distances from the n-well/p-substrate pickups to the n-well edge (hn, hp) or the distances between two adjacent pickups (Xn, Xp) are increased, the holding voltages of latchup test structures are decreased. But, all the holding voltages in



(a)



(b)



(c)

Fig. 12. Measured latchup I–V characteristics of the I/O cells with: (a) double guard rings at a temperature of 75 °C, (b) a single guard ring at a temperature of 100 °C, and (c) no guard ring at a temperature of 25 °C, fabricated in a 0.5-μm nonsilicided bulk CMOS process.

Figs. 21 and 22 are smaller than 1 V, therefore the internal circuits with such Xn/Xp and hn/hp pickups rules are still sensitive to latchup. This means that the internal circuits with pickup rules cannot avoid the latchup occurrence in internal circuits of a CMOS IC. If there are some trigger currents flowing in the n-well or p-substrate, the latchup paths in internal circuits drawn with the specified pickups rules can be still triggered on. However, if the internal circuits are drawn with more pickups in the layout (specified by a narrower pickup rules), a larger trigger current flowing in the n-well or p-substrate is needed to fire latchup in internal circuits.

2) Pickup Test Structures in the 0.35-μm Silicided Bulk CMOS Process: The test structures with different pickup distances are also fabricated in a 0.35-μm silicided bulk CMOS process to investigate their latchup immunity. The measured I–V curves of latchup test structures with different pickup distances in a 0.35-μm silicided bulk CMOS process are similar to those shown in Fig. 20. The relations between the holding voltage and the distance between two adjacent pickups (Xn, Xp) of the latchup test structure for internal circuits at the temperatures of 28 °C and 100 °C in this 0.35-μm process are shown in Fig. 23. From Fig. 23, due to the use of silicided diffusion, the distances between two adjacent pickups (Xn, Xp) do not significantly influence the holding voltage of latchup test structures. The holding voltage in Fig. 23 is still smaller than 1 V, therefore the internal circuits with such pickups (Xn, Xp) are still sensitive to latchup.

The relations between the threshold (magnitude) and the pulse width of the trigger current applied into the p-substrate or n-well to fire latchup in test structures with different pickup distances are also investigated and shown in Fig. 24(a) and (b). The experimental setup to investigate such dependences has been illustrated in Fig. 3, and the V_{DD} on test structures is biased at 3.3 V. The trigger current pulse is generated from a *Keithley* 2410 current source with tunable current magnitude and pulse width. The minimum trigger current under a fixed pulse width to fire latchup in test structure is defined as the threshold trigger current of the test structure. As seen in Fig. 24(a) and (b), the latchup test structure with a wider pickup distance has a lower threshold trigger current. A longer pulse width of the trigger current also causes a lower threshold trigger current to fire latchup in test structures. However, the threshold trigger current in the p-substrate or n-well to fire latchup in internal circuits drawn with the typical pickup rules is around 500∼900 μA only. Such internal circuits are still sensitive to latchup in bulk CMOS processes.

C. Latchup Occurrence at Internal Circuits Due to the Trigger Current at I/O Pins

From the above measured results, the I/O cell with single or double guard rings has a holding voltage greater than V_{DD}. Therefore, the I/O cells with guard rings should not cause a latchup problem for the CMOS IC. But, the internal circuits with pickups are still sensitive to latchup because the holding voltage of the parasitic p–n–p–n paths in internal circuits with the specified pickup rules is still about ∼1 V only, as shown in Figs. 21–23. In the latchup test, as shown in Fig. 7(a), the trigger current applied to the I/O pin will generate the substrate or well currents to fire latchup in the internal circuits, even if the I/O cells have no latchup problem. As seen in Fig. 24, a trigger cur-

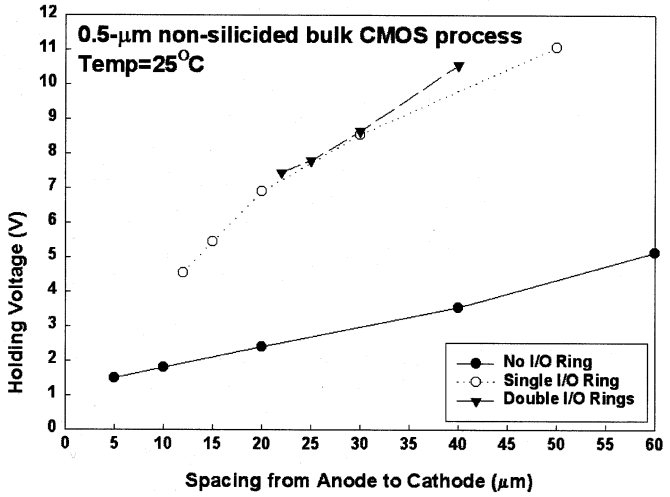


Fig. 13. Relations between the holding voltage and the anode-to-cathode spacing for I/O cells with different guard rings design at a temperature of 25 °C in a 0.5-μm nonsilicided bulk CMOS process.

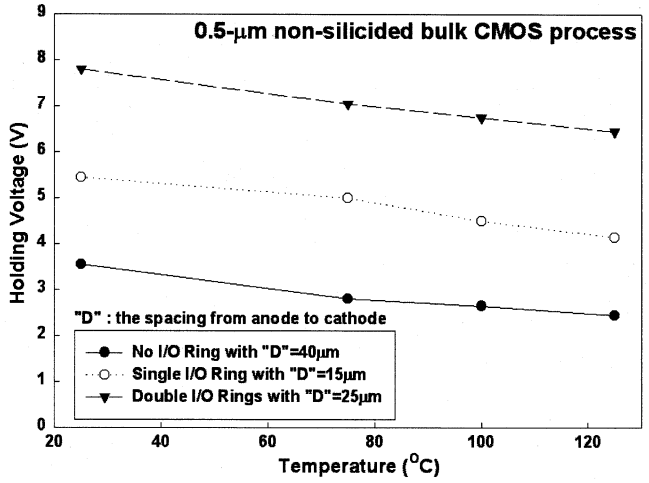


Fig. 14. Relations between the holding voltage and temperature for I/O cells with different guard rings design in a 0.5-μm nonsilicided bulk CMOS process.

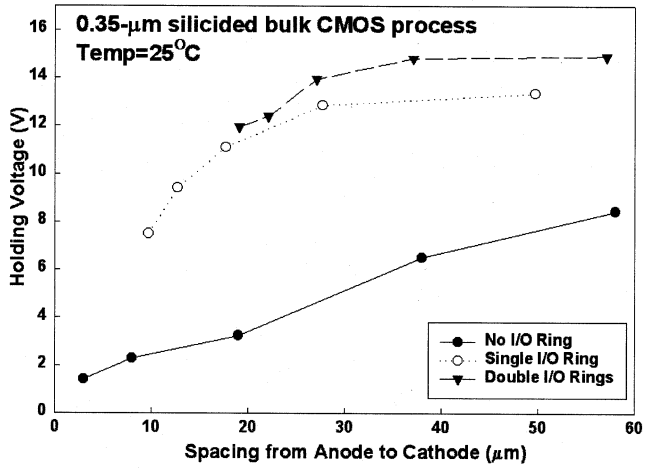


Fig. 15. Relations between the holding voltage and the anode-to-cathode spacing for I/O cells with different guard ring designs at the temperature of 25 °C in a 0.35-μm silicided bulk CMOS process.

rent in the p-substrate or n-well with a magnitude of only several hundreds of microamperes can fire latchup in internal circuits

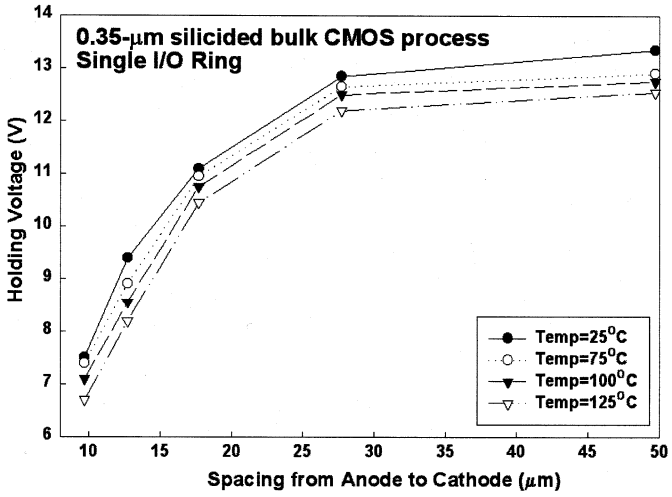


Fig. 16. Relations between the holding voltage and the anode-to-cathode spacing for I/O cells with only single guard ring at different temperatures in a 0.35-μm silicided bulk CMOS process.

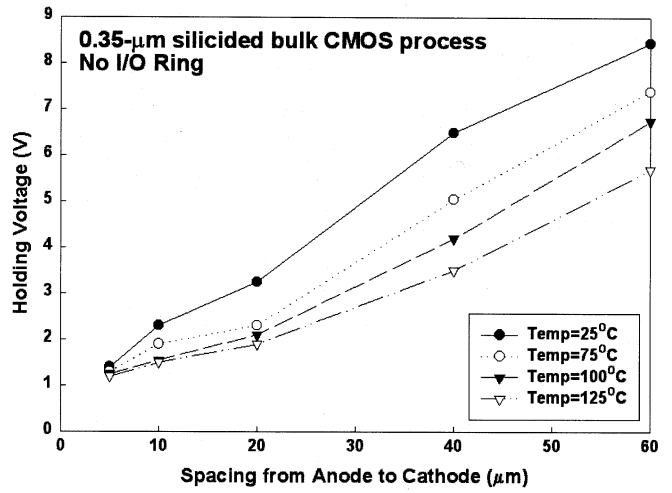
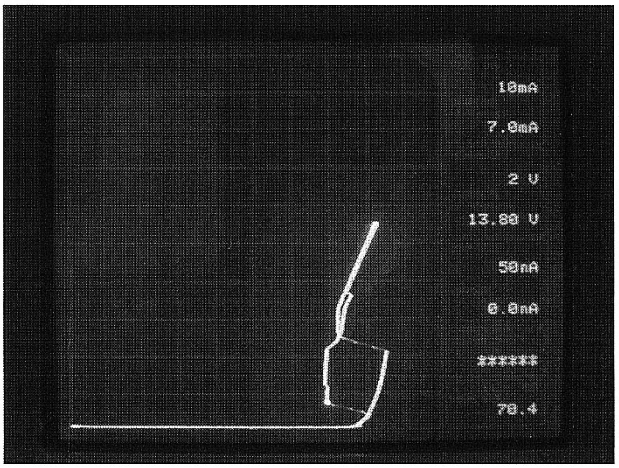


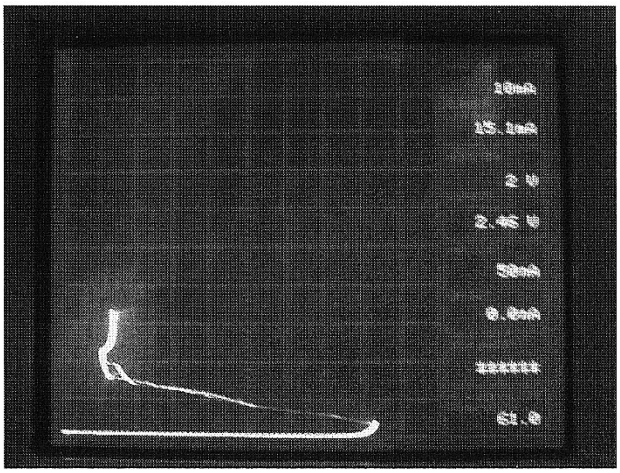
Fig. 17. Relations between the holding voltage and the anode-to-cathode spacing for I/O cells with no guard ring at different temperatures in a 0.35-μm silicided bulk CMOS process.

which is drawn with the typical pickup rules. Therefore, an interesting question is how much substrate or well currents will be generated by the trigger current applied at the I/O cells with different guard rings. In this subsection, an experimental method is used to find this relation.

The experimental setup shown in Fig. 25 is used to investigate the trigger current at I/O pins that causes latchup in the internal circuits. The *Keithley* 2410 current source with a maximum power delivery of 21 W and a current source range from ± 50 pA to ± 1.05 A is used to provide the required current pulse at I/O cells. Three independent dc power supplies are used to bias the I/O cells, the additional internal guard rings, and the latchup sensor cells, separately. The testchips are designed with different spacings from I/O cells to internal latchup sensor cells, as those shown in Figs. 9 and 10. The latchup sensor cells are the same as the latchup test structures with specified pickups to simulate the latchup path in internal circuits. A resistor of 100 Ω is connected between the V_{DD} power supply and the internal latchup sensor cells to limit the large latchup current to burn



(a)



(b)

Fig. 18. Measured latchup I–V characteristics of I/O cells with: (a) a single guard ring at a temperature of 25 °C and (b) no guard ring at a temperature of 125 °C, fabricated in a 0.25-μm silicided STI bulk CMOS process. (X axis: 2 V/div.; Y axis: 10 mA/ div.).

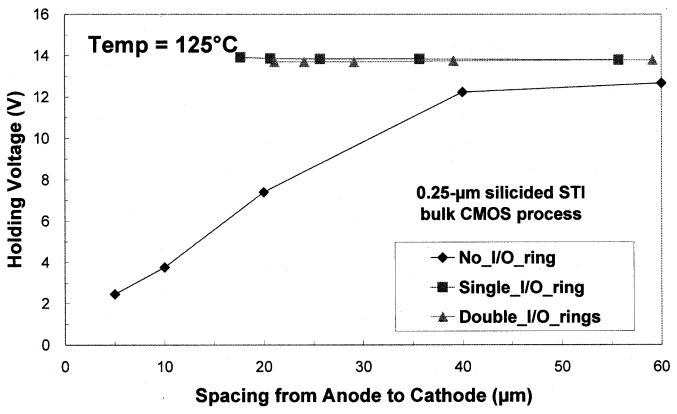
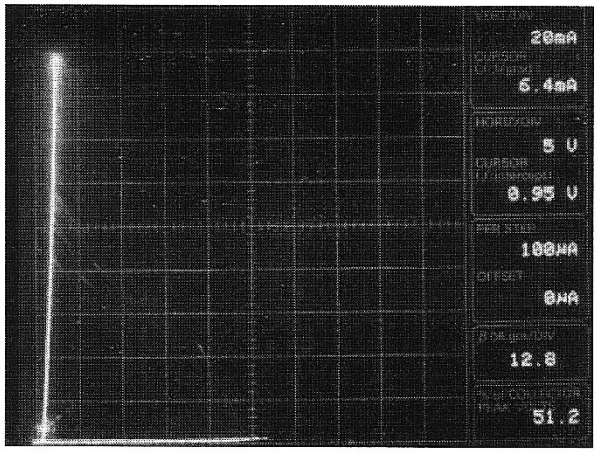
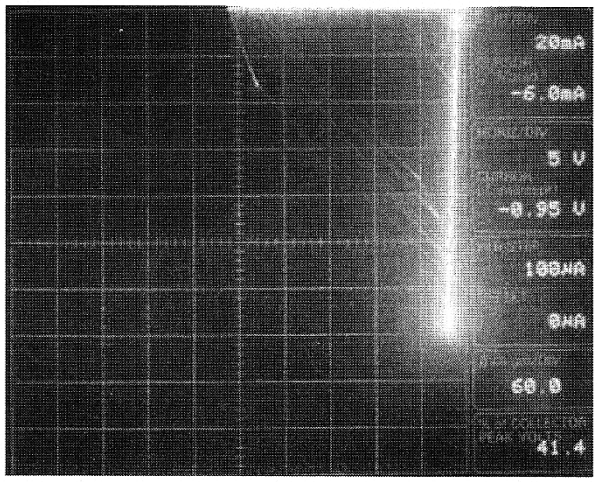


Fig. 19. Relations between the holding voltage and the anode-to-cathode spacing for I/O cells with different guard ring design at the temperature of 125 °C in a 0.25-μm silicided STI bulk CMOS process.

out the latchup sensor cells. The *HP*54 602A oscilloscope with a bandwidth of 150 Mhz is used to monitor the voltage waveform of the input current pulse on the I/O pin (CH1) and the voltage across the latchup sensor cells (CH2). If latchup is fired



(a)



(b)

Fig. 20. Measured I–V characteristics of latchup test structures for internal circuits with different trigger currents applied in: (a) p-substrate and (b) n-well, in a 0.5-μm nonsilicided bulk CMOS process. (X axis: 5 V/div.; Y axis: 20 mA/div.).

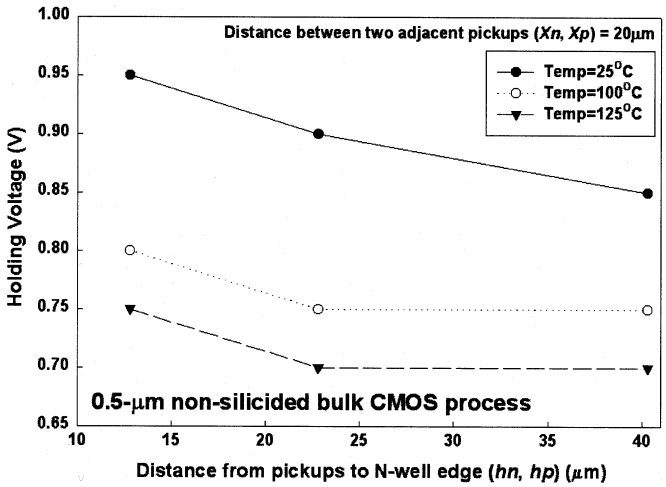


Fig. 21. Relations between the holding voltage and the distance from pickups to n-well edge (hn or hp) of latchup test structures for internal circuits at different temperatures in a 0.5-μm nonsilicided bulk CMOS process.

in the internal latchup sensors by the trigger current applied at I/O pins, the voltage level of CH2 will drop from V_{DD} to the

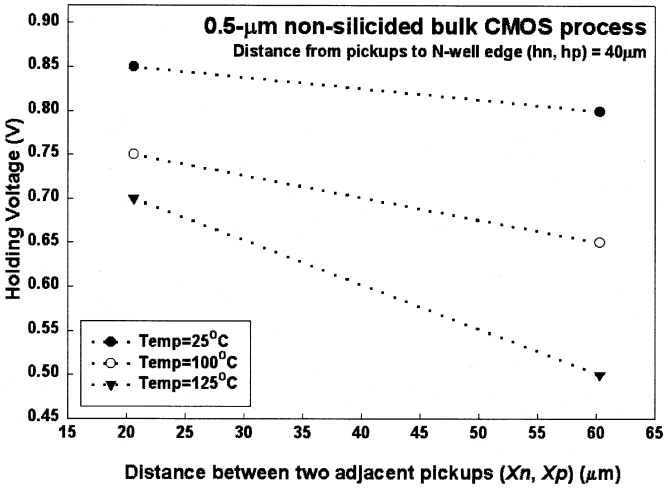


Fig. 22. Relations between the holding voltage and the distance between two adjacent pickups (Xn or Xp) of latchup test structures for internal circuits at different temperatures in a 0.5-μm nonsilicided bulk CMOS process.

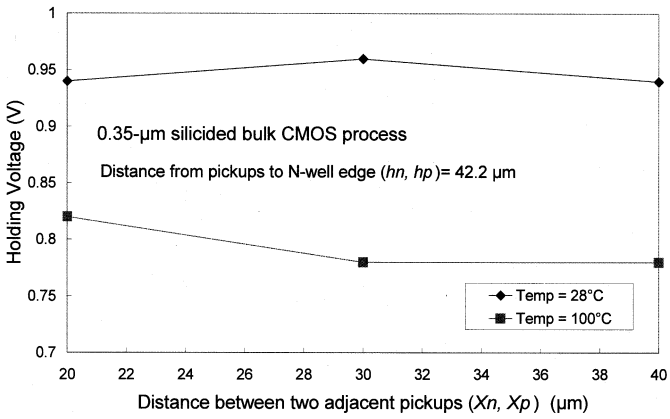
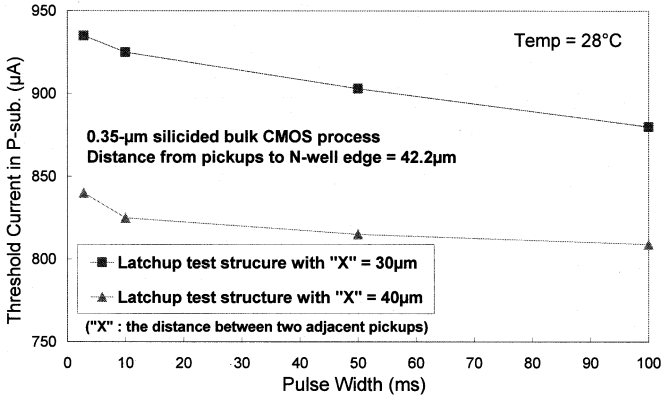


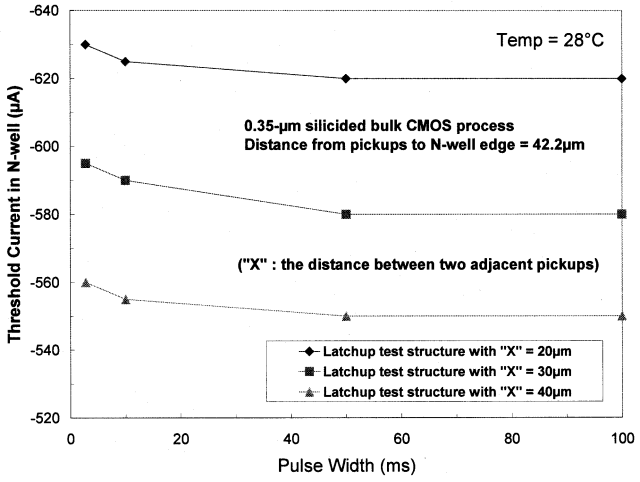
Fig. 23. Relations between the holding voltage and the distance between two adjacent pickups (Xn, Xp) of latchup test structures for internal circuits at the temperatures of 28 °C and 100 °C in a 0.35-μm silicided bulk CMOS process.

voltage level around the holding voltage ($\sim$1 V) of latchup sensors. Otherwise, if latchup is not triggered on in internal latchup sensors, the voltage level of CH2 will be remained at the original V_{DD} voltage level (5 V). By adjusting the current magnitude of the trigger current applied at I/O pins, the critical (threshold) trigger current at I/O pins to fire latchup in the internal latchup sensors can be found.

1) Results in the 0.5-μm Nonsilicided Bulk CMOS Process: The measured results to verify the performance of the additional internal double guard rings between I/O cells and internal circuits are shown in Fig. 26(a) and (b). The I/O cells in this testchip are all drawn with double guard rings to surround NMOS and PMOS in I/O cells. If the spacing from I/O cells to internal latchup sensors is increased, the trigger current on the I/O pins to fire latchup in internal circuits is also increased. When the additional internal double guard rings are added between I/O cells and internal circuits, the trigger current at I/O pins to fire latchup in internal circuits is significantly increased. With the help of the additional internal double guard rings, a distance of 30 μm from I/O cells to internal circuits can provide a latchup immunity of greater than $\pm$300 mA at



(a)



(b)

Fig. 24. Relations between the threshold (magnitude) and the pulse width of the trigger current applied into: (a) the p-substrate and (b) the n-well, to fire latchup in test structures with different pickup distances at the temperatures of 28 °C in a 0.35-μm silicided bulk CMOS process.

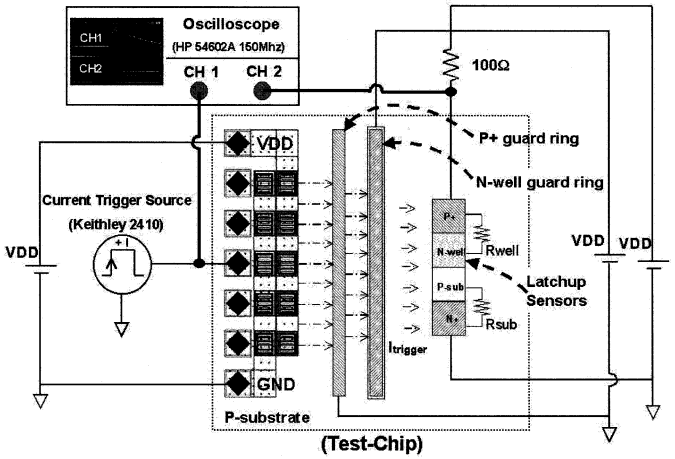
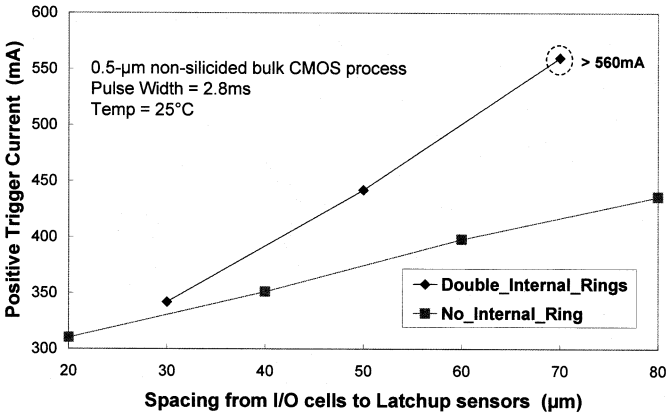


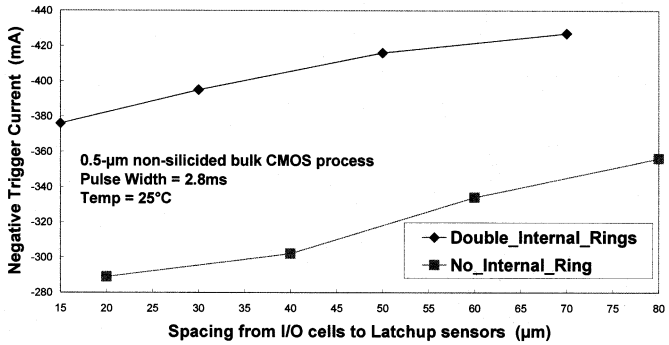
Fig. 25. Experimental setup used to find the relation that the trigger current applied at the I/O pin but to fire latchup in the internal circuits.

the temperature of 25 °C with a trigger current pulse width of 2.8 ms.

From Fig. 26(a) and (b), we can confirm that the internal circuits drawn with the specified pickup rules are still sensitive to latchup. By adding the additional internal guard rings (as those

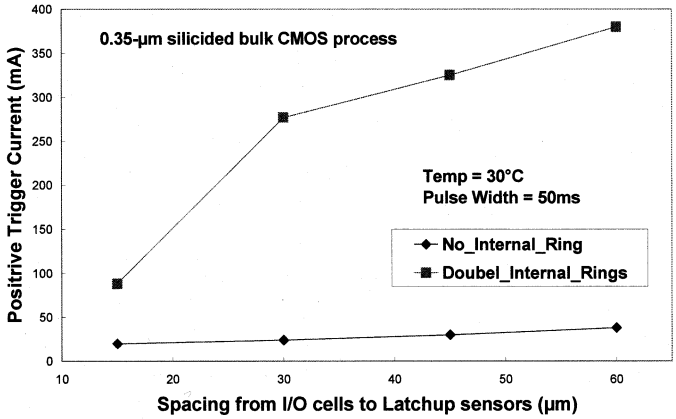


(a)

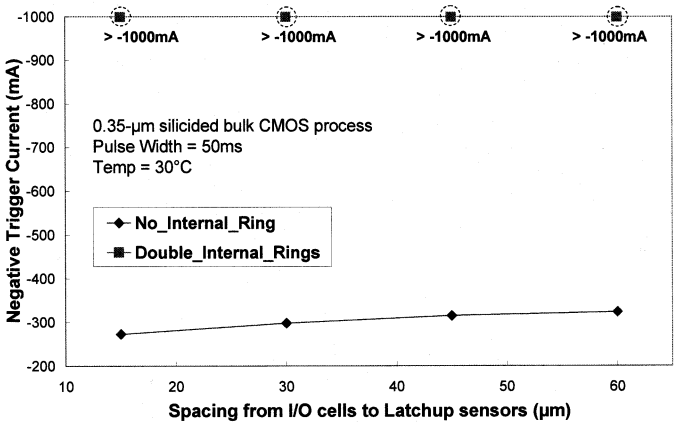


(b)

Fig. 26. Relations between: (a) the positive and (b) the negative trigger current applied at the I/O pins to fire latchup in internal latchup sensors and the layout spacing from I/O cells to latchup sensors with or without the additional internal guard rings in a 0.5-μm nonsilicided bulk CMOS process.



(a)



(b)

Fig. 27. Relations between: (a) the positive and (b) the negative trigger current at the I/O pins to fire latchup in internal latchup sensors and the layout spacing from I/O cells to latchup sensors with or without the additional internal guard rings in a 0.35-μm silicided bulk CMOS process.

shown in Fig. 10) between the I/O cells and the internal circuits, the threshold trigger current applied at I/O pins to fire latchup in internal circuits can be significantly increased. With the additional guard rings between I/O cells and internal circuits, the layout spacing from I/O cells to internal circuits can be further reduced to save the chip area but still keep an improved latchup immunity.

2) Results in the 0.35-μm Silicided Bulk CMOS Process: The measured results on the testchips fabricated in 0.35-μm silicided bulk CMOS process are shown in Fig. 27(a) and (b). The I/O cells in this testchip are all drawn with only a single guard ring to surround NMOS and PMOS in I/O cells. When the additional internal guard rings are added between the I/O cells and the internal circuits, the threshold trigger current at I/O pins to fire latchup in internal circuits is significantly increased. This increase, by using the additional internal guard rings, is much higher than that by using a wider distance between I/O cells and internal circuits. With the help of the additional internal guard rings, a distance of 30 μm from I/O cells to internal circuits can provide latchup immunity greater than $\pm$250 mA at the temperature of 30 °C with a trigger current pulse width of 50 ms. For the test patterns without such additional internal guard rings and with a distance of 60 μm from I/O cells to internal circuits, a positive trigger current of only 38 mA with a pulse duration of 50 ms can fire latchup in the internal circuits at the temperature of 30 °C. Therefore, the additional internal double guard rings should be drawn between I/O cells and internal circuits to maintain high latchup immunity. With the additional internal double guard rings, the layout spacing from I/O cells to internal circuits can be further reduced to save the silicon area of CMOS IC.

The relations between the positive or negative threshold trigger current at the I/O pins to fire latchup in the internal circuits and the pulse width of the trigger current are shown in Figs. 28 and 29. The results in Fig. 28 are measured from the test patterns with the additional internal double guard rings under different spacings from I/O cells to internal circuits at the temperature of 30 °C. The results in Fig. 29 are measured from the test patterns with no any internal guard ring under different spacings from I/O cells to internal circuits at the temperature of 30 °C. As seen in Figs. 28 and 29, the magnitude of threshold trigger current at I/O pins to fire latchup in the internal circuits will be slightly reduced by the increase of the pulse width of the trigger current at I/O cell. But, the additional internal double guard rings can significantly increase the magnitude of threshold trigger current at I/O pins to fire latchup in the internal circuits.

In Fig. 30, the relations between the positive threshold trigger current at I/O pins to fire latchup in the internal circuits and the

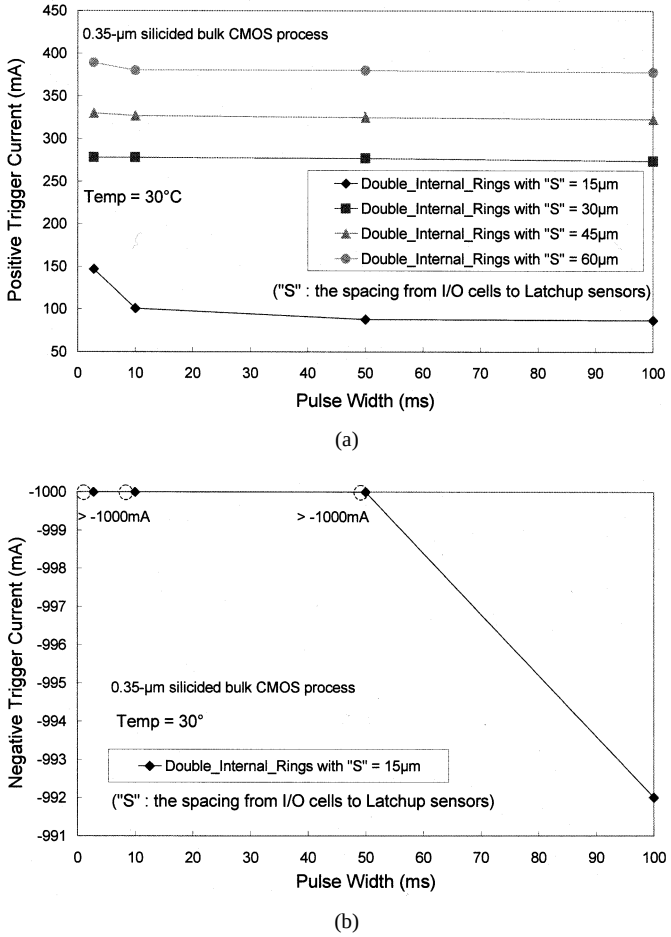


Fig. 28. Relations between: (a) the positive and (b) the negative trigger current at the I/O pins to fire latchup in internal latchup sensors and the pulse width of the trigger current with the additional internal double guard rings in a 0.35-μm silicided bulk CMOS process.

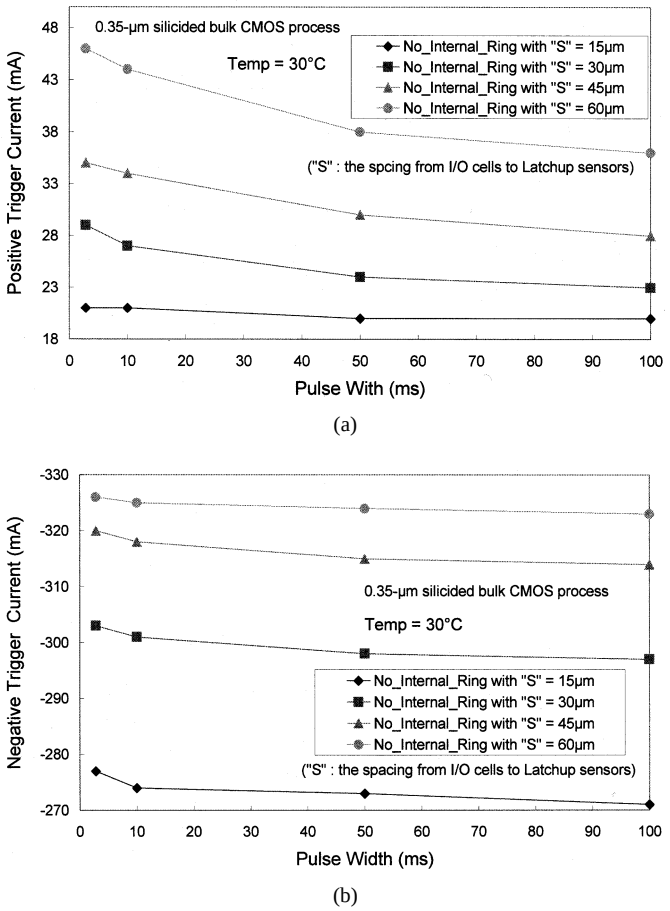


Fig. 29. Relations between: (a) the positive and (b) the negative trigger current at the I/O pins to fire latchup in internal latchup sensors and the pulse width of the trigger current with no internal guard ring in a 0.35-μm silicided bulk CMOS process.

diffusion width of the internal p+ diffusion guard ring are investigated at the temperature of 30 °C with the trigger current pulse width of 50 ms. The results are measured from the test patterns with the additional internal double guard rings and a fixed distance of 30 μm from I/O cells to internal circuits. In the test patterns, the width of the internal n+ diffusion (with n-well) guard ring is fixed at 3.4 μm, but the width of the internal p+ diffusion guard ring is drawn as 3, 6, and 9 μm to investigate its guard ring efficiency. As seen in Fig. 30, the threshold trigger current at I/O pins to fire latchup in the internal circuits is increased when the width of the internal p+ diffusion guard ring is increased.

3) Results in the 0.25-μm Silicided STI Bulk CMOS Process: The test patterns with or without the additional internal double guard rings are also verified in the 0.25-μm silicided STI bulk CMOS process, and the measured results are shown in Figs. 31 and 32 at the temperature of 125 °C with the trigger current pulse width of 50 ms. The I/O cells in this testchip are all drawn with only a single guard ring to surround NMOS and PMOS in I/O cells. In Fig. 31, the positive threshold trigger current at I/O pins to fire latchup in the internal circuits can be increased from the original 38 mA to become 335 mA by the additional internal double guard ring, when the test pattern has a fixed spacing of 30 μm from

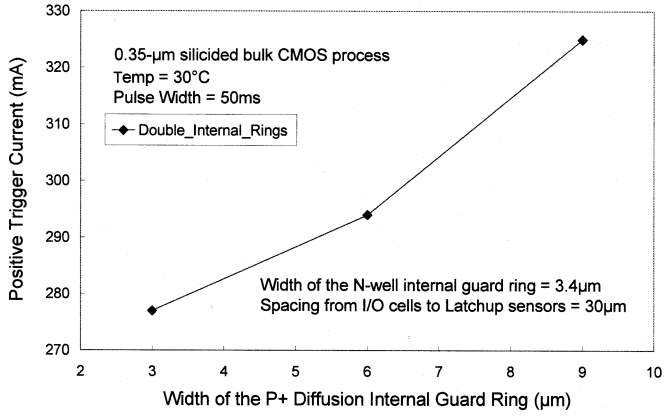


Fig. 30. Relations between the positive trigger current at the I/O pins to fire latchup in internal latchup sensors and the width of the p+ internal guard ring at the temperature of 30 °C in a 0.35-μm silicided bulk CMOS process.

I/O cells to internal circuits. In Fig. 32(a) and (b), the relations between the magnitude and the pulse width of threshold trigger current at I/O pins to fire latchup in the internal circuits are measured when the test pattern has a fixed spacing of 15 μm from I/O cells to internal circuits. From these figures, the efficiency of the additional internal guard rings is also proven in the 0.25-μm silicided STI bulk CMOS process.

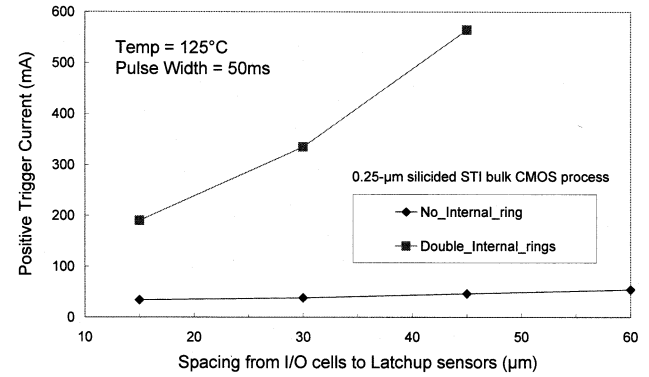
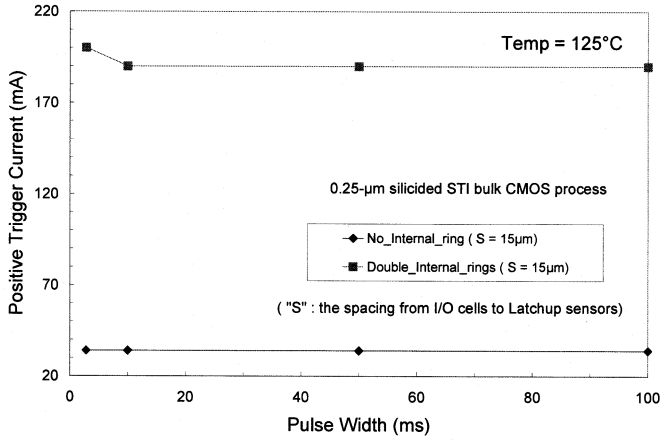
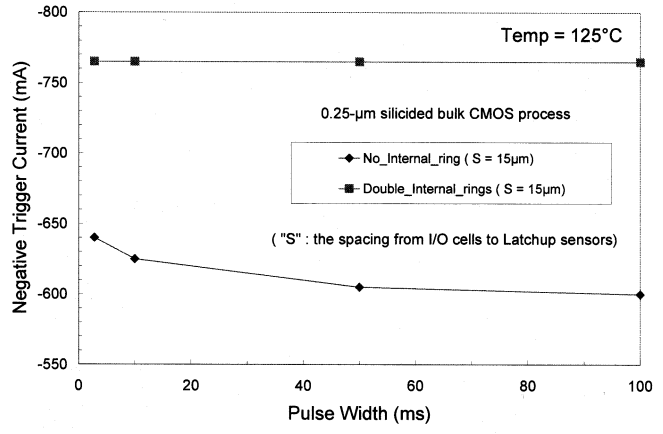


Fig. 31. Relations between the positive trigger current at the I/O pins to fire latchup in internal latchup sensors and the layout spacing from I/O cells to latchup sensors with or without the additional internal guard rings at a temperature of 125 °C in a 0.25-μm silicided STI bulk CMOS process.



(a)



(b)

Fig. 32. Relations between: (a) the positive and (b) the negative trigger current at the I/O pins to fire latchup in internal latchup sensors and the pulse width of the trigger current with or without the additional internal guard rings at a temperature of 125 °C in a 0.25-μm silicided STI bulk CMOS process.

Therefore, the additional internal double guard rings should be drawn as wide as possible in the real chip layout under a specified spacing from I/O cells to internal circuits. By using this methodology, one set of compact (area-efficient) latchup rules to improve latchup immunity in CMOS ICs can be established.

When comparing the curves, among Fig. 26 for 0.5-μm nonsilicided process, Fig. 27 for 0.35-μm silicided process, and Fig. 31 for 0.25-μm silicided STI process, the processes with silicided diffusion have a much lower threshold trigger current at I/O pad to fire latchup in the internal circuits if no additional guard rings are added in the chip. Even if the spacing from I/O cells to internal circuits is increased, the threshold trigger current at I/O pad is still not obviously increased. But, if the additional guard rings are added into the chip, the threshold trigger current at I/O pad can be significantly increased up to several hundreds of milliamperes. This is due to the silicided diffusion causing the main current flow to be close to silicon surface. Therefore, the latchup immunity of internal circuits can be significantly improved by adding the additional double guard rings placed between I/O cells and internal circuits in the chip layout.

V. Conclusion

A new methodology has been proposed to extract the area-efficient layout rules for latchup prevention in bulk CMOS processes. From the experimental results on the I/O cells, even at a higher temperature of 125 °C, the holding voltage of I/O cells in bulk CMOS processes with silicided diffusion can be greater than V_{DD} by using only single guard ring to surround the NMOS and PMOS and with a narrow anode-to-cathode spacing in I/O cells. Therefore, the I/O cells can be drawn with only a single guard ring to save layout area. From the measured results on the pickup test patterns to simulate the latchup paths in internal circuits, the holding voltages of latchup test structures with different pickup rules in three different bulk CMOS processes are all kept at about $\sim$1 V. A trigger current of only several hundreds of microamperes in the p-substrate or the n-well can fire on latchup in the test structures under different pickup rules. Therefore, the internal circuits even drawn with narrower pickup rules are still sensitive to latchup. However, the additional internal guard rings added between the I/O cells and the internal circuits can significantly increase latchup immunity of internal circuits. The excellent efficiency of the additional internal guard rings to increase latchup immunity has been practically proven in three different bulk CMOS processes.

By the new proposed methodology, one set of area-efficient compact latchup rules to prevent latchup occurrence in bulk CMOS processes can be extracted. For example, only with the single guard ring to surround NMOS and PMOS in I/O cells, the anode-to-cathode spacing of latchup path in I/O cells can be reduced to only 10 μm in a 0.35-μm silicided bulk CMOS process, but the I/O cells can be still free to latchup even at a higher temperature of 125 °C. With the additional internal double guard rings between I/O cells and internal circuits, the distance from I/O cells to internal circuits can be further shorten to only 30 μm, but the internal circuits still have a latchup immunity greater than $\pm$100 mA in both the 0.5-μm nonsilicided and 0.35-μm silicided CMOS processes. The CMOS ICs, fabricated in the 0.25-μm silicided bulk CMOS process with STI and lower V_{DD} voltage level, essentially have higher latchup immunity. Thus, the latchup design rules in such a 0.25-μm silicided STI bulk CMOS process can be more compact to save layout area than those used in the 0.5-μm nonsilicided or 0.35-μm silicided CMOS processes.

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