Enhanced Negative Substrate Bias Degradation in nMOSFETs With Ultrathin Plasma Nitrided Oxide

Tsu-Hsiu Perng, Chao-Hsin Chien, Ching-Wei Chen, Horng-Chih Lin, Chun-Yen Chang, *Fellow, IEEE*, and Tiao-Yuan Huang, *Fellow, IEEE*

***Abstract*—The degradation induced by substrate hot electron (SHE) injection in 0.13-μm nMOSFETs with ultrathin ($\sim$2.0 − nm) plasma nitrided gate dielectric was studied. Compared to the conventional thermal oxide, the ultrathin nitrided gate dielectric is found to be more vulnerable to SHE stress, resulting in enhanced threshold voltage (V_t) shift and transconductance (G_m) reduction. The severity of the enhanced degradation increases with increasing nitrogen content in gate dielectric with prolonged nitridation time. While the SHE-induced degradation is found to be strongly related to the injected electron energy for both conventional oxide [1], [2] and plasma-nitrided oxide, dramatic degradation in threshold voltage shift for nitrided oxide is found to occur at a lower substrate bias magnitude (~ -1 V), compared to thermal oxide ($\sim$ −1.5 V). This enhanced degradation by negative substrate bias in nMOSFETs with plasma-nitrided gate dielectric is attributed to a higher concentration of paramagnetic electron trap precursors introduced during plasma nitridation [3].**

***Index Terms*—Paramagnetic electron trap, plasma nitrided gate dielectric, substrate hot electron.**

I. Introduction

FOR MOSFETs employing ultrathin gate oxide, the drastic increase in standby power consumption as a result of the direct tunneling leakage current in the dielectric is a challenging issue, especially as device scaling leads to higher device density in a chip. In addition, the dopant impurity penetration through the ultrathin gate dielectric represents another major concern on the oxide scaling. In the past, nitrogen incorporation into the ultrathin gate oxide to form oxynitride and/or nitride/oxide stacks have been successfully demonstrated to alleviate the above shortcomings [4]. Among the available nitridation techniques, plasma nitridation is particularly viable and popular for preparing reliable ultrathin gate dielectric due to its uniformity, relatively high nitrogen concentration, low-process temperature, and the ability to preserve high-quality oxide/Si interface [5]–[7].

Nonetheless, the introduction of nitrogen into the gate dielectric is known to cause enhanced degradation in negative bias temperature instability (NBTI) for pMOSFETs [2]. For nMOSFETs, however, the less significant impact of plasma nitridation on device reliability was commonly reported [8]. In this paper, we report, for the first time, that by subjecting the device to substrate hot electron stress [9], nMOSFETs with ultrathin plasma-nitrided gate oxide ($\sim$2.0 nm) suffer an enhanced reliability degradation, compared to the device with conventional thermal oxide in terms of V_t shift and G_m reduction. The enhanced degradation under negative substrate bias is believed to be due to a higher level of paramagnetic electron trap precursors in the gate dielectric created by the plasma nitridation process [3].

Manuscript received January 2, 2003; revised February 10, 2003. This work was supported in part by the National Science Council of Taiwan, R.O.C., under Contract NSC-91-2721-2317-200. The review of this letter was arranged by Editor S. Kawamura.

T.-H. Perng, C.-W. Chen, C.-Y. Chang, and T.-Y. Huang are with the Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C.

C.-H. Chien and H.-C. Lin are with the National Nano Device Laboratories, Hsinchu 30050, Taiwan, R.O.C. (e-mail: chchien@ndl.gov.tw).

Digital Object Identifier 10.1109/LED.2003.812556

II. Experiment

Deep submicron (0.13 μm) nMOSFETs with ultrathin gate dielectrics were used in this study. After active device area definition, conventional thermal oxides were grown at 900 °C. In order to achieve a final equivalent oxide thickness (EOT) of approximately 2.0 nm for all splits, thermal oxides with various starting thickness were subjected to various plasma nitridation times. After deposition and patterning of a 150-nm thick undoped poly-Si film, arsenic dopants were implanted with an energy of 5 keV to dope the gate electrode and also to form the shallow source–drain junction. For activation, all samples were annealed using rapid thermal annealing (RTA) in N_2 gas ambient for 30 s. Subsequently, cobalt salicide, borophosphosilicate glass (BPSG), and metallization processes were performed to complete the device fabrication. For reliability testing, constant positive voltage of 2.2 V was applied to the gate with the source and drain grounded and the negative bias ranging from 0 V [i.e., constant voltage stress (CVS)] to −2 V was applied to the substrate terminal at room temperature. Device characteristics were recorded at certain time interval for stress time up to 10^4 s. The indicators of reliability degradation are transconductance G_m reduction and threshold voltage V_t shift. G_m is defined as the peak value of the transconductance of a device in linear region, while threshold voltage is defined at the interception extrapolated from the peak value.

III. Results and Discussions

Fig. 1 shows the characteristics of drain current (I_D) and transconductance (G_m) as a function of effective gate drive ($V_G - V_t$) at $V_D = 0.1$ V for different samples with and without plasma nitridation. It can be seen that the subthreshold slope and the peak value of transconductance are not degraded by the nitridation. This result is consistent with the previous report [10] in which the resultant nitrided layer was claimed to be only about 0.7 nm deep from the top of gate dielectric and the high-quality interface at the substrate side is maintained after

0741-3106/03$17.00 © 2003 IEEE

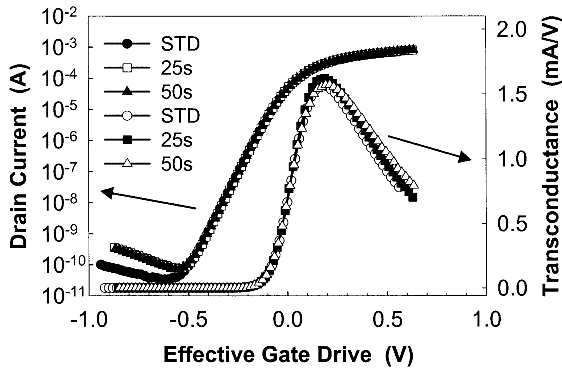
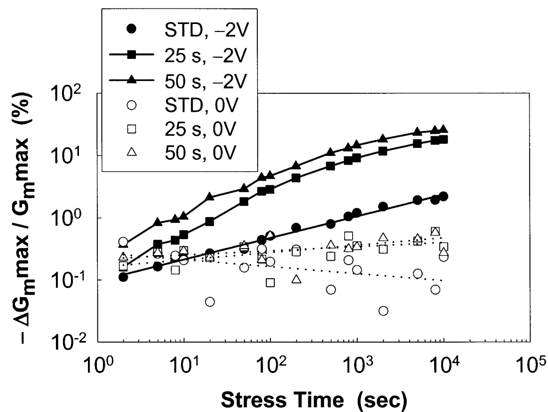
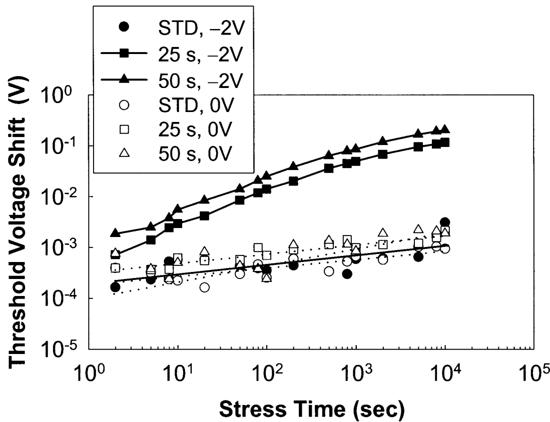


Fig. 1. Drain current (I_D) and transconductance (G_m) characteristics as a function of effective gate drive ($V_G - V_t$) for devices with thermal oxide (control) and plasma nitrided oxides (with plasma treatment time of 25 and 50 s, respectively).



(a)



(b)

Fig. 2. Substrate hot electron (SHE) stress time dependence of (a) relative G_m degradation and (b) threshold voltage (V_t) shift for devices with thermal oxide (control) and plasma nitrided oxides (with plasma treatment time of 25 and 50 s, respectively). Substrate biases are 0 and -2 V, respectively.

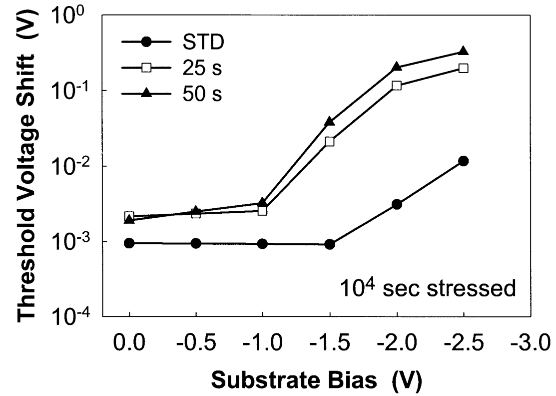


Fig. 3. Threshold voltage (V_t) shift of the devices with thermal oxide and plasma nitrided oxides as a function of substrate bias after 10^4 s of SHE stressing.

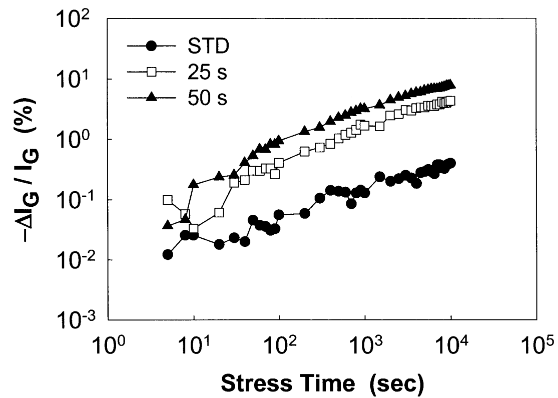


Fig. 4. Relative gate leakage current change as a function of SHE stress time for different samples.

plasma nitridation. The relative transconductance reduction and threshold voltage shift as a function of stress time are shown in Fig. 2(a) and (b), respectively. Two substrate biases, i.e., 0 and -2 V, were employed for comparison. For zero substrate bias, e.g., CVS, only negligible degradations were observed for all splits, irrespective of the gate dielectric preparation processes. When the magnitude of the substrate bias is raised to -2 V, the device with conventional thermal oxide remains stable and depicts only slight degradations in both G_m and V_t. In contrast, significant G_m reduction and V_t shift are observed for the nitrided devices. The extent of damage increases for samples with longer nitridation time (i.e., 50 s compared to 25 s). Fig. 3 depicts threshold voltage shifts as a function of substrate bias for different splits. Under low substrate bias, only a slightly larger threshold voltage shift is observed for the splits with plasma-nitrided oxides. This trend remains unchanged until the magnitude of the substrate bias reaches -1 V, where a dramatic increase in threshold voltage shift occurs for nitrided samples, independent of the incorporated nitrogen content. In contrast, the magnitude of the threshold substrate bias needed for inducing significant V_t shift for the sample with thermal oxide is 0.5 V larger (i.e., at a substrate bias of -1.5 V). Fig. 4 shows the relative gate current changes for different samples over stress time with a substrate bias of -2 V. A larger electron trapping density can be seen for samples with plasma nitridation and increases with increased plasma treatment time.

A plausible cause of the observed exacerbated degradation is plasma-induced damage during nitridation. But, it is ruled out because only insignificant and bias-insensitive degradation has been found at low substrate bias regime, which obviously contradicts with the fact that plasma-induced "latent" defects can be easily retriggered even under traditional constant voltage stress, i.e., $V_{BS} = 0$ V [11]. As is well known, trap filling of the as-fabricated defects in plasma-nitrided oxide, which

were speculated to be located near valence band [12], could account for the slightly larger V_t shift in the low substrate bias range. However, the trap-filling rate should not increase with the increasing energy of the transport carriers. Therefore, we hypothesize that nitrogen incorporation in the thermal oxide by plasma nitridation could introduce more precursors of paramagnetic electron traps into oxide bulk. These precursors (e.g., $\equiv$ Si_2NH or $\equiv$ Si_2N–NSi_2 $\equiv$) can be more easily broken, compared to the dominant precursors ($\equiv$ Si–O–O–Si $\equiv$) in thermal oxide, and become paramagnetic electron trap centers after hot electron stress. This explains the substrate-bias-dependent threshold voltage shift, since energy is needed to activate the bond breaking reaction [3].

IV. Conclusion

We report, for the first time, an enhanced degradation under negative substrate bias in nMOSFETs with ultrathin plasma-nitrided gate dielectric. The enhanced degradation is attributed to the introduction of paramagnetic electron trap precursors during plasma nitridation. Similar to NBTI in pMOSFETs, our findings are important for nMOSFETs from the reliability point of view. Even though the incorporation of nitrogen into thermal oxide is advantageous in many respects, our findings suggest that careful attention needs to be paid to ensure that plasma-nitrided gate dielectric meets the reliability requirements for the sub-100-nm device technology node.

References

[1] E. M. Vogel, J. S. Suehle, M. D. Edelstein, B. Wang, Y. Chen, and J. B. Bernstein, "Reliability of ultrathin silicon dioxide under combined substrate hot-electron and constant voltage tunneling stress," *IEEE Trans. Electron Devices*, vol. 47, pp. 1183–1191, June 2000.

[2] N. Kimizuka, K. Yamaguchi, K. Imai, T. Iizuka, C. T. Liu, R. C. Keller, and T. Horiuchi, "NBTI enhancement by nitrogen incorporation into ultrathin gate oxide for 0.10-μm gate CMOS generation," in *Proc. Symp. VLSI Technology*, 2000, pp. 92–93.

[3] H. Wong and V. A. Gritsenko, "Dielectric traps in amorphous silicon oxynitride," in *Proc. Hong Kong Electron Devices Meeting*, 2001, pp. 132–139.

[4] D. A. Buchanan, "Scaling the gate dielectric: Materials, integration, and reliability," *IBM J. Res. Develop.*, vol. 43, no. 3, pp. 245–264, May 1999.

[5] H. Yang, H. Niimi, J. W. Keister, G. Lucovsky, and J. E. Rowe, "The effects of interfacial sub-oxide transition regions and monolayer level nitridation on tunneling currents in silicon devices," *IEEE Electron Device Lett.*, vol. 21, pp. 76–78, Feb. 2000.

[6] Y. Wu, Y. M. Lee, and G. Lucovsky, "1.6 nm oxide equivalent gate dielectrics using nitride/oxide (N/O) composites prepared by RPECVD/oxidation process," *IEEE Electron Device Lett.*, vol. 21, pp. 116–118, Mar. 2000.

[7] C. H. Chen, Y. K. Fang, C. W. Yang, S. F. Ting, Y. S. Tsair, M. C. Yu, T. H. Hou, M. F. Wang, S. C. Chen, C. H. Yu, and M. S. Liang, "Thermally-enhanced remote plasma nitrided ultrathin (1.65 nm) gate oxide with excellent performances in reduction of leakage current and boron diffusion," *IEEE Electron Device Lett.*, vol. 22, pp. 378–380, Aug. 2001.

[8] N. Soin, J. F. Zhang, and G. Groeseneken, "MOSFET's reliability: Electron trapping in gate dielectric," in *Proc. Int. Conf. Semiconductor Electronics*, 2000, pp. 104–109.

[9] R. Degraeve, G. Groeseneken, R. Bellens, J. L. Ogier, M. Depas, P. J. Roussel, and H. E. Maes, "New insights in the relation between electron trap generation and the statistical properties of oxide breakdown," *IEEE Trans. Electron Devices*, vol. 45, pp. 904–911, Apr. 1998.

[10] S. V. Hattangady, R. Kraft, D. T. Grider, M. A. Douglas, G. A. Brown, P. A. Tiner, J. W. Kuehne, P. E. Nicollian, and M. F. Pas, "Ultrathin nitrogen-profile engineered gate dielectric films," in *IEDM Tech. Dig.*, 1996, pp. 495–498.

[11] K. Eriguchi, T. Yamada, Y. Kosaka, and M. Niwa, "Impacts of plasma process-induced damage on ultra-thin gate oxide reliability," in *Proc. Int. Reliability Physics Symp.*, 1997, pp. 178–183.

[12] M. Togo, K. Watanabe, M. Terai, S. Kimura, A. Morioka, T. Yamamoto, T. Tatsumi, and T. Mogami, "Controlling base-SiO_2 density of low-leakage 1.6 nm gate-SiON for high-performance and highly reliable n/pFET's," in *Proc. Symp. VLSI Technol.*, 2001, p. 81.