Available online at www.sciencedirect.com
SCIENCE DIRECT®
ELSEVIER
Materials Chemistry and Physics 80 (2003) 325–328
MATERIALS CHEMISTRY AND PHYSICS
www.elsevier.com/locate/matchemphys

Temperature dependent integrity of $Sr_{0.8}Bi_2Ta_2O_9$ films on ultra-thin Al_2O_3 buffered Si

Bang Chiang Lan [a], San Yuan Chen [a,*], Hsin-Yi Lee [b]

[a] Department of Materials Science and Engineering, National Chiao Tung University, Hsinchu, Taiwan, ROC
[b] Research Division Synchrotron Radiation Research Center, Hsinchu, Taiwan, ROC

Received 18 June 2002; received in revised form 18 October 2002; accepted 24 October 2002

Abstract

The annealing temperature dependent integrity of $Sr_{0.8}Bi_2Ta_2O_9$ (SBT) on ultra-thin 4 nm SiO_2 and Al_2O_3 buffered Si was investigated in this work. Although the capacitance–voltage characteristics show hysteresis loops in both cases, the memory window of $Sr_{0.8}Bi_2Ta_2O_9/Al_2O_3$ capacitor is larger than that of $Sr_{0.8}Bi_2Ta_2O_9/SiO_2$ capacitor. As increasing annealing temperature from 800 to 900 °C, the grain size and memory window of polycrystalline SBT increase both cases. At 800 °C, the leakage current density of $Sr_{0.8}Bi_2Ta_2O_9/Al_2O_3$ capacitor is 3.2×10^{-8} A/cm^2 at −3 V, which is low enough for deep sub-μm application. With increasing temperature to 900 °C, the leakage current in both structures becomes smaller.
© 2002 Elsevier Science B.V. All rights reserved.

Keywords: $Sr_{0.8}Bi_2Ta_2O_9$ (SBT); Al_2O_3 buffer; Memory window; Leakage current

1. Introduction

The thin films of Bi layered structured perovskite compound, $SrBi_2Ta_2O_9$ (SBT), is well known to show excellent ferroelectric properties because of its specific crystal structure. Due to the particular properties, SBT thin films have been widely studied for the application in metal–ferroelectric–semiconductors field effect transistors (MFS-FETs) [1,2]. Although the metal/ferroelectric/semiconductors memory has been studied for about 40 years [3], the progress of this memory is very slow because of the problems of interface reaction between ferroelectric material and Si [4,5]. In order to overcome these problems, an intermediate layer of SiO_2, CeO_2, or Y_2O_3 [6–8] is inserted between ferroelectric material and Si layer that results in the metal/ferroelectric/insulator/semiconductors (MFIS) structure [9,10]. However, the inserted gate dielectric must be thin enough to avoid significant voltage drop in this layer. Furthermore, for process integration with next generation high performance and low voltage logic technology, ultra-thin gate dielectric layer and large capacitance are required. Recently, the ultra-thin Al_2O_3 of 4 nm thickness was used as both gate dielectric and diffusion barrier for one-transistor (1T) ferroelectric–metal-oxide–semiconductor FET (FeMOSFET) memory because of the excellent gate dielectric and diffusion barrier properties [11,12]. Good device memory characteristics of 1T Pb(Zr, Ti)O_3 FeMOSFET have also been achieved [13,14]. Because SBT has better fatigue resistence than PZT [15], in this paper, we have further studied the temperature dependent memory characteristics of $SrBi_2Ta_2O_9$ on ultra-thin 4 nm Al_2O_3 buffered Si in comparison with those on the same 4 nm SiO_2 buffered Si.

2. Experimental

Four-inch Si p-type wafers were used in this study. A HF-vapor passivation was used to suppress the native oxide formation before other treatment. After the deposition, amorphous Al layer was thermally evaporated on wafers. The Al layer was oxidized at a temperature of 400 °C for 2 h to form 4 nm Al_2O_3 and finally annealed at 800 °C for 30 min in nitrogen ambient. More detailed fabrication process can be found in these researches [11,12]. In comparison with Al_2O_3, conventional thermal SiO_2 on Si was grown in oxygen ambient and annealed at 900 °C for 5 min. The size of memory window in MFIS structure is quite important as the value of Pr in MIM structure. In the previous researches, the size of memory window is linear presented with coercive field [16]. Based on the researches $Sr_{0.8}Bi_2Ta_2O_9$ has been chosen as the main component [17,18]. The deposition

* Corresponding author. Tel.: +886-3-5731818; fax: +886-3-5725490.
E-mail address: sychen@cc.nctu.edu.tw (S.Y. Chen).

0254-0584/02/$ – see front matter © 2002 Elsevier Science B.V. All rights reserved.
PII: S0254-0584(02)00517-5

process using strontium 2-ethylhexanotate [$Sr(C_8H_{15}O_2)_2$], bismuth 2-ethylhexanoate [$Bi(C_8H_{15}O_2)_2$], tantalum ethoxide [$Ta(OC_2H_5)_5$] as the metal-organic precursors. The SBT formula solution were prepared and with xylene as the solvent to adjust the concentration of the solution. The solutions with a mole ratio (Sr:Bi:Ta) of 0.8:2:2.0 were spin coated on both gate dielectrics at 4000 rpm for 30 s and then followed by subsequent drying. This procedure was repeated for several times to obtain the desired film thickness of 3500 Å. Between each coating, the wet films were pyrolyzed for several minutes. The as-deposited films were annealed at different temperatures from 600 to 900 °C for 30 min. The chemical composition of the films was determined using inductively coupled plasma (ICP). The molar number (Sr/Bi/Ta = 0.78/2.05/2.0) of Sr, Bi, and Ta in those films is very close to the composition (Sr/Bi/Ta = 0.8/2/2.0) in the precursor solution [19]. After that, the Al backside and Pt upper electrodes were formed by thermal evaporation. The device size of the fabricated MOS capacitor is 3.14×10^{-4} cm^2. The structure property of SBT films was analyzed by MAC Science M18XHF X-ray diffractometer with Cu Kα radiation. The thickness and surface morphology of the films was observed using Hitachi S-4000 scanning electron microscopy (SEM). The electrical and ferroelectric properties were characterized by *I–V* and *C–V* measurements using HP-4155B and HP-4284, respectively.

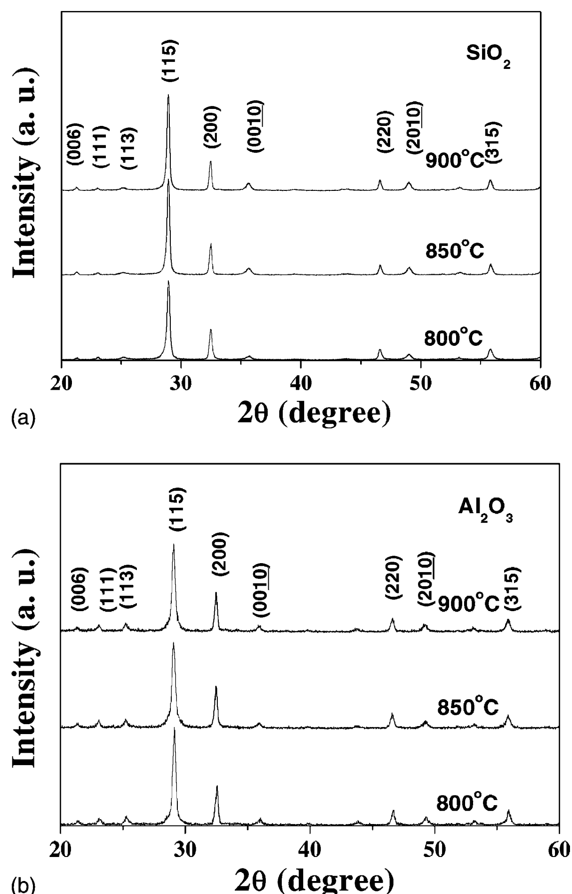

Fig. 1. XRD patterns of SBT on (a) 4 nm SiO_2/Si and (b) 4 nm Al_2O_3/Si.

3. Results and discussion

XRD studies of SBT films as a function of annealing temperature have indicated that the films annealed at 600 °C are amorphous. At 650 °C, SBT phase starts to develop and a broad diffraction peak of (1 1 5) appears around $2\theta \sim 28.5°$,indicating that the film is not fully crystallized. As the annealing temperature increased to 750 °C, the (1 1 5) peak in the XRD pattern becomes sharper. Fig. 1 shows the XRD patterns of SBT films on both Al_2O_3 and SiO_2 annealed at 800–900 °C. The relative intensity of (1 1 5) peak is much higher than any other orientations so that SBT films grown on both insulator are (1 1 5) oriented. The obtained SBT films on both insulators are polycrystalline and no second phases are detected even though the annealing temperature increases to 900 °C. In contrast, for the SBT films on Pt/Ti/SiO_2/Si, the pyrochlore phase was usually detected at the annealing temperature higher than 850 °C [20].

Figs. 2 and 3 illustrate the typical SEM surface images obtained from SBT on SiO_2/Si and Al_2O_3/Si, respectively. It is observed that these films are relatively uniform without cracks and the grain size of SBT thin films is strongly dependent on the annealing temperature. At 800 °C, the SBT grains on both cases are rod-like. The grain size of SBT films on SiO_2 insulator is much smaller than that on Al_2O_3 as shown in Figs. 2(a) and 3(a). As increasing annealing temperature to 900 °C, the morphology of the SBT films

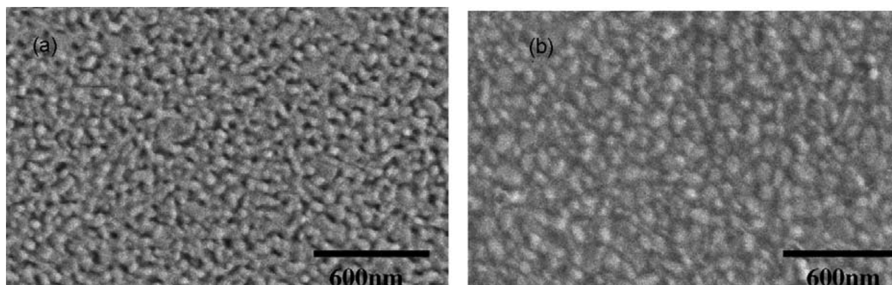

Fig. 2. SEM images of SBT on 4 nm SiO_2/Si annealed at (a) 800 °C and (b) 900 °C.

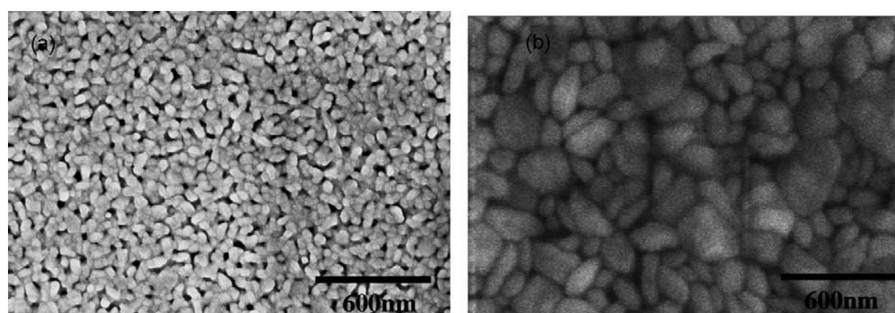

Fig. 3. SEM images of SBT on 4 nm Al_2O_3/Si annealed at (a) 800 °C and (b) 900 °C.

becomes different in both insulators. As shown in Figs. 2(b) and 3(b), the grains on both insulators become coarsening especially for the SBT films on Al_2O_3 insulator.

Fig. 4 shows the typical *C–V* curves of both SBT/Al_2O_3/Si and SBT/SiO_2/Si structure. The sweep voltages in this measurement change between +5 and −5 V back and forth at the frequency of 1 MHz. Clockwise hysteresis loops are observed, which indicates the switching of the ferroelectric polarization.

The good *C–V* characteristic of SBT films on Al_2O_3/SiO_2 at 1 MHz is observed and the dielectric constant of Al_2O_3 is about 9 that is two times larger than that of SiO_2. The good gate dielectric property would be further considered to integrate SBT thin films on Al_2O_3 gate dielectric. Fig. 5 shows the memory window of SBT capacitors on both Al_2O_3 and SiO_2 insulators at different annealing temperatures of 800, 850, and 900 °C, respectively. For the $Sr_{0.8}Bi_2Ta_2O_9$ capacitor in the both insulators, it was found that the memory window size increases with annealing temperature in the range of 800–900 °C. The width of memory window of SBT/Al_2O_3/Si capacitor is larger than that of SBT/SiO_2/Si capacitor. This improved ferroelectric property for the SBT films on Al_2O_3/Si may be due to the excellent diffusion barrier property of Al_2O_3 than SiO_2 as consistent with the report by Chin et al. that the low interface trap density and better reliability can be obtained using Al_2O_3 than SiO_2 as buffer layer of Si [21,22]. The atoms in SBT may diffuse into SiO_2 at the higher annealing temperature and degrades the ferroelectric property. This result is consistent with our previous work in 1T PZT/Al_2O_3 memory [11,12]. This further demonstrates that the memory window value is strongly dominated by the buffer layer of the SBT capacitors.

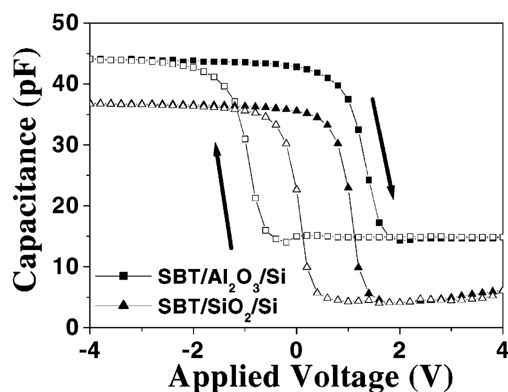

Fig. 4. *C–V* characteristics of both $Sr_{0.8}Bi_2Ta_2O_9$/Al_2O_3/Si and $Sr_{0.8}Bi_2Ta_2O_9$/SiO_2/Si structures annealed at 800 °C with program/erase voltages of ±5 V.

Fig. 6(a) and 6(b) show the annealing temperature dependent leakage current for SBT films on SiO_2 and Al_2O_3, respectively. The leakage current was measured with a hold time 0.5 s and delay time 0.5 s. In both cases, the leakage current shows a general decreasing trend as the annealing temperature increases. This result is probably attributed to the fact that the Al_2O_3 insulator layer becomes thickness with annealing temperature that makes the leakage current decrease. The current density of 3.4×10^{-7} and 3.2×10^{-8} A/cm^2 are measured at an applied voltage of −3 V for SBT/SiO_2 and SBT/Al_2O_3 at 800 °C, respectively. As the annealing temperature increases higher than 800 °C, i.e. 900 °C, the SBT/SiO_2 has relatively low current leakage (2.5×10^{-8} A/cm^2) compared to that (3.7×10^{-8} A/cm^2) of SBT/Al_2O_3. Since the grain morphology and size of SBT/SiO_2 and SBT/Al_2O_3 are quite similar at 800 °C, we may speculate that the SBT/Al_2O_3 capacitor has lower current leakage because Al_2O_3 insulator has larger bandgap than SiO_2. Because the leakage current of dielectric is the well known Fowler–Nordheim (F–N) tunneling at high field, the smaller leakage current is due to the additional large bandgap Al_2O_3 gate dielectric because F–N tunnel-

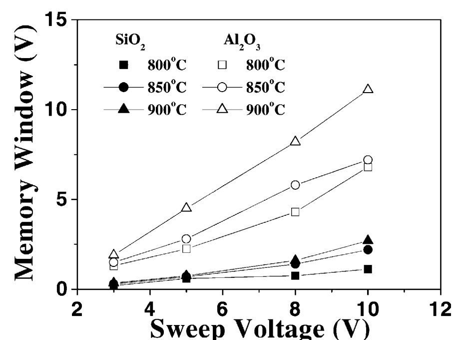

Fig. 5. Memory window of SBT/Al_2O_3/Si and SBT/SiO_2/Si capacitors as a function of annealing temperatures.

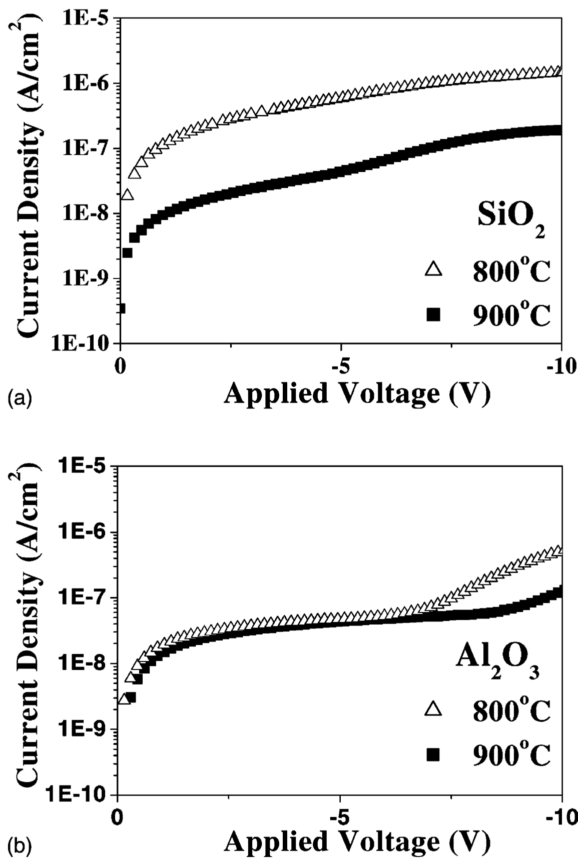

Fig. 6. Annealing temperature dependent *J–V* characteristics of SBT on (a) 4 nm SiO_2/Si and (b) 4 nm Al_2O_3/Si.

ing is exponentially dependent on bandgap according to following F–N equation:

$$J = \frac{q^3 E_D^2}{16\pi^2 \hbar \phi_D m_D^*} \exp\left(-\frac{4(2m_D^*)^{0.5}\phi_D^{3/2}}{3\hbar q E_D}\right)$$

where E_D, m_D^*, and ϕ_D are the dielectric electric field, effective mass and barrier height, respectively. Therefore, a lower leakage current can be obtained for the SBT/Al_2O_3 structure. On the other hand, at 900 °C, the grain size of SBT film on Al_2O_3 is bigger than that of SBT film on SiO_2 that may cause a slight increase in leakage current of the former structure compared to the latter structure. That is because the film with the larger grain size has fewer grain boundaries and presents rough surface that will result in a higher leakage current [23]. However, the leakage current is still low enough for advanced deep sub-μm application.

4. Conclusion

We have characterized the annealing temperature dependent integrity of SBT on ultra-thin Al_2O_3 and SiO_2 buffered Si. Over the wide range of annealing temperature, the SBT on ultra-thin Al_2O_3 has superior memory window than that of SiO_2 with the same thickness of 4 nm. At 800 °C, the leakage current of SBT/Al_2O_3 capacitor is about 3.2×10^{-8} A/cm^2 at −3 V which is still low enough for advanced deep sub-μm application.

References

[1] H. Watanabe, T. Mihara, H. Yoshimori, C.A. Paz de Aroujo, Jpn. J. Appl. Phys., Part 1 34 (1995) 5420.
[2] Y.T. Kim, D.S. Shin, Appl. Phys. Lett. 71 (1997) 3507.
[3] J.L. Moll, Y. Tarui, IEEE Trans. Electr. Devices, ED-10, 1963, p. 338.
[4] Y. Shichi, S. Tanimoto, T. Goto, K. Kuroiwa, Y. Tarui, Jpn. J. Appl. Phys. 33 (1994) 5172.
[5] S.Y. Wu, Ferroelectrics 11 (1976) 379.
[6] T. Hirai, K. Teramoto, T. Nishi, T. Goto, Y. Tarui, Jpn. J. Appl. Phys., Part 1 33 (1994) 5219.
[7] E. Tokumitsu, K. Itani, B.K. Moon, H. Ishiwara, Jpn. J. Appl. Phys., Part 1 34 (1995) 5202.
[8] T. Kanashima, M. Okuyama, Jpn. J. Appl. Phys., Part 1 38 (1999) 2044.
[9] Y.T. Kim, D.S. Shin, Appl. Phys. Lett. 71 (1997) 3507.
[10] Y. Matsui, M. Okuyama, M. Noda, Y. Hamakawa, Appl. Phys. A 28 (1982) 61.
[11] A. Chin, C.C. Liou, C.H. Lu, W.J. Chen, C. Tsai, in: Proceedings of the Symposium on VLSI Technology, 1999, p. 133.
[12] A. Chin, Y.H. Wu, S.B. Chen, C.C. Liao, W.J. Chen, in: Proceedings of the Symposium on VLSI Technology, 2000, p. 16.
[13] A. Chin, C.L. Sun, S.Y. Chen, M.Y. Yang, IEEE Electr. Device Lett. 22 (2001) 336.
[14] M.Y. Yang, S.B. Chen, A. Chin, C.L. Sun, B.C. Lan, S.Y. Chen, International Electron Devices Meeting (IEDM), Washington, DC, USA, December 2001.
[15] T. Mihara, H. Yoshimori, H. Watanabe, C.A. Paz de Araujo, Jpn. J. Appl. Phys., Part 1 34 (1995) 5233.
[16] T. Kanashima, M. Okuyama, Jpn. J. Appl. Phys. 38 (1999) 2044.
[17] T. Noguchi, T. Hase, Y. Miyakasa, Jpn. J. Appl. Phys. 35 (1996) 4900.
[18] H. Watanabe, T. Mihara, H. Yoshimori, C.A. Paz de Araujo, Jpn. J. Appl. Phys. 34 (1995) 5240.
[19] S.Y. Chen, V.C. Lee, J. Appl. Phys. 87 (2000) 8024.
[20] R. Dat, J.K. Lee, O. Auciello, A.I. Kingon, Appl. Phys. Lett. 67 (1995) 572.
[21] A. Chin, Y.H. Wu, S.B. Chen, C.C. Liao, W.J. Chen, in: Proceedings of the Symposium on VLSI Technology, US, June 2000, p. 19.
[22] A. Chin, C.C. Liao, C.H. Lu, W.J. Chen, C. Tsai, in: Proceedings of the Symposium on VLSI Technology, Japan, June 2000, pp. 133–134.
[23] M. Nayak, S.Y. Lee, T.Y. Tseng, Mater. Chem. Phys. 77 (2002) 34.