

Auger Recombination-Enhanced Hot Carrier Degradation in nMOSFETs With a Forward Substrate Bias

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Abstract—Enhanced hot carrier degradation in nMOSFETs with a forward substrate bias is observed. The degradation cannot be explained by conventional channel hot electron effects. Instead, an Auger recombination-assisted hot electron process is proposed. In the process, holes are injected from the forward-biased substrate and provide for Auger recombination with electrons in the channel, thus substantially increasing channel hot electron energy. Measured hot electron gate current and the light emission spectrum provide evidence that the high-energy tail of channel electrons is increased with a positive substrate bias. The drain current degradation is about ten times more serious in forward-biased substrate mode than in standard mode. The Auger-enhanced degradation exhibits positive temperature dependence and may appear to be a severe reliability issue in high temperature operation condition.

Index Terms—Auger recombination, forward substrate bias, hot carrier degradation, positive temperature dependence.

I. INTRODUCTION

THE REDUCTION of supply voltage in scaled CMOS devices is expected to alleviate hot carrier effects. However, impact ionization caused substrate current is still observable in MOS devices even at a drain bias below the band-gap voltage [1]. Several possible mechanisms are proposed for low-voltage hot carrier effects [2]–[4]. For examples, at a drain voltage below 2.0 V, electron-electron scattering may account for the high-energy tail of the electron energy distribution [2], [3]. The broadening of the electron energy levels due to electron-phonon interactions can also contribute to the high-energy tail [4]. Moreover, Auger recombination has been proposed to provide additional required energy for hot carrier degradation [5], [6]. In Auger process, one electron is recombined with a hole, and the released energy is transferred to another electron. This energy-transferred process is an effective electron energy gain mechanism especially at low drain bias.

The Auger-enhanced hot carrier effects can possibly occur in various device structures and operation conditions [6]–[10]. Fig. 1 illustrates different hole creation processes in a nMOSFET. In Fig. 1(a), holes are created due to impact ionization in the drain

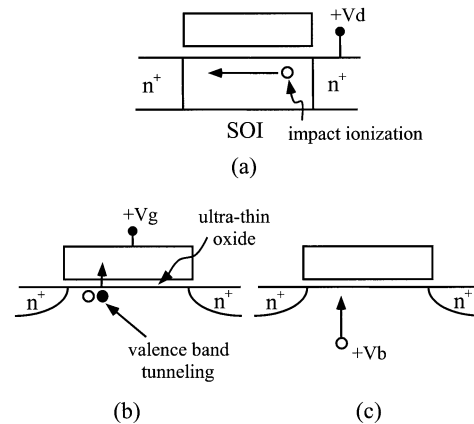


Fig. 1. Auger recombination process in various nMOSFET structures and operation conditions. (a) Impact ionization created holes flowing to the region near the source in a SOI MOSFET. (b) $+V_g$ induced valence-band electron tunneling in ultrathin MOSFETs and leaving holes in Si substrate. (c) Substrate hole injection to the channel by a positive substrate bias in FBS operation.

depletion region. These holes flow to the region near the source in a SOI structure [7] for Auger recombination with channel electrons. In ultrathin oxide nMOSFETs [Fig. 1(b)], a positive gate bias can cause valence-band electron direct tunneling to the gate and leave a hole behind in the channel for Auger process [8], [9]. In Fig. 1(c), a positive substrate bias is applied and holes are injected from the substrate to the channel [10]. The application of a positive substrate bias (V_b) in a nMOSFET has many advantages in analog and digital circuits. For example, in analog applications, better transistor matching and enhanced low-power analog performance can be achieved by applying a forward substrate bias [11]. Lower flicker noise is also obtained in such bias condition [12]. With respect to digital circuits, a novel concept of a dynamic threshold voltage nMOSFET (DTMOS) [13], [14] was proposed by applying a positive bias at the substrates. Higher on-state current and lower off-state leakage can be achieved simultaneously in DTMOS operation mode. In addition, a DTMOS with SOI substrate can extend the RF application of Si-based devices to even higher frequencies [15]. For utmost performance improvement, the substrate bias in a nMOSFET can be sometimes as large as 0.7 V [12], [16] or even above [17].

However, the reliability issue of a nMOSFET in forward-biased substrate (FBS) mode is rarely studied. In this paper, a comprehensive study of hot carrier degradation in FBS operation is conducted. We found that hot electron process in this

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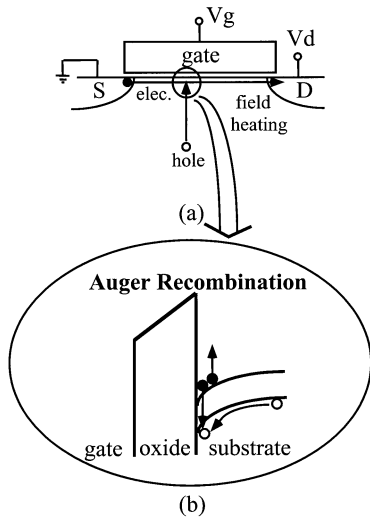


Fig. 2. Illustration of Auger recombination assisted hot electron energy gain process in FBS mode.

operation mode cannot be simply explained by channel field heating. Rather, Auger recombination-assisted electron energy gain plays an important part in the hot carrier process. In our model, holes are injected from positively biased substrate to the channel, as illustrated in Fig. 2(a). The injected holes provide for recombination with electrons in the inversion region and release the excess energy to other channel electrons. The process is depicted in Fig. 2(b). The energetic electrons arising from the Auger process are then accelerated by lateral electric field, thus resulting in a larger hot electron tail than in standard MOSFET operation with $V_b = 0$ V.

In this paper, Section II contains a brief description of device characterization. The measured hot electron gate current and photon luminescence spectrum are shown in Section III. These measurements confirm that the increase of the hot electron tail results from the FBS operation. Numerical simulation of the Auger recombination rate in the channel is included. In Section IV, Auger recombination-enhanced device degradation in FBS mode is characterized. The temperature and drain bias dependence of the Auger-enhanced degradation is investigated.

II. DEVICE CHARACTERIZATION

In this paper, a nMOSFET with a gate width of $100 \mu\text{m}$ and a gate length of $0.25 \mu\text{m}$ is used. The device has a gate oxide thickness about 50 \AA . Hot carrier luminescence is measured with a Hamamatsu C3230 single photon counting system [18]. The photon number at different wavelengths is counted individually. The measurement result is then corrected for the wavelength dependence of the filter transmittance. Fig. 3 shows the V_g -dependence of emitted light intensity and substrate current in FBS and standard operation modes. $V_d = 2.5$ V. Due to a strong correlation between light emission and substrate current, maximum I_b stress around $V_g = 1/2V_d$ is performed in both FBS and standard modes. Drain current in the triode region with $V_d = 0.1$ V is measured to monitor hot carrier degradation. The operation temperature is from room temperature to 125°C .

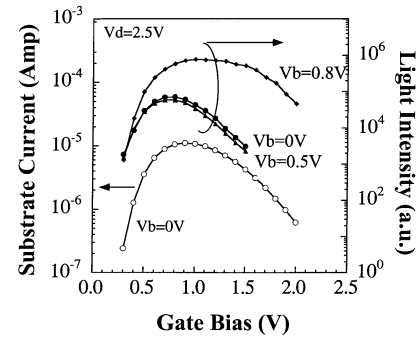


Fig. 3. Substrate current and photon light intensity as a function of gate bias with different substrate biases. $V_d = 2.5$ V. The bandpass filter is 800 nm .

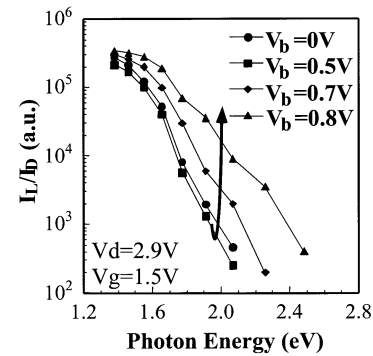


Fig. 4. Hot electron light emission spectra in a nMOSFET with different substrate biases. I_L represents the light intensity and I_D is the drain current.

III. AUGER RECOMBINATION-ENHANCED HOT ELECTRON DISTRIBUTION

It is well known that hot electron light emission in a MOSFET can be used to probe the electron energy distribution in the channel [19], [20]. Fig. 4 shows the light emission spectra in a nMOSFET with different substrate bias. The integration time is 100 s . The measured light intensity (I_L) is normalized to the drain current (I_D) to compensate for the different carrier flux in the channel due to the body effect. A turn-around feature is noticed in Fig. 4 as V_b increases from 0 to 0.8 V. I_L/I_D decreases initially and then increases with V_b . The reduction of I_L/I_D at $V_b = 0.5$ V is a consequence of a smaller drain lateral field due to the reduction of threshold voltage. The smaller accelerated field reduces hot electron energy and thus the corresponding light emission. As the substrate bias increases to 0.8 V, Auger effect plays a dominant role and the hot electron tail is enhanced considerably even though the drain acceleration field is smaller.

In addition to hot electron luminescence, the gate injection current is enhanced by a positive substrate bias. The gate current injection at different substrate bias is plotted in Fig. 5. Again, the gate current is normalized by the drain current. Similarly, the gate current first decreases and then increases as V_b changes from 0 to 0.8 V. Fig. 6 shows the hot electron gate current for various drain and substrate biases. In this figure, the hot electron gate current is dependent on both drain and substrate biases. The drain bias determines lateral field heating while the substrate bias gives rise to the Auger effect. The dependence of the gate

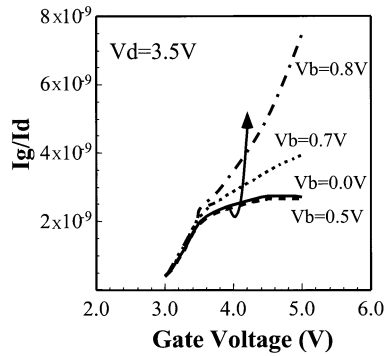


Fig. 5. Normalized gate current versus gate voltage in a nMOSFET with different substrate biases. The measurement drain bias is 3.5 V.

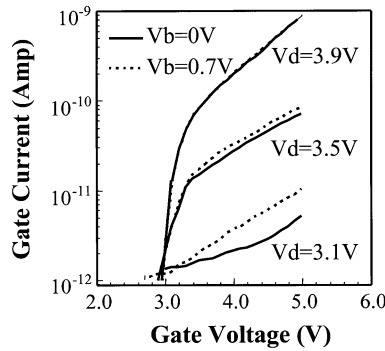


Fig. 6. Hot electron gate injection current versus gate voltage with different drain bias.

current on both drain and substrate biases implies that the electron energy gain process in FBS mode is due to combined Auger recombination and drain field acceleration. It should be pointed out that the substrate bias effect becomes more pronounced at a smaller drain bias in Fig. 6. The reason is that channel field acceleration itself at a low drain bias is not enough to provide electrons with sufficient energy to overcome the gate oxide barrier.

In order to evaluate the dependence of the Auger effect on substrate bias, a numerical analysis of Auger recombination rate in the channel is performed. The Auger recombination rate is expressed as follows [6]:

$$R_{AU} = C_0[n^2p] \quad (1)$$

where the Auger coefficient C_0 is about 10^{-31} cm^6/s . n and p denote electron and hole concentrations and vary with position. The electron and hole distributions at the Si-SiO₂ surface are obtained from a two-dimensional (2-D) device simulation. Fig. 7 shows the calculated Auger recombination rate along the channel. The corresponding lateral electric field is also drawn in the figure. The x -axis is the distance from the source junction. Auger recombination occurs for the most part near the source side because substrate hole injection is largest there. Note that the lateral electric field slightly decreases as the substrate voltage increases from 0.5 to 0.8 V, whereas the Auger recombination rate increases by orders of magnitude due to the exponential dependence of hole injection on substrate bias. The energetic electrons created by Auger recombination near the source side are subsequently accelerated by lateral electric field near the drain side, thus, causing a larger hot electron tail.

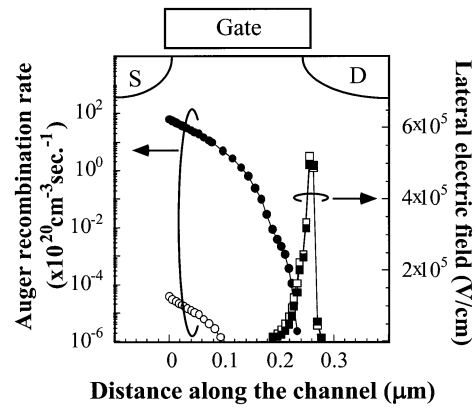


Fig. 7. Simulated Auger recombination rate and lateral electric field along the channel. $V_d = 2.9$ and $V_g = 1.5$ V. Open symbol and full symbol represent simulation under $V_b = 0.5$ and $V_b = 0.8$ V, respectively.

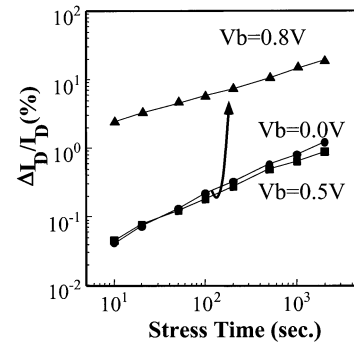


Fig. 8. Linear drain current degradation as a function of stress time. Drain current is measured at $V_g = 2.0$ and $V_d = 0.1$ V. Stress drain bias is 2.9 V and gate bias is 1.5 V.

IV. ENHANCED HOT CARRIER DEGRADATION

To demonstrate the Auger effect on device hot carrier reliability, the linear drain current degradation versus stress time is shown in Fig. 8 for different substrate bias. The drain current degradation is increased by one order of magnitude when substrate bias increases from 0 to 0.8 V. In addition, the drain current degradation exhibits a turn-around phenomenon, as noticed in hot electron luminescence measurement (Fig. 4). For analog applications, we compare the flicker noise degradation in standard hot carrier stress and in FBS stress. Since hot carrier stress induced noise degradation is larger in the triode region [21], the flicker noise measured at $V_g = 2$ and $V_d = 0.1$ V is shown in Fig. 9. The flicker noise degradation in FBS mode is enhanced by several times. This is because the FBS mode has a larger hot electron tail and thus causes more serious flicker noise degradation.

The temperature effect on the Auger enhanced degradation is also investigated. Fig. 10(a) and (b) compares the temperature dependence of hot electron gate current in standard mode and in FBS mode. V_d is 3.5 V in measurement. As expected, the gate current in standard mode has negative temperature dependence because of increased phonon scattering at higher temperature [22]. However, the gate current in FBS mode shows reversed I_g -temperature dependence. The reason for the positive temperature dependence is twofold. First, the substrate hole injection increases with temperature. Second, the Auger coefficient itself

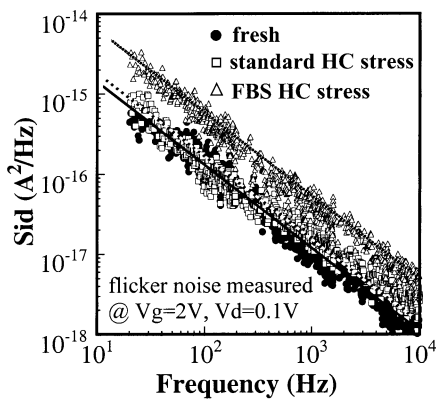


Fig. 9. Drain current noise power spectra S_{id} of a nMOSFET in different stress conditions. Flicker noise is measured at $V_g = 2.0$ and $V_d = 0.1$ V. Stress drain bias is 2.9 V and gate bias is 1.5 V. V_b is 0 V in standard hot carrier stress and is 0.8 V in the FBS stress.

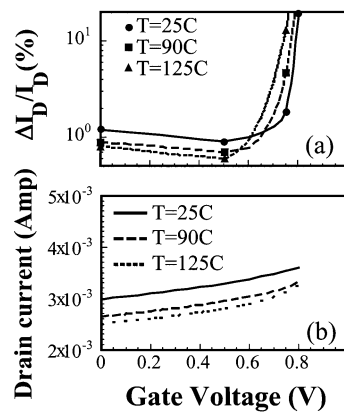


Fig. 12. (a) Substrate bias effect on drain current degradation and (b) the corresponding stress drain current, measured at different stress temperatures. The stress time is 2000 s, and the stress $V_g = 1.5$ and $V_d = 2.9$ V.

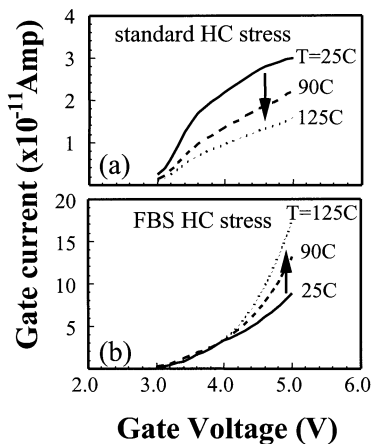


Fig. 10. Temperature dependence of hot electron gate current at (a) $V_b = 0$ V and (b) $V_b = 0.8$ V. The drain bias is 3.5 V.

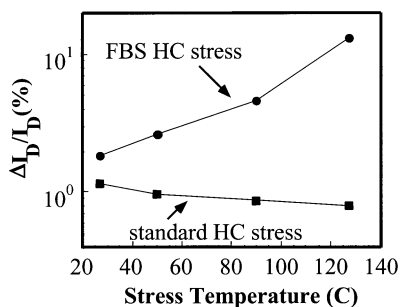


Fig. 11. Temperature dependence of linear drain current degradation. The stress time is 2000 s, and stress $V_g = 1.5$ and $V_d = 2.9$ V.

exhibits positive temperature dependence [23]. The temperature effect on drain current degradation is shown in Fig. 11. As opposed to the standard hot carrier stress, temperature accelerated degradation is observed in FBS mode with stress $V_d = 3.5$ V. The degradation is enhanced by eight times from $T = 25$ to 125 °C. This point is particularly significant to device reliability since today's high performance components are required to operate in such high temperature range. The substrate bias dependence of drain current degradation is shown in Fig. 12. The

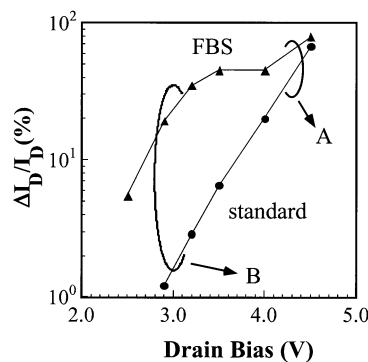


Fig. 13. Linear drain current degradation as a function of stress drain bias. The stress time is 2000 s and $T = 25$ °C. The stress V_g is chosen at max. I_b stress.

measured result shows opposite temperature dependence in the low V_b region and in the high V_b region. In the low V_b region, Auger effects are negligible and field heating is the dominant electron energy gain process. In the high V_b region, the Auger effect plays a major role in the electron energy gain process. The critical V_b for the onset of the Auger enhanced degradation becomes smaller as temperature increases. For example, the V_b threshold for the Auger induced degradation is around 0.5 V at 125 °C. Once the applied substrate bias is above this critical voltage, the device degradation increases exponentially with V_b . In other words, the substrate bias appropriate for FBS operation should be limited to 0.5 V from the viewpoint of device reliability.

To further understand the role of the Auger effect, we evaluate the drain bias dependence of the Auger enhanced degradation. The result is shown in Fig. 13. At a relatively high drain bias (region A), drain field acceleration itself can provide sufficient energy for Si-H bond breaking and interface trap generation. The degradation in FBS mode and in standard mode therefore does not exhibit much difference. At a medium drain bias (region B), electrons by field acceleration only cannot acquire sufficient energy to break Si-H bonds. The combined Auger recombination and channel field heating process is necessary to provide sufficient energy. As a result, Auger-enhanced degradation is much larger than standard hot carrier stress in this bias region.

V. CONCLUSION

The substrate bias effect on hot carrier reliability in FBS operation mode has been investigated. A new hot carrier degradation mechanism, attributed to an Auger recombination enhanced hot electron process, is proposed. This Auger enhanced degradation exhibits positive temperature dependence and is more significant at a lower supply voltage. This new degradation mode may bring about a major reliability concern in high temperature operation and imposes a limitation on the applied substrate bias.

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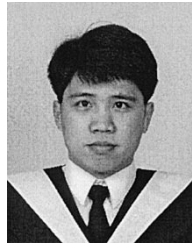
REFERENCES

- [1] K. G. Anil, S. Mahapatra, and I. Eisele, "Role of inversion layer quantization on sub-bandgap impact ionization in deep-sub-micron n-channel MOSFETs," in *IEDM Tech. Dig.*, 2000, pp. 675–678.
- [2] A. Abramo, C. Fiegna, and F. Venturi, "Hot carrier effects in short MOSFET's at low applied voltages," in *IEDM Tech. Dig.*, 1995, pp. 301–304.
- [3] A. Ghetti, L. Selmi, R. Bez, and E. Sangiorgi, "Monte Carlo simulation of low voltage hot carrier effects in non volatile memory cells," in *IEDM Tech. Dig.*, 1996, pp. 379–382.
- [4] J. Tang and K. Hess, "Theory of hot electron emission from silicon into silicon dioxide," *J. Appl. Phys.*, vol. 54, pp. 5145–5151, 1983.
- [5] E. Sangiorgi, B. Ricco, and P. Olivo, "Hot electrons and holes in MOSFET's biased below the Si-SiO₂ interfacial barrier," *IEEE Electron Device Lett.*, vol. EDL-6, pp. 513–515, 1985.
- [6] B. Ricco, E. Sangiorgi, and D. Cantarelli, "Low-voltage hot-electron effects in short channel MOSFETs," in *IEDM Tech. Dig.*, 1984, pp. 92–95.
- [7] M. Yamaji, K. Taniguchi, C. Hamaguchi, K. Sukegawa, and S. Kawamura, "Degradation mechanisms of thin film SIMOX SOI-MOSFET characteristics-optical and electrical evaluations," *IEICE Trans. Electron.*, vol. E77-C, pp. 373–378, 1994.
- [8] C. W. Tsai, S. H. Gu, L. P. Chiang, T. Wang, Y. C. Liu, L. S. Huang, M. C. Wang, and L. C. Hsia, "Valence-band tunneling enhanced hot carrier degradation in ultra-thin oxide nMOSFETs," in *IEDM Tech. Dig.*, 2000, pp. 139–142.
- [9] W. K. Yeh, W. H. Wang, Y. K. Fang, and F. L. Yang, "Temperature dependence of hot-carrier-induced degradation in 0.1 μ m SOI nMOSFET's with thin oxide," *IEEE Electron Device Lett.*, vol. 23, pp. 425–427, July 2002.
- [10] L. P. Chiang, C. W. Tsai, T. Wang, U. C. Liu, M. C. Wang, and L. C. Hsia, "Auger recombination enhanced hot carrier degradation in nMOSFET's with positive substrate bias," in *Symp. VLSI Tech.*, 2000, pp. 132–133.
- [11] J. A. Babcock, P. Francis, H. Haggag, J. Darmawan, T. W. Lee, P. Lindorfer, C. Olgaard, R. B. Merrill, and D. K. Schroder, "Effect of body-to-source bias on the analog characteristics of 0.35 μ m partially depleted SOI CMOS for low-voltage low-power mixed-mode applications," in *IEEE Int. SOI Conf.*, 1998, pp. 25–26.
- [12] T. L. Hsu, D. D. Tang, and J. Gong, "Low-frequency noise properties of dynamic-threshold (DT) MOSFET's," *IEEE Electron Device Lett.*, vol. 20, pp. 532–534, Oct. 1999.
- [13] F. Assaderaghi, D. Sinitsky, S. A. Parke, J. Bokor, P. K. Ko, and C. Hu, "Dynamic threshold-voltage MOSFET (DTMOS) for ultra-low voltage VLSI," *IEEE Tran. Electron Devices*, vol. 44, pp. 414–422, Mar. 1997.
- [14] H. Kotaki, S. Kakimoto, M. Nakano, T. Matsuoka, K. Adachi, K. Sugimoto, T. Fukushima, and Y. Sato, "Novel bulk dynamic threshold voltage MOSFET (B-DTMOS) with advanced isolation (SITOS) and gate to shallow-well contact (SSS-C) process for ultra low power dual gate CMOS," in *IEDM Tech. Dig.*, 1996, pp. 459–462.
- [15] Y. Momiyama, T. Hirose, H. Kurata, K. Goto, Y. Watanabe, and T. Sugii, "A 140 GHz ft and 60 GHz fmax DTMOS integrated with high-performance SOI logic technology," in *IEDM Tech. Dig.*, 2000, pp. 451–454.
- [16] I. Y. Chung, Y. J. Park, and H. S. Min, "A new SOI inverter for low power applications," in *IEEE Int. SOI Conf.*, 1996, pp. 20–21.
- [17] C. Y. Chang, J. G. Su, H. M. Hsu, S. C. Wong, T. Y. Huang, and Y. C. Sun, "Investigations of bulk dynamic threshold-voltage MOSFET with 65 GHz 'normal-mode' ft and 220 GHz 'over-drive mode' ft for RF applications," in *Symp. VLSI Tech.*, 2001, pp. 89–90.
- [18] E. Inuzuka and H. Suzuki, "Emission microscopy in semiconductor failure analysis," in *IMPC*, 1994, pp. 1492–1496.
- [19] A. Toriumi, M. Yoshimi, M. Iwase, Y. Akiyama, and K. Taniguchi, "A study of photon emission from n-channel MOSFET's," *IEEE Trans. Electron Devices*, vol. 34, pp. 1501–1508, 1987.
- [20] M. Lanzoni, E. Sangiorgi, C. Fiegna, M. Manfredi, and B. Ricco, "Extended (1.1–2.9eV) hot-carrier-induced photon emission in n-channel Si MOSFET's," *IEEE Electron Device Lett.*, vol. 12, pp. 341–343, June 1991.
- [21] R. Brelerdow, W. Weber, D. Schmitt-Landsiedel, and R. Thewes, "Hot carrier dependence of the low-frequency noise in MOS transistors under analog and RF operating conditions," *IEEE Trans. Electron Devices*, vol. 49, pp. 1588–1596, Sept. 2002.
- [22] D. Esseni, L. Selmi, E. Sangiorgi, R. Bez, and B. Ricco, "Temperature dependence of gate and substrate currents in the CHE crossover regime," *IEEE Electron Device Lett.*, vol. 16, pp. 506–508, Dec. 1995.
- [23] L. Huld, N. G. Nilsson, and K. G. Svantesson, "The temperature dependence of band-to-band Auger recombination in silicon," *Appl. Phys. Lett.*, vol. 35, pp. 776–777, 1979.



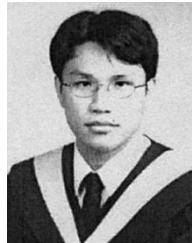
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