Substrate-Triggered Technique for On-Chip ESD Protection Design in a 0.18-μm Salicided CMOS Process

Ming-Dou Ker, *Senior Member, IEEE,* and Tung-Yang Chen, *Associate Member, IEEE*

***Abstract*—The substrate-triggered technique for input, output, and power-rail electrostatic discharge (ESD) protection, as comparing to the traditional gate-driven technique, has been proposed to effectively improve ESD robustness of IC products. With the substrate-triggered technique, on-chip ESD protection circuits for the input, output, and power pins have been designed and verified in a 0.18-μm salicided CMOS process. The experimental results have confirmed that the proposed substrate-triggered design can effectively and continually improve ESD robustness of CMOS devices. The human-body-model (HBM) ESD robustness of NMOS with a device dimension of $W/L = 300$ μm/0.3 μm can be improved from the original 0.65 kV with the traditional gate-driven design to become 3.2 kV with the proposed substrate-triggered design.**

***Index Terms*—Electrostatic discharge (ESD), ESD protection circuits, gate-driven technique, second breakdown, substrate-triggered technique.**

I. Introduction

TO SUSTAIN reasonable electrostatic discharge (ESD) robustness in deep-submicron CMOS ICs, on-chip ESD protection circuits must be added into the chips [1], [2]. The ESD level of commercial IC products is generally required to be higher than 2 kV in human-body-model (HBM) ESD stress [3]. The typical on-chip ESD protection circuits in a CMOS IC to effectively protect internal circuits against ESD damage is shown in Fig. 1 [4]. In order to sustain the required ESD level, on-chip ESD protection circuits are often drawn with larger device dimensions, which are often realized with multiple fingers in a layout designed to reduce total layout area [5], but during ESD stress, the multiple fingers of ESD protection MOSFET cannot be uniformly turned on. Only several fingers of the MOSFET were turned on and therefore damaged by ESD [6]–[8]. This often causes a low ESD level in an ESD protection circuit, even if the MOSFET has a large device dimension.

To improve turn-on uniformity among the multiple fingers of NMOS, the gate-driven design [9]–[11] or substrate-triggered design [12]–[15] had been reported to increase ESD robustness of NMOS with large device dimension. Recently, ESD robustness of the gate-driven NMOS had been found to be decreased dramatically when the gate voltage is somewhat increased [8], [10]. The gate-driven design causes ESD current to mainly crowd and discharge through the surface channel of NMOS; therefore, NMOS is easily burned out by ESD energy to cause the sudden degradation on ESD level of the gate-driven devices [8].

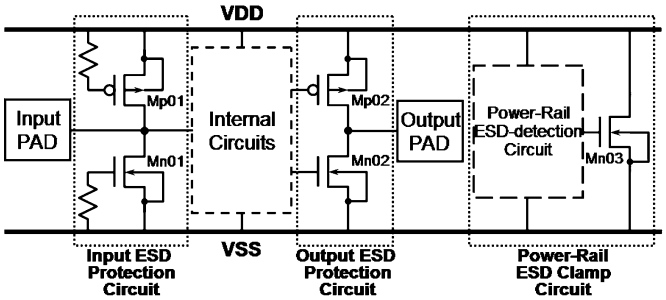

Fig. 1. Typical on-chip ESD protection circuits in a CMOS IC.

In this paper, the substrate-trigger effect on MOSFET devices for ESD protection has been investigated in detail with the dc current–voltage (*I–V*) curve and TLP-measured second breakdown current (It_2). On-chip ESD protection circuits for input, output, and power rails are designed with this substrate-triggered technique [16]. The proposed ESD protection circuits have been verified in a 0.18-μm salicided CMOS process to successfully improve ESD robustness of the I/O cells.

II. Substrate-Triggered Device

A. Structure of Substrate-Triggered ESD Protection Device

The device cross-sectional views and the corresponding finger-type layout patterns of the traditional gate-driven and the new proposed substrate-triggered NMOSs are shown in Fig. 2(a) and (b), respectively. The physical gate-oxide thickness of those devices is about $\sim$35 Å in the 0.18-μm 1.8-V salicided CMOS process. Such thin gate-oxide NMOSs with different channel widths but a fixed channel length of 0.3-μm and a fixed unit finger length of 25-μm had been fabricated in a 0.18-μm salicided CMOS process [17] with an extra silicide-blocking mask to block the silicided diffusion. The clearances from the contact to poly-gate edge in the drain and source diffusions of the traditional finger-type NMOS in Fig. 2(a) are 3-μm and 1-μm, respectively. The clearances from the contact to poly-gate edge on the drain and source diffusions

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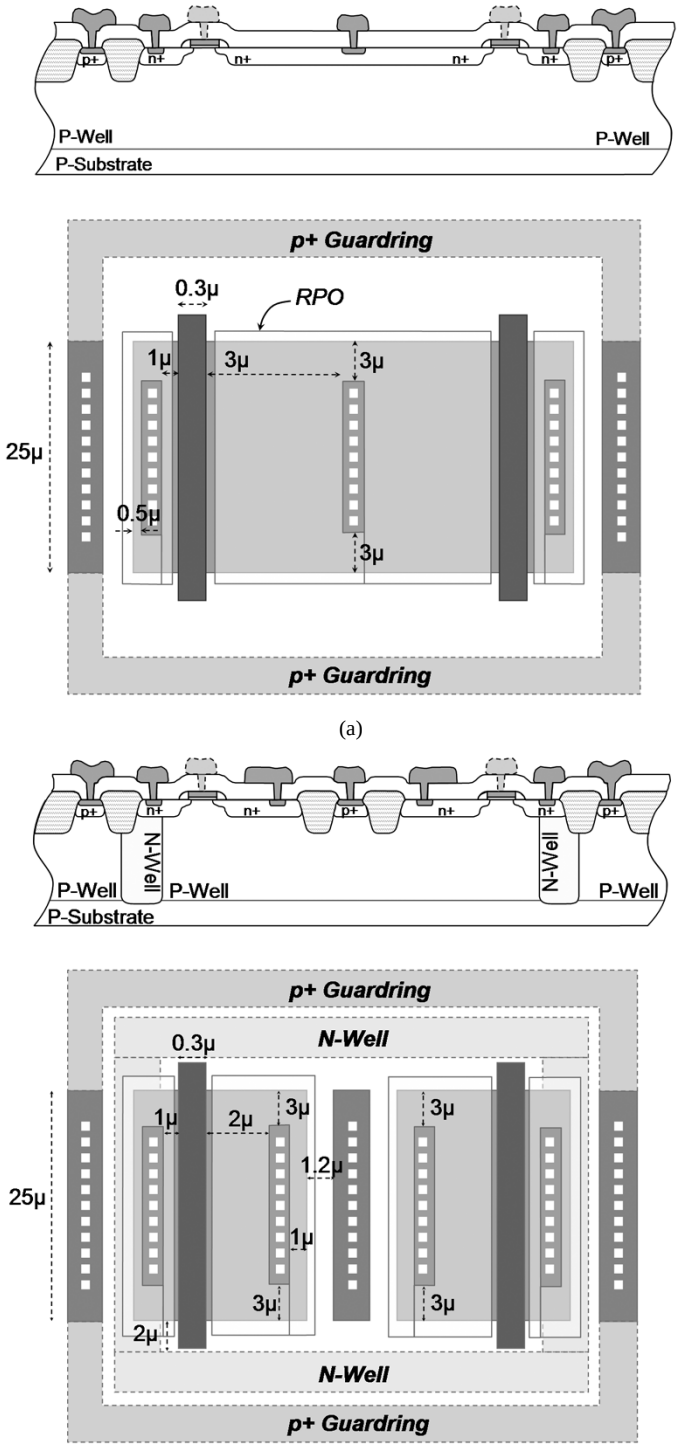


Fig. 2. Device structures and corresponding layout patterns of (a) the traditional finger-type NMOS and (b) the proposed substrate-triggered NMOS, for ESD protection.

of the substrate-triggered NMOS in Fig. 2(b) are drawn as 2-μm and 1-μm to save layout area, respectively. In Fig. 2(b), a p+ diffusion is located at the center of NMOS layout, which is used as the substrate-triggered node of ESD protection device. An additional N-well ring locating under the source regions and surrounding the whole device, as shown in Fig. 2(b), is used to form a larger equivalent substrate resistance for more effective substrate-triggered performance.

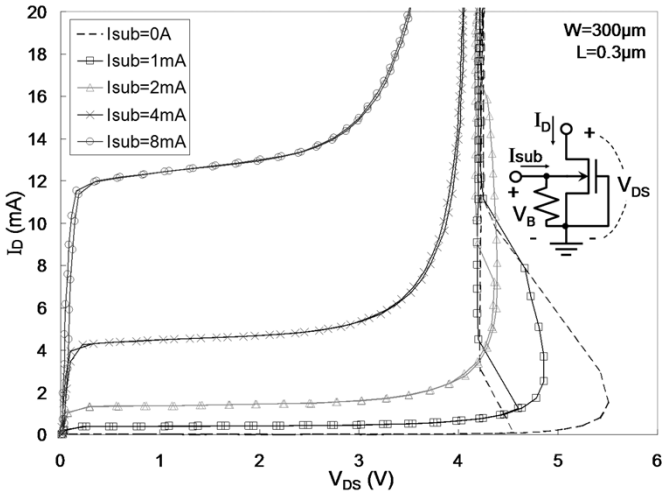
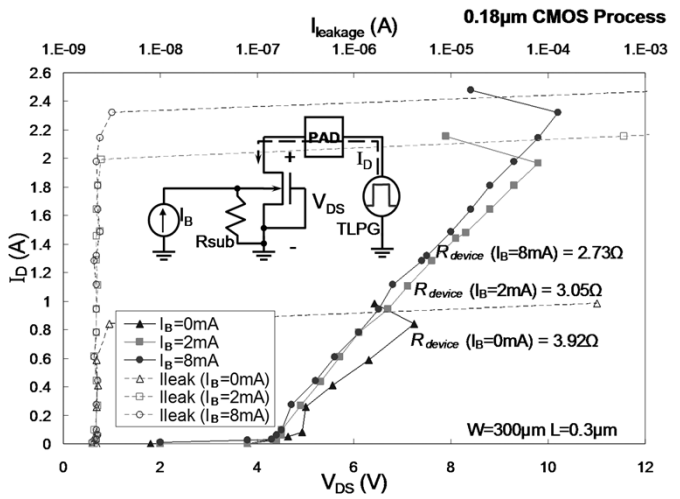


Fig. 3. DC *I–V* curves of the substrate-triggered NMOS under different substrate current biases.

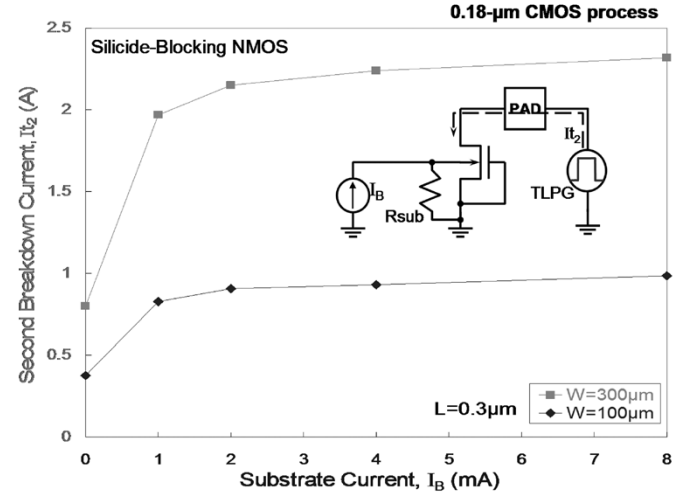
B. Characteristics of Substrate-Triggered Device

The dc *I–V* curves of the fabricated substrate-triggered NMOS with $W/L = 300$ μm/0.3 μm under different substrate biases are measured in Fig. 3. The original trigger voltage and holding voltage of the substrate-triggered NMOS without substrate bias are 5.5 and 4 V, respectively. The substrate current can lower the trigger voltage of NMOS, which can improve turn-on efficiency of NMOS during ESD stress.

To investigate the device behavior during high ESD current stress, a transmission line pulsing (TLP) technique has been widely used to measure the second breakdown characteristics of devices [18], [19]. The transmission line pulse generator (TLPG) with a pulse width of 100 ns is used to find the It_2 (second breakdown current) of the fabricated NMOSs under different substrate-biased currents. The TLP-measured *I–V* characteristics of substrate-triggered NMOS ($W/L = 300$ μm/0.3 μm) under substrate biases of 0, 2, and 8 mA are shown in Fig. 4(a). The corresponding leakage currents in Fig. 4(a) are measured, after each TLP pulse stress, on the drain of gate-grounded NMOS under the bias conditions of $V_{DS} = 1.8$ V and no substrate-biased current. The turn-on resistance is decreased from 3.92 to 2.73 Ω, while the substrate-biased current is increased from 0 to 8 mA. The substrate bias can change the turn-on resistance of substrate-triggered NMOS during ESD stress. This implies that the substrate bias can modulate the effective turn-on area or turn-on path of parasitic lateral BJT in the NMOS to have higher ESD robustness [8], [20]. The dependence of It_2 on the substrate-biased current of NMOS devices with different channel widths in a 0.18-μm salicided CMOS process is shown in Fig. 4(b). The second breakdown currents of the substrate-triggered NMOSs with $W = 300$ or $W = 100$ μm can be continually increased by the substrate bias. The It_2 of NMOS with a channel width of 300 μm without substrate-triggered current is only 0.8 A, but it can be increased up to 2.2 A, while the NMOS has a substrate-triggered current of 2 mA. With a higher It_2, the NMOS can sustain a higher ESD level. While the substrate-triggered current is increased to 8 mA, the It_2 in Fig. 4(b) is not degraded. Therefore, the



(a)



(b)

Fig. 4. (a) TLP-measured *I–V* curves and turn-on resistances of the substrate-triggered NMOS devices in a 0.18-μm salicided CMOS process. (b) The dependence of It_2 on the substrate-biased current of NMOS with different channel widths.

substrate-triggered technique can continually improve ESD robustness of NMOS, without causing the sudden degradation on its ESD robustness that happened in the gate-driven NMOS [8], [10].

III. On-Chip ESD Protection Circuits With Substrate-Triggered Design

Since the ESD events may have positive or negative ESD voltage on an input (or output) pin with the VDD or VSS pins relatively grounded, there are four ESD-stress conditions on an input (or output) pin [3], [11]. Generally, the traditional I/O ESD protection circuits in Fig. 1 have the lowest ESD levels under the positive-to-VSS and negative-to-VDD ESD-stress conditions, because the protection devices in these two ESD-stress conditions are often operated in the reverse-biased breakdown condition. Thus, the proposed substrate-triggered design is used to significantly improve ESD robustness of ESD protection circuits in these two worst ESD-stress conditions.

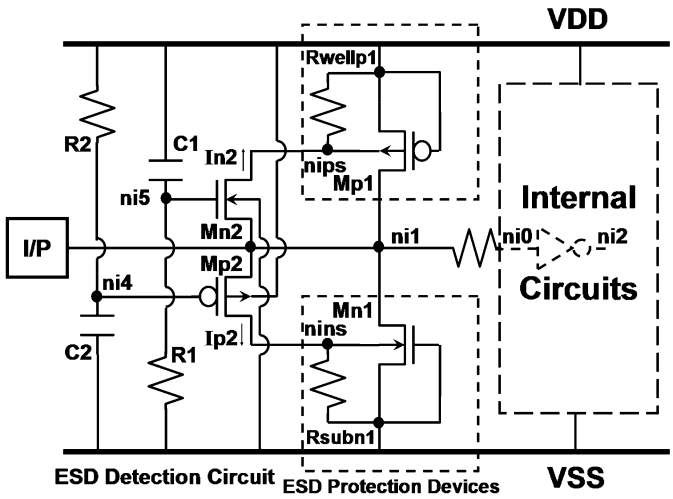


Fig. 5. Proposed input ESD protection circuit with substrate-triggered design.

A. Input ESD Protection Circuits With Substrate-Triggered Design

The input ESD protection circuit with the substrate-triggered design is shown in Fig. 5. The ESD detection circuits with resistors ($R1$ and $R2$), capacitors ($C1$ and $C2$), and NMOS/PMOS ($Mn2/Mp2$) connected in Fig. 5 are used to detect the ESD events, and then to generate substrate-triggered current to turn on ESD protection devices ($Mn1$ and $Mp1$). The ESD protection devices are kept off when the IC is under the normal circuit operating condition. To meet these requirements, the RC time constant in the ESD detection circuit is designed about 0.1$\sim$1 μs to achieve the desired operations.

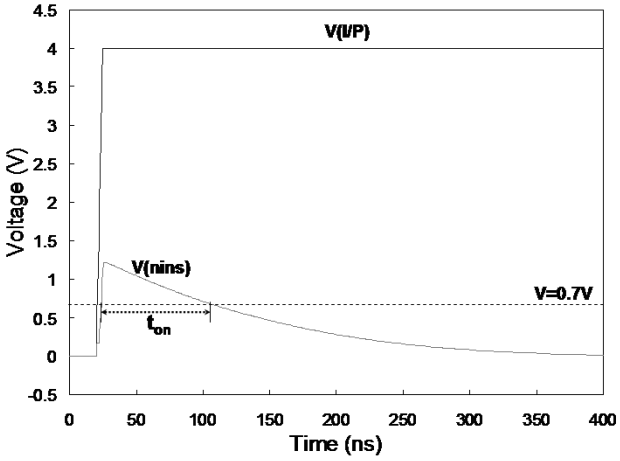
During positive-to-VSS ESD stress (VDD power pin is floating), the nodes ni4 and nins in Fig. 5 have the initial voltage levels the same as VSS. The positive-to-VSS ESD voltage across the input pad and VSS power line will be conducted into the VDD power line through the parasitic drain-to-well diode of PMOS ($Mp1$), and to charge up the node ni4 of the capacitor $C2$. The HBM ESD voltage has a rise time about $\sim$10 ns [3]. The voltage level at the node ni4 is increased much slower than the voltage level on the input pad, because the $R2$–$C2$ circuit has a time constant of microsecond. Due to the delay of voltage increase on the node ni4, $Mp2$ device with a $\sim$0-V gate voltage is turned on by the positive ESD voltage at the pad and conducts a current $Ip2$ into the node nins to trigger on the ESD protection NMOS ($Mn1$). The triggered-on NMOS provides a low-impedance path to discharge the ESD current from the input pad to VSS. Because the substrate-triggered NMOS is turned on by a positive substrate current rather than by the drain snapback breakdown, the NMOS can be turned on at lower voltage to discharge ESD current before the internal circuits are damaged by the overstress ESD voltage. So, the internal circuits can be effectively protected by the proposed ESD protection circuits with substrate-triggered technique.

During the negative-to-VDD ESD stress (VSS power pin is floating), the nodes ni5 and nips in Fig. 5 have the initial voltage levels the same as VDD, which is grounded under such a ESD stress. The negative-to-VDD ESD voltage across the

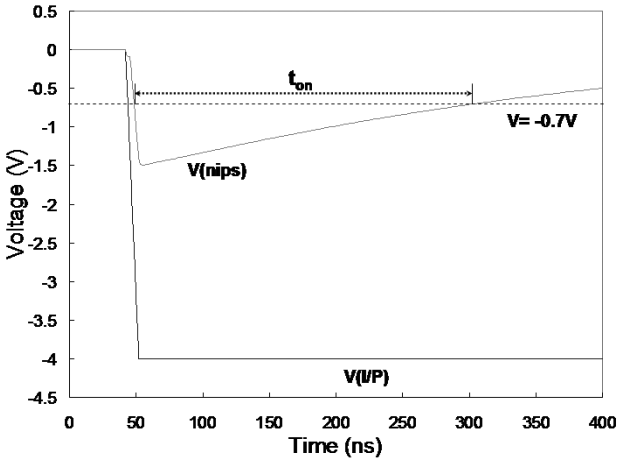
input pad and VDD power line will be conducted to the floating VSS power line through the parasitic drain-to-substrate diode of NMOS ($Mn1$), and charge the node ni5 of the capacitor $C1$ to a negative voltage level. Due to the delay of voltage decrease on the node ni5, the Vgs of $Mn2$ is greater than its threshold voltage during such a negative-to-VDD ESD stress. So, the $Mn2$ device is turned on by the ESD voltage and conducts a negative current $In2$ into the node nips to trigger on the ESD protection PMOS ($Mp1$). The ESD protection PMOS is turned on by a triggering current in its N-well rather than by the drain snapback breakdown. So, the PMOS can be turned on with a faster speed to discharge ESD current before the internal circuits are damaged by the overstress negative ESD voltage.

To meet the aforementioned circuit operations, the HSPICE is used to find the suitable RC value and device sizes in the ESD detection circuit, which are chosen as $R1 = R2 = 10$ kΩ, $C1 = C2 = 20$ pF, and W/L of $Mp2$ ($Mn2$) $= 20$ μm/0.8 μm. The HSPICE simulated voltage waveforms in time domain at the node nins during the positive-to-VSS ESD stress is shown in Fig. 6(a). The simulated voltage waveforms in the time domain at the node nips during the negative-to-VDD ESD stress is shown in Fig. 6(b). In Fig. 6(a), a ramp voltage with a rise time of 10 ns is used to simulate the rising edge of an HBM ESD pulse in the positive-to-VSS ESD-stress condition. The ESD detection circuit should be designed to generate the triggering current into the substrate-triggered NMOS (or PMOS), before the ESD protection NMOS (or PMOS) is broken down by the ESD voltage. Because the NMOS has a snapback-breakdown voltage of $\sim$5.5 V in the 0.18-μm CMOS process, the pulse height of the ramp voltage in this simulation is set as 4 V to monitor the voltage on the node nins before the ESD protection NMOS is broken down. As shown in Fig. 6(a), the voltage waveform on the node nins is simultaneously increased when the ramp voltage is applied to the input pad, whereas the VSS is grounded and VDD is floating. By changing the RC time constant or the device size of $Mp2$, the turn-on time $(t_{\rm on})$ of ESD protection NMOS can be adjusted. In Fig. 6(b), a negative ramp voltage with a fall time of 10 ns is used to simulate the falling edge of a negative HBM ESD pulse in the negative-to-VDD ESD-stress condition. As shown in Fig. 6(b), the voltage waveform on the node nips is simultaneously decreased when the negative ramp voltage is applied to the input pad, whereas the VDD is grounded and VSS is floating. Because NMOS $Mn2$ has a higher driving current than that of PMOS $Mp2$ in the ESD detection circuit, the simulated turn-on time $(t_{\rm on})$ in Fig. 6(b) is longer than that in Fig. 6(a). If the device dimension of $Mp2$ is increased, the turn-on time $(t_{\rm on})$ in Fig. 6(a) can be further increased. The dependence of turn-on time $(t_{\rm on})$ on the device dimension of $Mp2$ or $Mn2$ is shown in Fig. 7. The turn-on time can be modified by changing the device dimension of $Mp2$ or $Mn2$ or by changing the RC time constant in the ESD detection circuit. The turn-on time of the ESD protection device is designed about $\sim$200 ns to meet the half-energy discharging time of the HBM ESD waveform [3].

When the IC is in the normal circuit operating condition with the power supplies, the node ni4 (ni5) is biased at VDD (VSS) through the resistor $R2$ ($R1$) to turn off the $Mp2$ ($Mn2$). Therefore, the substrate-triggered ESD protection NMOS (PMOS) is guaranteed to be kept off. The device dimension of ESD protection NMOS (PMOS) is adjusted to meet the required ESD level within a specified layout area.



(a)



(b)

Fig. 6. HSPICE simulated voltage waveforms to find the turn-on time of the proposed input ESD protection circuit under (a) the positive-to-VSS ESD-stress condition and (b) the negative-to-VDD ESD-stress condition.

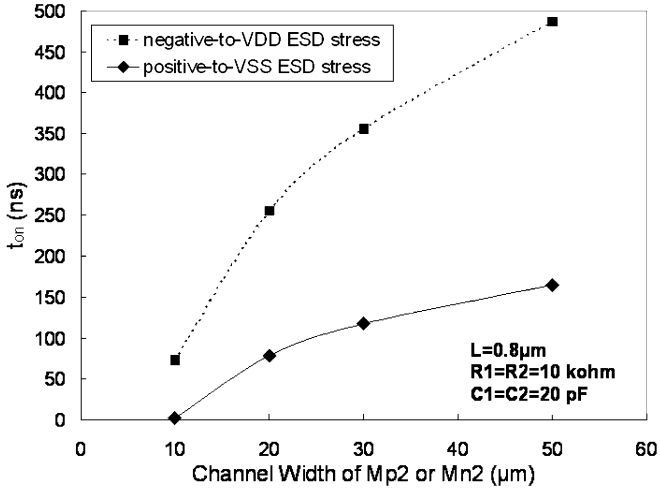


Fig. 7. Dependence between the turn-on time $(t_{\rm on})$ and the device dimension of $Mp2$ or $Mn2$ in the proposed input ESD protection circuit during positive-to-VSS or negative-to-VDD ESD-stress conditions.

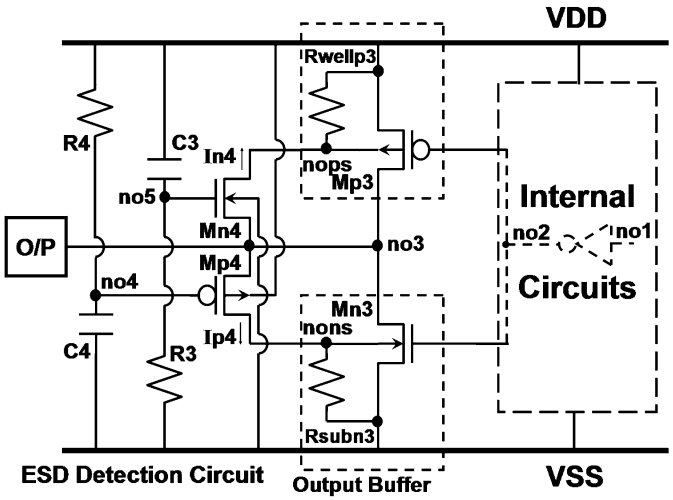


Fig. 8. Output ESD protection circuit with the proposed substrate-triggered design.

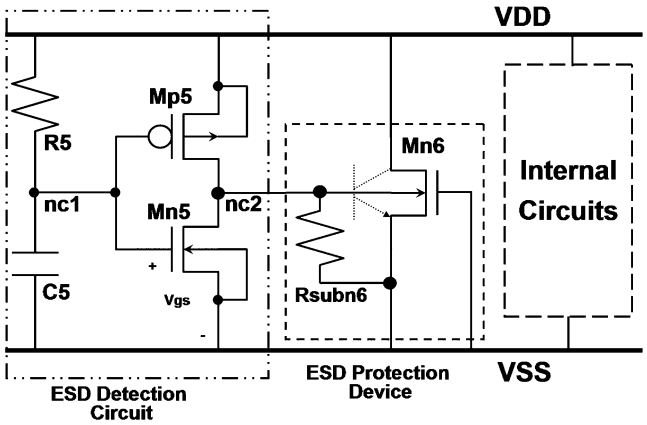


Fig. 9. Power-rail ESD clamp circuit with the proposed substrate-triggered design.

B. Output ESD Protection Circuit With Substrate-Triggered Design

The output ESD protection circuit with the proposed substrate-triggered design is shown in Fig. 8. The PMOS ($Mp3$) and NMOS ($Mn3$) of output buffer with larger device dimensions to drive external load also work as the ESD protection devices. The ESD detection circuits with resistors ($R3$ and $R4$), capacitors ($C3$ and $C4$), and NMOS/PMOS ($Mn4/Mp4$) are connected in Fig. 8 to detect ESD events. The gates of the output buffer are connected to the pre-driver buffer. The operation principles of the output ESD protection circuit during ESD-stress conditions are similar to those of the input ESD protection circuit described in the previous section. The ESD detection circuit is designed to detect the ESD events and generates a triggering current into the trigger node of substrate-triggered NMOS ($Mn3$) or PMOS ($Mp3$).

Because the $Mp3$ and $Mn3$ devices in the output buffer are triggered on through their bulk nodes, the ESD detection circuit does not connect to the gates of the output buffer. The gates of the output buffer can be fully controlled by its pre-driver circuit without any conflict to the ESD detection circuit. So, the proposed substrate-triggered design is more feasibly applied to the output buffer, as compared to the gate-driven design.

C. Power-Rail ESD Clamp Circuit With Substrate-Triggered Design

The power-rail ESD clamp circuit with substrate-triggered design is shown in Fig. 9. To efficiently clamp ESD voltage across VDD and VSS power lines before internal circuits are damaged, the ESD detection circuit ($R5$, $C5$, $Mn5$, and $Mp5$) is used to detect ESD events and to turn on the substrate-triggered NMOS ($Mn6$). The RC time constant in the power-rail ESD clamp circuit is designed about 0.1$\sim$1 μs to achieve the desired circuit operations [4].

The RC delay circuits, connected between the VDD and VSS power rails in the input ESD protection circuit of Fig. 5, in the output ESD protection circuit of Fig. 8, and in the power-rail ESD clamp circuit of Fig. 9, can be further merged together in the chip to save the total layout area. For example, the $R2$–$C2$ in Fig. 5 can be shared as $R4$–$C4$ in Fig. 8, and also shared as $R5$–$C5$ in Fig. 9. So, the I/O cells in a chip can shared with only one RC delay circuit ($R2$–$C2$) for triggering all ESD protection NMOSs, and shared with another RC delay circuit ($R1$–$C1$) for triggering all ESD protection PMOSs.

IV. Experimental Results

To compare with the substrate-triggered design, the traditional input/output ESD protection and power-rail ESD clamp circuits, as shown in Fig. 10, are also fabricated in the same testchip in a 0.18-μm salicided CMOS process. In Fig. 10(a), NMOS ($Mni1$), and PMOS ($Mpi1$) have a gate-coupled design to protect the input stage of internal circuits during ESD stress. In Fig. 10(b), PMOS ($Mpo3$) and NMOS ($Mno3$), of the output buffer with larger dimensions, are also used as ESD protection devices to sustain ESD stress. In Fig. 10(c), the ESD clamp circuit with a gate-driven design is placed between the VDD and VSS power rails [4]. The devices of $Mni1$, $Mno3$, and $Mnc2$ with different total channel widths are drawn with the traditional finger-type layout, as shown in Fig. 2(a).

A. ESD Level

The *ZapMaster* ESD tester, produced by Keytek Instrument Corp., is used to measure the HBM ESD level of the fabricated testchips. The failure criterion is generally defined at 1-μA leakage current under 1.1 times V_{DD} bias, when the ESD protection circuit is in the off state. The ESD levels of the fabricated input/output ESD protection circuits and power-rail ESD clamp circuits with the substrate-triggered or the traditional designs have been tested, and the results are compared in Figs. 11–13, respectively.

In Fig. 11, the positive HBM ESD pulses are zapping on the input pad of the input ESD protection circuit with VSS grounded under the positive-to-VSS HBM ESD test. The input ESD protection circuit with a substrate-triggered design has made an excellent improvement on its ESD level, as compared to the traditional design. The proposed input ESD protection circuit with substrate-triggered NMOS ($W/L = 300$ μm/0.3 μm) can sustain an ESD level of 3.3 kV. However, the input

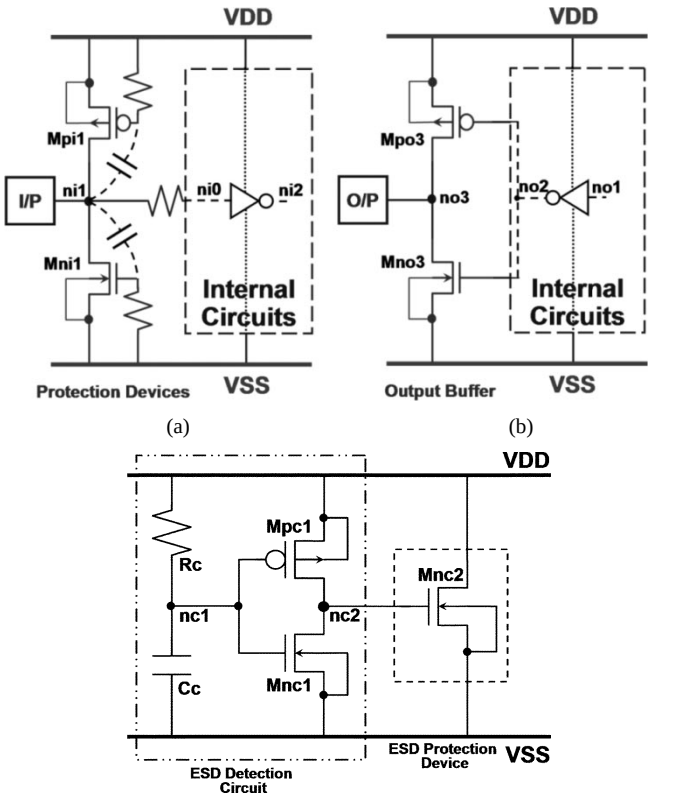


Fig. 10. Illustrations of the traditional (a) input ESD protection circuit, (b) output ESD protection circuit, and (c) power-rail ESD clamp circuit with gate-driven design.

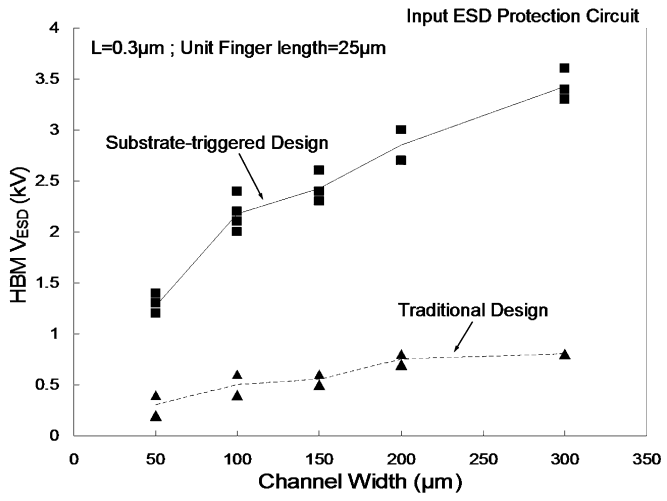


Fig. 11. Comparison of ESD robustness between the proposed substrate-triggered input ESD protection circuit and the traditional input ESD protection circuit.

ESD protection circuit with the same device dimension under a traditional design has an ESD level of only 0.8 kV.

In Fig. 12, the positive HBM ESD pulses are stressed on the output pad of the output buffer with VSS grounded under the positive-to-VSS HBM ESD test. The substrate-triggered design can also effectively improve ESD robustness of output buffer. The ESD level of output NMOS with $W/L = 300$ μm/0.3 μm

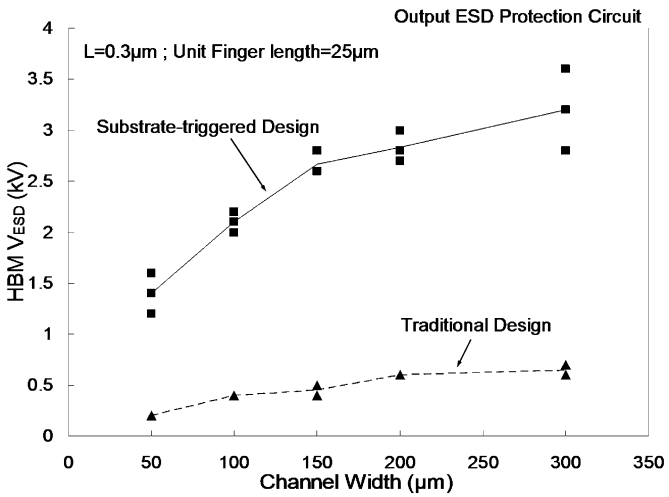


Fig. 12. Comparison of ESD robustness between the proposed substrate-triggered output ESD protection circuit and the traditional output ESD protection circuit.

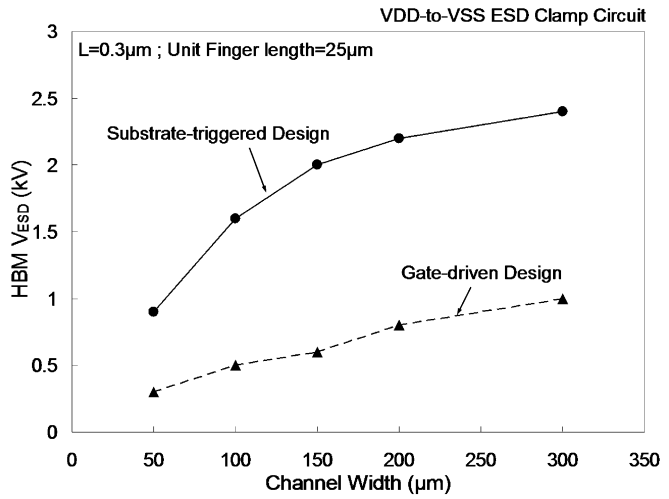


Fig. 13. Comparison of ESD robustness between the proposed substrate-triggered power-rail ESD clamp circuit and the gate-driven power-rail ESD clamp circuit.

can be improved from 0.65 kV with the traditional design to 3.2 kV with the substrate-triggered design.

In Fig. 13, the positive HBM ESD pulses are stressed on the VDD of the power-rail ESD clamp circuit with VSS grounded. ESD robustness of the ESD clamp circuit with substrate-triggered NMOS of $W/L = 300$ μm/0.3 μm is 2.5 kV, but that with the traditional gate-driven design under the same device dimension can sustain the ESD level of only 1 kV. These have verified the excellent effectiveness of the proposed substrate-triggered technique to improve ESD robustness in a 0.18-μm CMOS process.

B. Turn-On Verification

To verify the aforementioned ESD detection function in the proposed input ESD protection circuit, a voltage pulse generated from a pulse generator (*HP 8118*) is used to simulate the rising edge of a positive-to-VSS HBM ESD pulse. The gen-

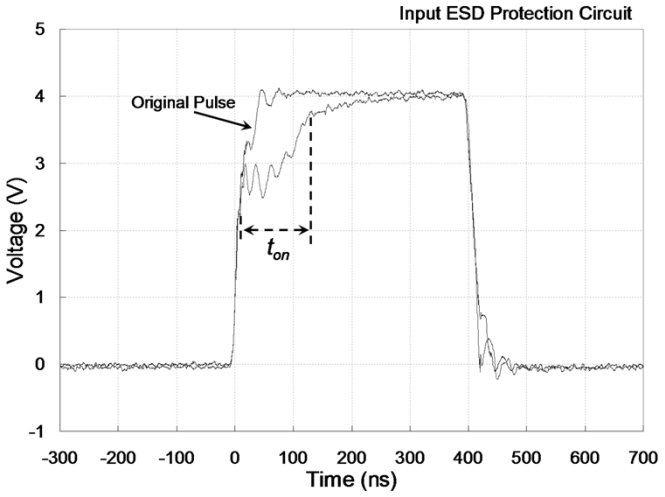


Fig. 14. Comparison between the original 0–4-V voltage waveform with a rise time of ∼10 ns generated from a pulse generator and the degraded voltage waveform on the input pad of the proposed input ESD protection circuit.

erated voltage pulse originally has a square-type voltage waveform with a rise time of about ∼10 ns and a pulse height of 4 V, as shown in Fig. 14. When the positive voltage pulse is applied to the input pad of the proposed input ESD protection circuit with VSS grounded, the sharp-rising edge of the ESD-like voltage pulse will trigger on ESD protection NMOS to provide a low-impedance path between the input pad and VSS power line. The voltage waveform on the input pad is therefore degraded by the turned-on ESD protection NMOS. The degraded voltage waveform on the input pad is also shown in Fig. 14. The voltage waveform is degraded at the rising edge because ESD protection NMOS is simultaneously turned on when the ESD-like voltage pulse is applied to the input pad. The voltage degradation is dependent on the turn-on resistance of the parasitic lateral BJT in ESD protection NMOS and the output resistance of the pulse generator. The maximum voltage drop from the applied 4-V voltage level in Fig. 14 is 1.5 V. The larger device dimension of the ESD protection device in the proposed input ESD protection circuit can lead to a larger voltage drop from the applied voltage level. When the node ni4 in Fig. 5 is charged up to turn off PMOS ($Mp2$) in the ESD detection circuit, ESD protection NMOS will be turned off, and the voltage waveform will be restored to the original voltage level. From Fig. 14, the substrate-triggered NMOS has a turn-on time $(t_{\rm on})$ of ∼120 ns under such a 4-V voltage pulse stress.

To verify ESD detection function in the power-rail ESD clamp circuit with substrate-triggered design, the same 4-V voltage pulse is applied to VDD power line to simulate the rising edge of a positive HBM ESD event. The measured voltage waveform is similar to that shown in Fig. 14, which also verifies the turn-on efficiency of the proposed power-rail ESD clamp circuit.

V. Conclusion

From the circuit analysis and experimental results, the substrate-triggered technique has been confirmed to continually improve ESD robustness of ESD protection devices without sudden degradation as that found in the traditional gate-driven design. With the substrate-triggered technique, the input, output, and power-rail ESD protection circuits have been successfully designed and verified in a 0.18-μm CMOS process to protect the internal circuits of CMOS IC. Because the output buffers are triggered on through their bulk nodes, the ESD detection circuit does not connect to the gates of the output buffer. The gates of the output buffer can be fully controlled by its pre-driver circuit without any conflict to the ESD detection circuit. So, the proposed substrate-triggered design is more feasibly applied to the output buffer, as compared to the gate-driven design. Without adding extra ESD implantation into the CMOS process, the ESD protection device with the proposed substrate-triggered design can sustain much higher ESD stress than that of the traditional gate-driven design. This substrate-triggered technique, designed and realized by using circuit and layout technique, will be one of the best and most cost-efficient ESD protection solutions to improve ESD robustness of IC products in the subquarter-micron CMOS technologies.

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