Substrate Bias Dependence of Breakdown Progression in Ultrathin Oxide pMOSFETs

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***Abstract*—Negative substrate bias-enhanced oxide breakdown (BD) progression in ultrathin oxide (1.4 nm) pMOS is observed. The enhanced progression is attributed to the increase of hole-stress current resulting from BD-induced, channel-carrier heating. The carrier temperature extracted from the spectral distribution of hot-carrier luminescence is around 1300 K. The substrate bias dependence of post-BD hole-tunneling current is confirmed from measurement and calculation. The observed phenomenon is particularly significant to ultrathin gate oxide reliability in floating substrate (SOI) and forward-biased substrate devices.**

***Index Terms*—Breakdown (BD) progression, carrier temperature, substrate bias, ultrathin oxide pMOS.**

I. Introduction

GATE-oxide breakdown (BD) has been considered as one of the most critical reliability issues for aggressive scaling of oxide thickness. In ultrathin oxide devices, oxide BD is evolved in a progressive way and the oxide leakage current increases slowly with stress time [1]–[3]. Previous study has shown that a small increase in gate leakage due to oxide BD is considered to be nondestructive for circuit operation [4]. The oxide failure time is thus determined by BD hardness involved in a progressive process, or in other words, by BD evolution rate.

A forward-substrate bias (V_b) is sometimes employed in certain analog and digital MOS circuits to achieve improved device characteristics [5]. In addition, the floating body configuration of partially depleted floating substrate (SOI) CMOS will result in a nonzero body voltage due to various body-charging mechanisms [6], [7]. Although the dependence of oxide BD on V_b has been widely explored [8], [9], a forward V_b effect on the evolution of oxide BD is rarely investigated.

In this work, we observe for the first time that oxide BD progression in a 1.4-nm oxide pMOS exhibits distinct V_b dependence. The devices were stressed at a high gate voltage ($V_g = -3.5$ V) until the onset of BD ($t_{\rm BD}$), and then the devices were subjected to a lower gate voltage stress ($V_g = -3.0$ V) with different substrate bias to study the evolution of oxide BD. The Weibull distribution of oxide failure time ($t_{\rm fail}$) for different stress V_b is shown in Fig. 1 by assuming that oxide failure is defined as ten times increase in gate current. Apparently, a forward V_b aggravates BD evolution, and the responsible mechanism will be discussed.

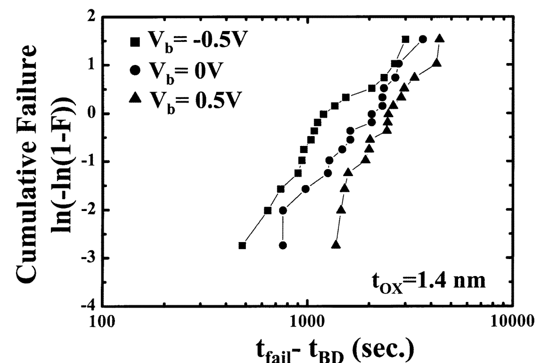

Fig. 1. Weibull plot of oxide failure time ($t_{\rm fail}$) for a 1.4-nm oxide pMOS. Stress V_g is -3 V and V_b is -0.5, 0, and 0.5 V. The $t_{\rm fail}$ is defined as an increase of gate current by ten times. The device area is 2×2 μm.

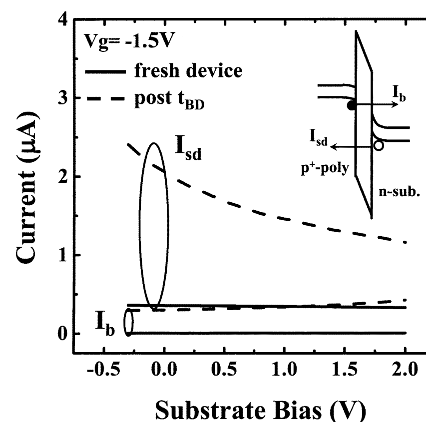

Fig. 2. Charge separation measurement result of electron current (I_b) and hole current ($I_{\rm sd}$) versus substrate bias. The inset shows the electron and hole current flows at a negative gate bias. In measurement, source, drain, and substrate are grounded, and the gate voltage is -1.5 V. The hole-tunneling current is measured at the source, and the drain and the electron current is measured at the substrate.

II. Mechanism for Enhanced BD Progression

To investigate the role of V_b in BD evolution, we analyze the polarity of stress-gate current first by using charge-separation measurement. The gate current in an ultrathin oxide (1.4 nm) pMOS is found to have comparable electron (I_b) and hole ($I_{\rm sd}$) components at a negative gate bias. Fig. 2 shows that the dominant component after $t_{\rm BD}$ is the hole current. Unlike I_b and $I_{\rm sd}$ in a fresh device, the post-$t_{\rm BD}$ hole current increases significantly with a negative V_b. By comparing the V_b dependence of

Manuscript received January 10, 2003. This work was supported by yhe Nationa Council of Taiwan, R.O.C., under Grant NSC 90-2215-E009-069 and from UMC, Taiwan (89C189). The review of this letter was arranged by Editor B. Yu.

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Digital Object Identifier 10.1109/LED.2003.810890

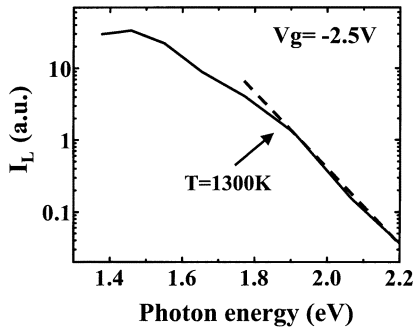


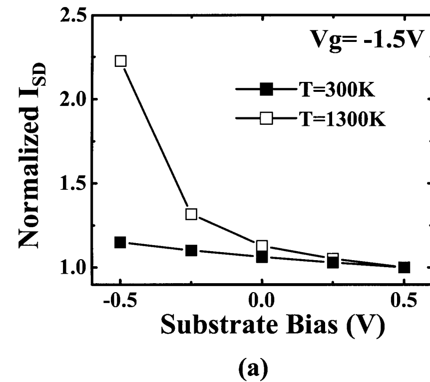
Fig. 3. Measured spectral distribution of light emission (I_L) after oxide breakdown. The dashed line represents the Boltzmann tail with a carrier temperature of 1300 K. $V_g = -2.5$ V.

post-$t_{\rm BD}$ I_b and $I_{\rm sd}$, we exclude the possibility that the V_b dependence of the post-$t_{\rm BD}$ hole current is caused by the change of effective gate-to-channel bias in the BD spot [2] resulting from V_b modulated channel resistance. Otherwise, the post-$t_{\rm BD}$ electron tunneling current (I_b) should exhibit the same V_b dependence. Furthermore, substrate impact ionization [9] and negative bias temperature instability (NBTI) effects are also excluded, since the trend of the V_b dependence is opposite.

Fig. 3 shows the measured spectral distribution of hot carrier light emission after $t_{\rm BD}$. The measurement is performed with a Hamamatsu C3230 single photon counting system. The photon number at different wavelengths is counted individually. The measurement result is then corrected for the wavelength dependence of the filter transmittance. The pre-$t_{\rm BD}$ light emission is negligible and is not shown here. The extracted carrier temperature from the high-energy tail of the spectrum is around 1300 K. There are two theories to explain the rise of carrier temperature after BD [10], [11]. First, based on the model proposed in [10], the gate voltage will penetrate into the substrate after BD and cause lateral field heating of channel carriers. This mechanism is unlikely here because the post-$t_{\rm BD}$ I_b does not exhibit V_b dependence, as pointed out earlier. The second explanation is that high-dissipated energy, released by valence electrons (I_b) from the gate through the BD path, will locally produce a temperature rise of holes in the channel [11].

III. Simulation of Hole-Tunneling Current

To show that the rise of hole temperature may account for the V_b dependence of post-$t_{\rm BD}$ $I_{\rm sd}$, we calculate the hole-tunneling current from $T = 300$ to 1300 K. In our calculation, we solved the coupled Poisson and Schrodinger equation to obtain the valence band diagram. A single band effective mass approximation is used. The hole direct-tunneling current can be calculated through the Tsu Esaki equation [12]. See (1), shown at the bottom of the page, where m^* is the hole effective mass in Si, E_f ($E_{f'}$) denotes the Fermi energy in the channel (p^+-poly), E_n stands for the nth subband energy, and D_n is the hole tunneling probability. Other variables have their usual definitions.



(a)

cond. / sub-band	channel hole dist. (%)			
	300K		1300K	
	V_b=-0.3	V_b=2	V_b=-0.3	V_b=2
1st	98	99.9	62.7	81.3
2nd	1.9	0.1	13.8	13.1
3rd	0.1	0	6	3.5

(b)

Fig. 4. (a) Simulated substrate bias effect on hole-tunneling current for different hole temperatures. The hole current is normalized to its value at $V_b = 0.5$ V. (b) Distribution of channel holes in the lowest three subbands. The gate bias in simulation is -1.5 V. The parameters used in simulation is $m^*(\mathrm{Si}) = 0.67m_o$, $m^*(\mathrm{SiO_2}) = 0.55m_o$, ϕ_h(hole barrier height at SiO_2 interface) $= 4.25$ eV, $t_{\rm ox} = 1.4$ nm, and N_B(substrate doping) $= 1 \times 10^{18}$ cm^{-3}. The density of states mass $m^*(\mathrm{Si})$ is treated as a fitting parameter.

It should be emphasized that it is not our intention here to calculate detailed charge transport in the BD path since the effective oxide thickness after $t_{\rm BD}$ is not known. Instead, our purpose is to investigate the influence of hole temperature on hole distribution in subbands and corresponding V_b effect on hole-tunneling current. Therefore, the simple Wentzel–Kramers–Brillouin (WKB) formula for direct tunneling is employed. Our result in Fig. 4(a) clearly shows that the hole-tunneling current exhibits larger V_b dependence at a higher temperature. The simulation can well interpret the measured V_b dependence of post-$t_{\rm BD}$ $I_{\rm sd}$ by simply using an elevated hole temperature. To further explain the temperature effect on the V_b dependence, the distribution of channel holes in the lowest three subbands is given in Fig. 4(b). Before $t_{\rm BD}$, hole temperature is 300 K. Most of inversion holes reside in the first subband, regardless of V_b, for example, 99.9% at $V_b = 2$ V versus 98% at $V_b = -0.3$ V. In other words, the V_b effect on hole-tunneling current is small at 300 K. After $t_{\rm BD}$, the hole temperature is increased. For $V_b = 2$ V, since the substrate confinement field is large, a large part of holes (81%) still stay in the first subband, although the hole temperature is rather high (1300 K), but for $V_b = -0.3$ V, the confinement substrate field is small, and a large portion of holes are thermally excited to higher sub-bands, where the oxide tunneling probability is large.

$$I_{\rm sd} = qm^* \left(\frac{1}{2\pi^2\hbar^3}\right) k_B T \sum_n D_n \left\{ \ln\left(1 + \exp\left(\frac{(E_n - E_f)}{(k_B T)}\right)\right) - \ln\left(1 + \exp\left(\frac{(E_n - E_{f'})}{(k_B T)}\right)\right) \right\} \tag{1}$$

A larger hole-tunneling current is obtained. Thus, the substrate bias effect on hole-tunneling current becomes more significant at a higher hole temperature.

IV. Conclusion

BD evolution in ultrathin oxide pMOS is aggravated by a forward-substrate bias. Numerical analysis shows that the enhanced BD evolution can be explained by a rise of substrate hole temperature and thus increased hole stress current. The accelerated BD evolution has large impact on circuit lifetime in forward-biased substrate or SOI devices.

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