A Third-Order Continuous-Time Sigma-Delta Modulator for Bluetooth

Wen-Lin Yang, Wen-Hung Hsieh and Chung-Chih Hung
Department of Communication Engineering
National Chiao Tung University
Hsinchu, Taiwan

***Abstract*—This paper presents the design of a third-order continuous-time (CT) single-bit active-RC sigma-delta (ΣΔ) modulator for Bluetooth application. Through the use of the architecture, cascade of resonators with distributed feedback (CRFB), the signal bandwidth can be improved without increasing the order of the modulator. All integrators are implemented by active-RC type to have better linearity. Furthermore, in order to reduce the effect of the clock jitter, the feedback digital-to-analog converter (DAC) shape is realized by non-return-to-zero (NRZ). The modulator is designed in a standard digital 0.18μm CMOS process with a chip area of 1.32×1.23 mm^2. The measurement results show that the modulator achieves 56.8dB SNDR and 60dB dynamic range over 1MHz signal bandwidth, consuming 22.2mW at 1.8V supply.**

I. Introduction

Sigma-delta analog-to-digital converters (ADCs) are traditionally used in instrumentation, voice, and audio applications that require low signal bandwidth and high resolution. In recent years, there has been a growing trend to move ADC towards the system front-end. Due to the scaling in VLSI technology, high performance digital systems can be realized. The ADC has to provide a higher dynamic range for the interface between analog and digital data. Therefore, sigma-delta ADCs which can achieve high resolution with wide input bandwidth for wireless and wireline communication systems becomes more and more important [1] [2].

In ΣΔ ADC, the use of CT loop filter provides several advantages over discrete-time (DT) implementations. Without critical slewing and settling issues, as in switched-capacitor circuits, CT integrators are often promised to achieve better power-performance efficiency [3]. Moreover, CT integrators are praised for better noise immunity due to their inherent anti-aliasing filtering which are especially advantageous in RF receivers [4].

This paper is organized as follows. Section II describes the architecture of the modulator. In section III, the system analysis and circuit implementations are presented. Section IV shows the measurement results of the third-order CT ΣΔ modulator and section V gives a conclusion.

II. Architecture

The loop filter of the third-order CT modulator uses CRFB architecture as shown in Fig. 1. The transfer function can be derived by

$$H(s)=\frac{a_3\cdot c_3\cdot s^2+(c_2\cdot c_3\cdot a_2)s+c_1\cdot c_2\cdot c_3\cdot a_1}{s^3+g\cdot c_2\cdot c_3} \quad (1)$$

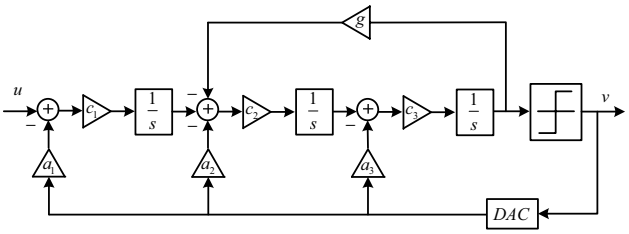
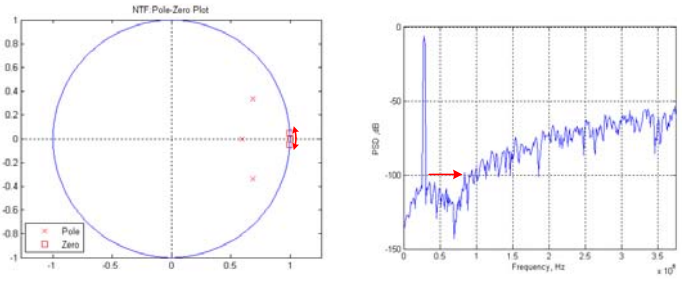


Fig. 1 CRFB architecture



(a) (b)

Fig. 2 (a) Pole-zero plot of CRFB and (b) PSD of CRFB

The advantage of the architecture enables to realize noise transfer function (NTF) zeros as two conjugate complex pairs on the unit circle to obtain wider bandwidth. For example, the pole-zero plot of the third-order architecture is illustrated in Fig. 2 (a). In Fig. 2 (a), we can observe that there are one zero at DC and two conjugate zeros on the unit circle as the described advantage. The power spectrum density (PSD) is shown in Fig. 2 (b). It is expected that even greater benefits can be obtained by optimizing the location of the zeros of higher-order NTF [5].

III. System Analysis and Circuit Implementations

A. System Analysis

The first step of design ΣΔ modulator is to determine the NTF. By using the ΣΔ toolbox [5], the NTF can be easily derived according to the specifications. In this work, we design a third-order modulator, where the oversampling ratio (OSR) is equal to 50 and the maximum out-of-band gain of the NTF is 1.7. In Fig. 3, the maximum out-of-band gain of the NTF versus the peak SNR in system level is simulated. Due to the stability issue, we can find that the maximum out-of-band gain of the NTF is limited.

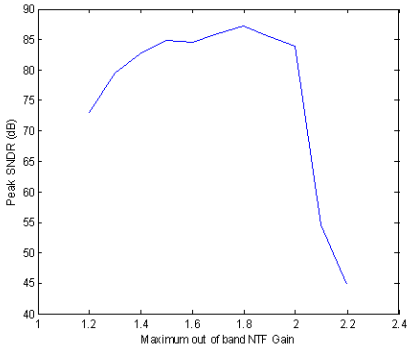


Fig. 3 Maximum out-of-band gain of the NTF versus the peak SNR

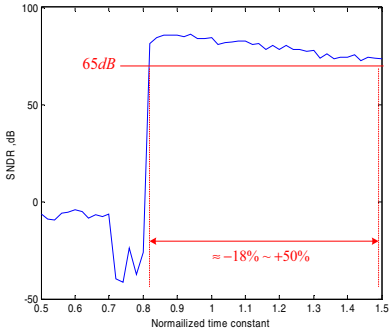


Fig. 4 Simulated SNDR for -6dBFS input under the variation of the time constant

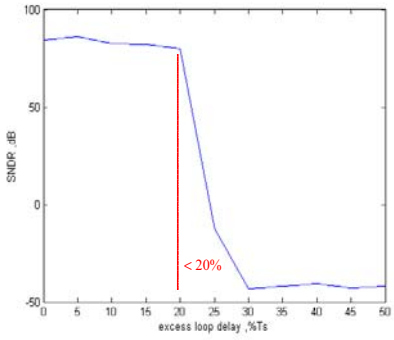


Fig. 5 Simulated SNDR for -6dBFS input under the effect of the excess loop delay

1) RC Variation: One of the circuit imperfections in CT ΣΔ modulators is the variation of the RC time constant. In modern standard digital process, the actual value of resistors and capacitors can vary as large as ±20%. For CT modulators, ±20% variation is more than enough to derive the modulator into unstable operation. Therefore, by analyzing the behavior model, the SNDR performance for -6dBFS input under the variation of the time constant is shown in Fig. 4. We can find that a time constant variation of about +50% can also make the modulator stable and achieve the 65dB SNDR performance. However, a negative time constant variation results in the unstable modulator instead. Consequently, an additional tuning circuit is needed to vary the time constant of the CT modulator and ensure that the modulator is in stable operation. Although the new normalized time constant 1.1 or 1.2 has wider range, the original time constant is chosen to achieve higher performance.

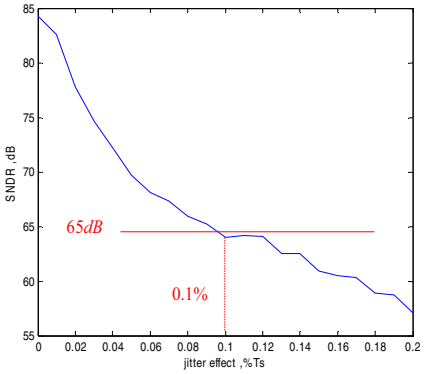


Fig. 6 Simulated SNDR for -6dBFS input under the effect of the clock jitter

2) Excess Loop Delay: The time including quantizer delay and the response time of the feedback DAC is called excess loop delay. The excess loop delay can cause the deviation of the transfer function to degrade the performance or even seriously make the modulator unstable. By the behavior model analysis, the allowable excess loop delay can be estimated and the limitation can be achieved in circuit level design. Fig. 5 shows the simulated SNDR performance for -6dBFS input under the effect of the excess loop delay. We can find that when the excess loop delay is larger than 25% T_s, the modulator will be unstable. Therefore, we have 20% T_s delay tolerance.

3) Clock Jitter: The clock jitter arises from both the quantizer and the feedback DACs. Due to the same order noise shaping, the sampling error at the quantizer only adds little noise to the modulator output. Nevertheless, the clock jitter in the feedback DACs generates unshaped noise. The noise can degrade the modulator performance sorely. Thereby, by the behavior model analysis, we can estimate the performance degradation generated by clock jitter noise. Fig. 6 shows the simulated SNDR for -6dBFS input under the effect of the clock jitter. If the 65dB SNDR performance wants to be achieved, the effect of the clock jitter should be smaller than 0.1% T_s. This can be accomplished by an additional preamplifier in the quantizer to improve speed.

B. Circuit Implementations

Fig. 7 shows the simplified block diagram of the CT modulator. All stage integrators are implemented by the typical type, active-RC. Because of the closed-loop operation, the active-RC integrator has better linearity than the g_m-C type. The single-bit quantizer is composed of the preamplifier, the regenerative latch and the SR latch which realizes the NRZ shape.

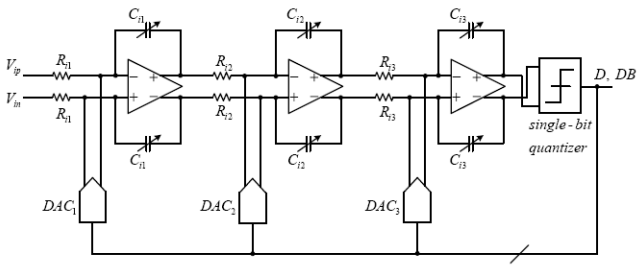


Fig. 7 Simplified block diagram of the CT third-order modulator

1) Amplifier: Due to the Bluetooth application for the design, where the sampling frequency is 100MHz and the bandwidth is 1MHz, the opamp uses a telescopic topology. Compared with the two-stage and folded cascode opamps, telescopic opamps achieve the highest speed with the lowest power consumption and generate low noise. In order to reduce the in-band noise, gain boosting technique is applied to the differential cascade stage as shown in Fig. 8. The objective is to maximize the output impedance to attain a high voltage gain.

2) Integrator: Fig. 9 shows the active-RC integrator with the current steering DAC. The DAC level (-1, +1) is realized by the feedback digital codes, D and DB. The difference of the input signal and the DAC level is stored into C_i and then transferred into the next stage integrator.

3) Comparator: The single-bit quantizer includes preamplifiers and a low-offset regenerative latch as shown in Fig. 10. In Fig. 10 (b), when V_{CK} goes to high, since the M_7 and M_8 are in saturation region so that the comparator has low-offset voltage. When V_{CK} goes to low, there is no power dissipation and the outputs are reset to V_{DD}. Due to the property, the SR latch maintains previous outputs to form the NRZ shape.

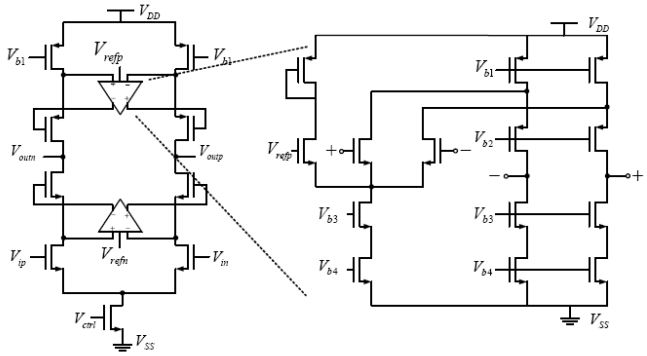


Fig. 8 Telescopic opamp with gain boosting of the first stage

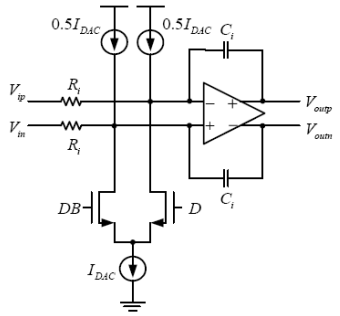


Fig. 9 Active-RC integrator with current steering DAC

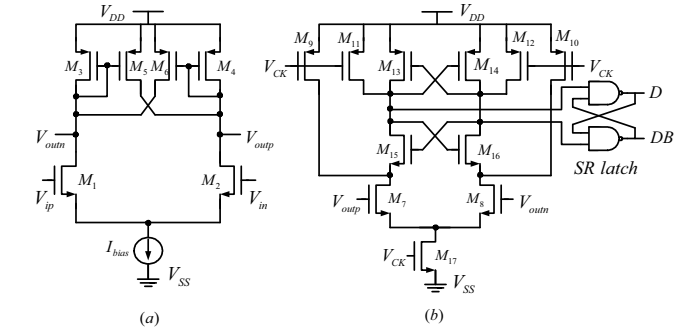


Fig. 10 (a) A cross-coupled preamplifier and (b) Low-offset regenerative latch

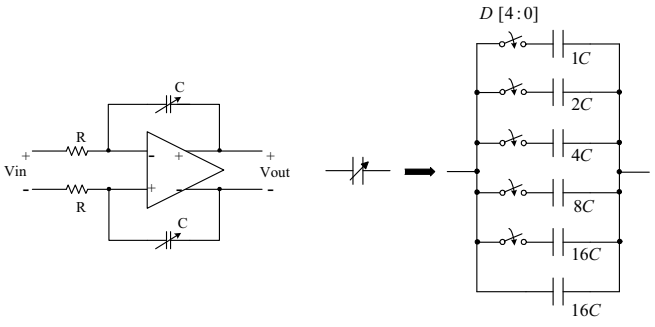


Fig. 11 Tuning circuit

4) Tuning Circuit: From behavior model simulation, only about -18% time constant variation is allowed to maintain 65dB SNDR performance for Bluetooth application. To ensure that the modulator is in stable operation, the tuning circuit shown in Fig. 11 must be used [6]. In Fig. 11, there are an always-in-use capacitor which is 16C and five in-use capacitors which are 1C, 2C, 4C, 8C and 16C. The normal value of the capacitances is 32C. Through the use of the digital control signals, the minimum and maximum available capacitances are 16C and 47C, respectively. Thereby, the minimum tuning range is from -50% (16C/32C) to +46.875% (47C/32C) and the tuning resolution is 3.125% (C/32C), where C is the tuning step.

IV. Measurement Results

Fig. 12 shows the chip microphotograph. The continuous-time single-bit active-RC sigma-delta modulator for Bluetooth application has been fabricated by TSMC 0.18μm CMOS mixed-signal process. The output data of the modulator are saved by the logic analyzer. Using MATLAB to do fast Fourier transform (FFT) with 65536 points, the power spectrum density can be obtained as shown in Fig. 13. The input sine wave is 0.798MHz and the sampling frequency is 100MHz. The signal bandwidth is 1MHz and the oversampling ratio is equal to 50. The SNDR is about 56.8dB for -5dBFS input and the ENOB is 9.14bits. The SFDR is about 73dB. Fig. 14 shows the dynamic range plot which is the SNDR versus the normalized input level. The measured power consumption is 22.2mW at 1.8V supply voltage. The performance of this CT modulator is summarized in Table I. Table 2 lists the comparison between previously reported DT SDM and the CT modulator. The FOM is described as follows

$$FOM = \frac{Power}{2 \cdot BW \cdot 2^{((SNDR-1.76)/6.02)}} \quad (2)$$

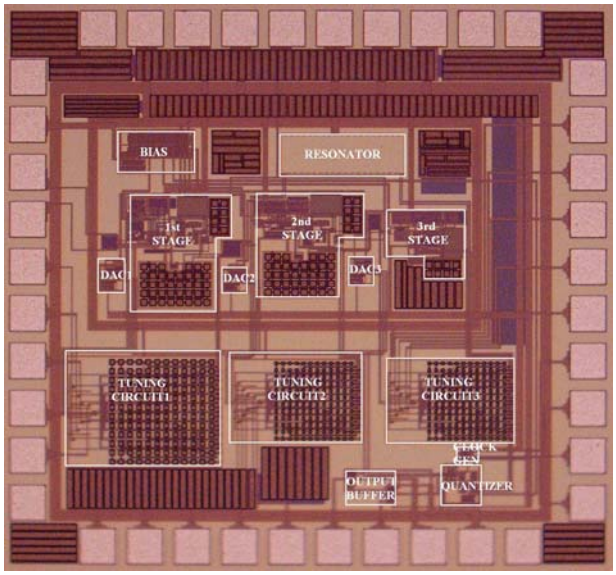


Fig. 12 Die photo

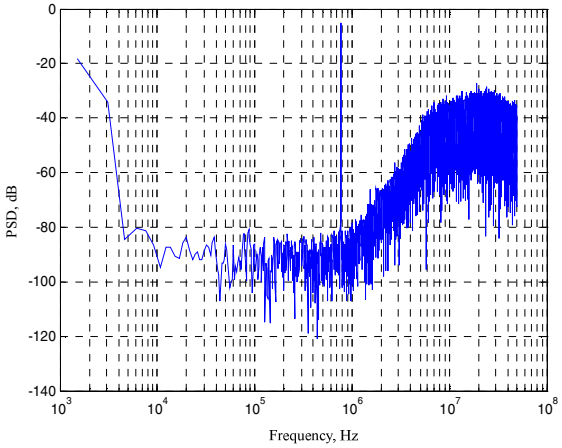


Fig. 13 PSD with 65536 points FFT

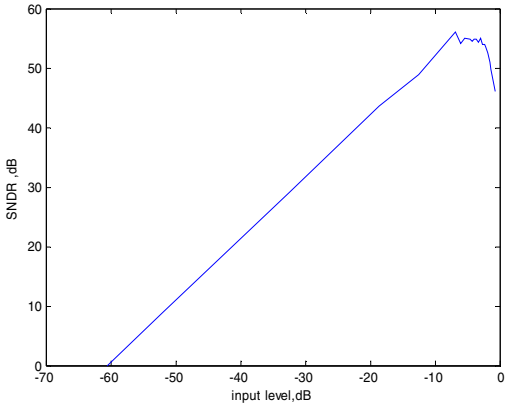


Fig. 14 Dynamic range plot

TABLE I
PERFORMANCE SUMMARY

Parameters	Measurement Results
Technology	TSMC 0.18μm process
Power Supply	1.8V
Sampling Frequency	100MHz
Signal Bandwidth	1MHz
SNDR	56.8dB
ENOB	9.14bits
Dynamic Range	60dB
Area	1.32mm x 1.23mm
Power Consumption	22.2mW

TABLE II
COMPARISON BETWEEN DT SDM AND THIS WORK

Reference	[7]	[7]	This work
Architecture	2-2 MASH	2-2-2 MASH	3rd-order
SNDR (dB)	72	79	56.8
BW (MHz)	1.1	1.1	1
F_s (MHz)	52.5	52.5	100
Process (μm)	0.35	0.35	0.18
Power (mW)	187	248	22.2
FOM (pJ/conv.)	26.26	15.48	19.6

V. CONCLUSIONS

A continuous-time third-order single-bit sigma-delta modulator for Bluetooth application is designed in TSMC 0.18μm digital CMOS process. The architecture of the modulator utilizes CRFB structure to improve the signal bandwidth. In order to reduce the effect of the clock jitter, the feedback DAC shape is realized by NRZ. The third-order CT single-bit modulator achieves 56.8dB SNDR and 60dB dynamic range in 22.2mW power consumption.

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