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# Effect of Zr/Ti Ratios on Characterization of $Pb(Zr_xTi_{1-x})O_3$ Thin Films on $Al_2O_3$ Buffered Si for One-Transistor Memory Applications

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$Pb(Zr_xTi_{1-x})O_3$ (PZT) thin films have been prepared on $Al_2O_3$/Si and $PbTiO_3$/$Al_2O_3$/Si substrates, respectively. On $Al_2O_3$/Si substrates, Ti-rich PZT thin films had lower perovskite transformation temperatures than those of Zr-rich PZT films. Therefore, $PbTiO_3$ was used as the seeding layer on $Al_2O_3$/Si to form a $PbTiO_3$/$Al_2O_3$/Si substrate. The threshold voltage shift of a PZT(53/47)/$PbTiO_3$/$Al_2O_3$/Si capacitor reaches 9 V with ±10 V writing voltages, which is much larger than the 2 V of the PZT(0/100)/$PbTiO_3$/$Al_2O_3$/Si capacitor. Different memory mechanisms in the capacitance-voltage characteristics of capacitors were further examined and discussed in this paper.
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Recently, one-transistor memory has attracted much attention because of the excellent performance.[1-4] Unfortunately, little progress has been achieved in one-transistor memory because it is difficult to integrate different materials as stack gate dielectrics and to fabricate a metal/ferroelectric/insulator/Si (MFIS) capacitor structure.[5,6] Although the effects of different substrates and annealing temperatures have been studied,[7,8] the ferroelectric material in each research has the same composition, and the related influences were not discussed as in the study in a metal/ferroelectric/metal capacitor.[9] Thus, it is necessary to do some systematic research on the effects of ferroelectric material compositions on the memory properties in the MFIS capacitor.

The solid solution $Pb(Zr_xTi_{1-x})O_3$ (PZT) system has a complex phase diagram containing materials exhibiting unique properties such as piezoelectricity, pyroelectricity, and ferroelectricity.[10] All these properties are strongly related to the different structures and compositions in the PZT solid solution. For example, it is well known that the coupling factor and permittivity of PZT located at the morphotropic phase boundary (MPB) show maximum values.[11] Among its many superior properties, the high dielectric constant and remnant polarization of PZT have made it a promising material for memory applications.[12,13] It is necessary to study the effect of compositions on the memory properties of an MFIS capacitor with PZT as the ferroelectric layer. In this paper, we have prepared PZT thin films on $Al_2O_3$/Si substrates as the MFIS capacitor and investigated the characteristics related to four Zr/Ti ratios (0/100, 30/70, 53/47, and 60/40) to find the relationship between the electrical properties of an MFIS capacitor and the phase and microstructure of PZT films with different compositions.

## Experimental

*PZT stock solution synthesis and thin-film deposition.*—PZT ferroelectric thin films were deposited by the chemical solution deposition method using multiple spin coating. The advantage of chemical solution deposition was the accuracy of composition control. For chemical solution synthesis, lead acetate trihydrate, zirconium n-propoxide, and titanium isopropoxide were used as precursors and dissolved in the solvents composed of acetic acid and methanol in sequence.[7] An excess lead precursor was added to compensate the lead loss during crystallization, and four Zr/Ti ratios of the chemical solution were varied from titanium-rich (Ti-rich) compositions (Zr/Ti = 0/100 and 30/70) to zirconium-rich (Zr-rich) compositions (Zr/Ti = 53/47 and 60/40). After each coating, the

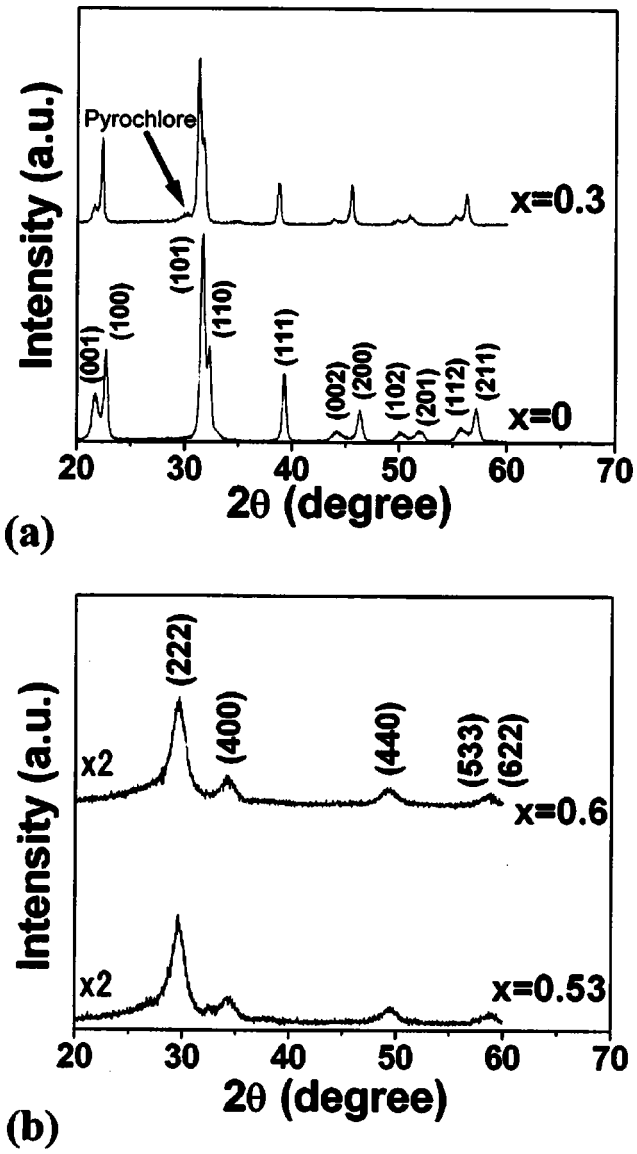


**Figure 1.** XRD patterns of $Pb(Zr_xTi_{1-x})O_3$ thin films with (a) $x = 0$ and 0.3 and (b) $x = 0.53$ and $x = 0.6$ on $Al_2O_3$/Si.

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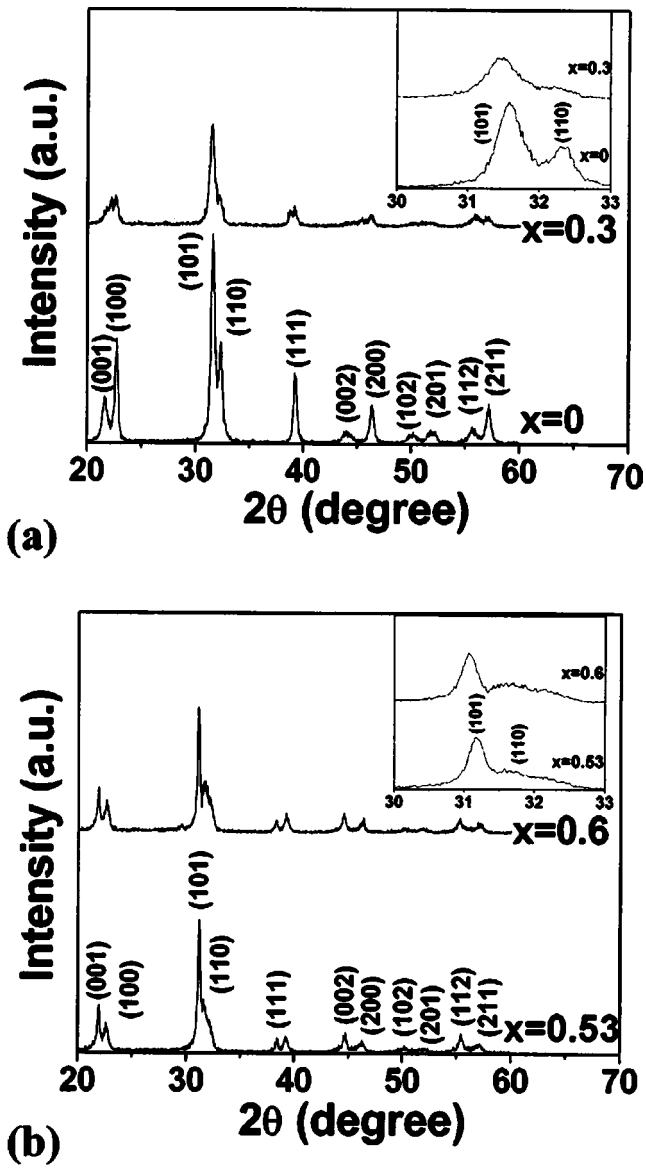


**Figure 2.** XRD patterns of $Pb(Zr_xTi_{1-x})O_3$ thin films with (a) $x = 0$ and 0.3 and (b) $x = 0.53$ and $x = 0.6$ on $PbTiO_3/Al_2O_3/Si$.

wet films were pyrolyzed for several minutes, and the multilayer films, 650 nm thick, were annealed at 650°C for 1 h.

*Preparation of $Al_2O_3/Si$ and $PbTiO_3(PTO)/Al_2O_3/Si$ substrates.*—To fabricate the insulator buffered layer, a 10 nm thick $Al_2O_3$ gate dielectric was formed on p-type (100) Si wafers following our previously reported procedure.[14,15] For preparing the seeding layer, 80 nm thick lead titanate (PTO) film was deposited on $Al_2O_3/Si$ and then annealed at 550°C so that the $PTO/Al_2O_3/Si$ substrates could be obtained.

*Film and capacitor characterization.*—We have used X-ray diffraction (XRD) to determine the phase and the crystallinity of PZT. The surface morphology and the thickness of PZT were observed by scanning electron microscopy (SEM). For electrical measurement, Au was used as the upper electrode with an area of $5 \times 10^{-4}$ $cm^2$, and the Al bottom electrode was deposited at the back side. Capacitance-voltage (C-V) and current density-voltage (J-V) characteristics were measured to check the electrical properties of PZT capacitors.

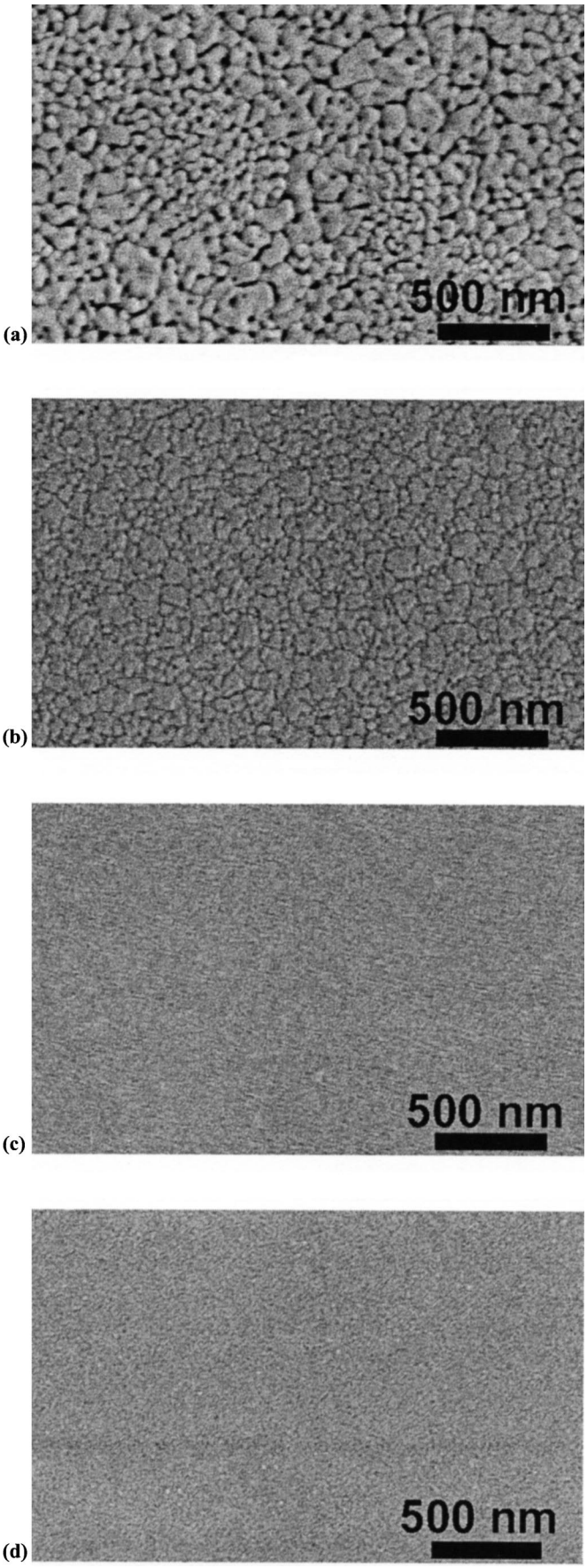


**Figure 3.** SEM images of $Pb(Zr_xTi_{1-x})O_3$ thin films with (a) $x = 0$, (b) $x = 0.3$, (c) $x = 0.53$, and (d) $x = 0.6$ on $PbTiO_3/Al_2O_3/Si$.

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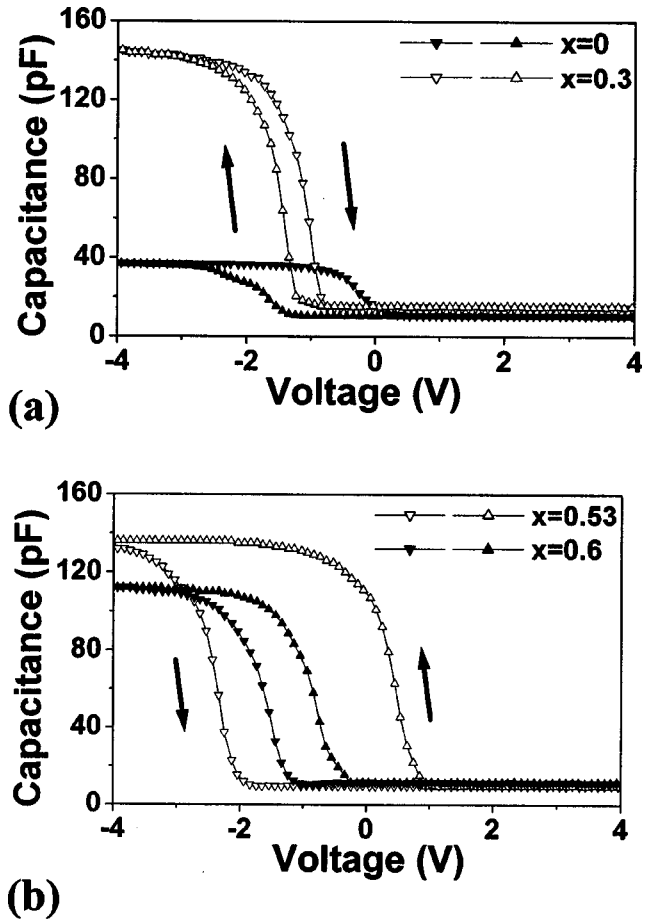


**Figure 4.** C-V characteristics of $Pb(Zr_xTi_{1-x})O_3/PbTiO_3/Al_2O_3/Si$ capacitors with (a) $x = 0$ and 0.3 and (b) $x = 0.53$ and 0.6 under ±5 V sweep voltage.

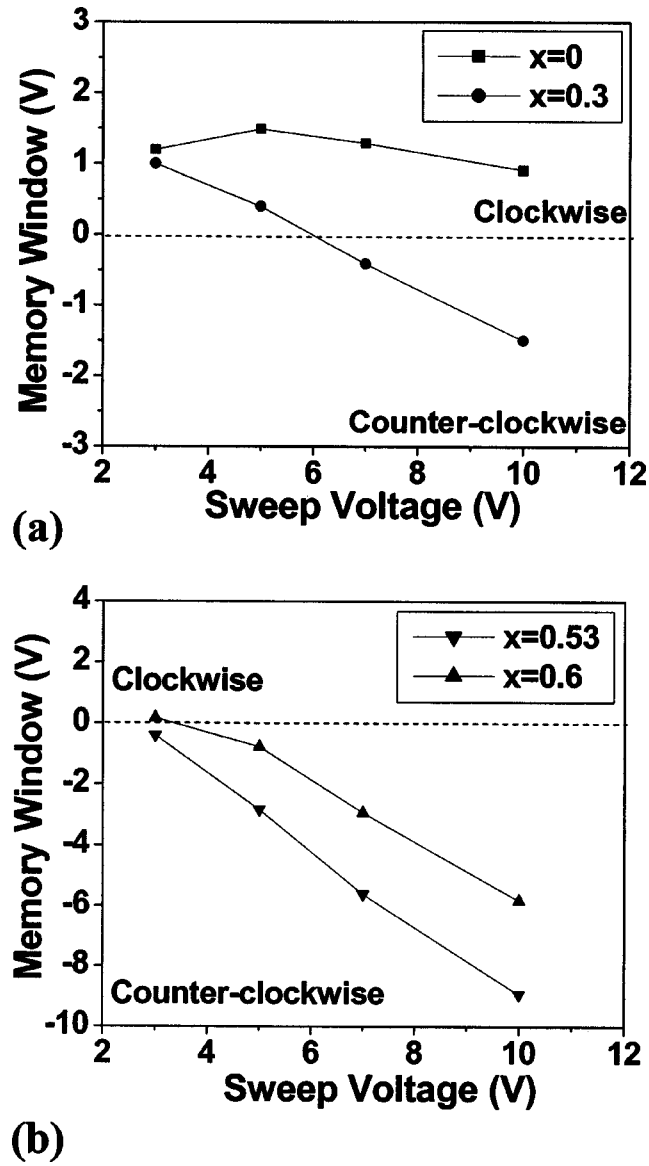


**Figure 5.** Memory window of $Pb(Zr_xTi_{1-x})O_3/PbTiO_3/Al_2O_3/Si$ capacitors with (a) $x = 0$ and 0.3 and (b) $x = 0.53$ and 0.6.

## Results and Discussion

Figures 1a and b show the XRD patterns of $Pb(Zr_xTi_{1-x})O_3$ deposited on $Al_2O_3$(10 nm)/Si, with $x = 0$-0.3 and 0.5-0.6, respectively. As shown in Fig. 1a, the major phase of Ti-rich PZT films is a perovskite phase, although a small and broad peak at diffraction angle $2\theta \sim 29.5°$ belonging to a pyrochlore phase is observed for the PZT (30/70). In contrast, the XRD patterns in Fig. 1b show that Zr-rich PZT films have a nonferroelectric pyrochlore phase rather than a perovskite phase. Therefore, it is suggested that PZT films with higher Zr/Ti ratios have higher perovskite transformation temperatures. Although this tendency is similar to that published in the literature,[16] the transformation temperatures of PZT on $Al_2O_3/Si$ substrates are obviously higher than those on single-crystal sapphire substrates.[16] This phenomenon may occur because the nucleation of perovskite PZT would be easier on crystalline substrates than on amorphous substrates.[17]

To reduce the perovskite transformation temperature of PZT, an additional PTO seeding layer was deposited on $Al_2O_3/Si$ substrates prior to the PZT films. Figure 2 shows the XRD patterns of PZT thin films deposited on $PTO/Al_2O_3/Si$ substrates with a seeding layer. In Fig. 2b, clearly, the formation of the pyrochlore phase is inhibited. Therefore, the PTO seeding layer is proved able to lower the transformation temperatures, which is similar to the result on crystalline substrates.[16,18] However, the intensity and full width at half-maximum (fwhm) of the major XRD peak position of Zr-rich PZT ($x$ 0.53 and 0.60) at 31.5° are lower and larger than that on Pt substrates, respectively.[8] These results imply that the microstructure of Zr-rich PZT films may be different from that on Pt substrates.

We have further used SEM to observe the microstructure of PZT thin films on $PTO/Al_2O_3/Si$ substrates. Figure 3a-d display the surface morphology of $Pb(Zr_xTi_{1-x})O_3$ films on $PTO/Al_2O_3/Si$ substrates, with $x = 0$, 0.3, 0.53, and 0.60, respectively. The microstructures for Ti-rich PZT show a large grain size, greater than 50 nm. In contrast, the microstructures for Zr-rich PZT exhibit a very small grain size, much less than 50 nm. These results are consistent with the weak XRD intensity and large fwhm shown in Fig. 1. These SEM images indicate that inserting the additional PT seeding layer could greatly suppress the nucleation of the pyrochlore phase, but a higher process temperature is still required for Zr-rich PZT with a perovskite phase to improve the crystallinity.

We have studied the memory property of PZT on $PTO/Al_2O_3/Si$ substrates using C-V measurements at 1 MHz. Figure 4a, b show the C-V characteristics of $PZT/PTO/Al_2O_3/Si$ capacitors. Under the same ±5 V sweep voltages, the Ti-rich PZT capacitors ($x = 0$ and 0.3) show a clockwise hysteresis loop, but the Zr-rich PZT capacitors show a counterclockwise loop. It is believed that the clockwise hysteresis loop is due to the ferroelectricity, while the counterclockwise loop is the result of a charge trapping effect.[4] Although both

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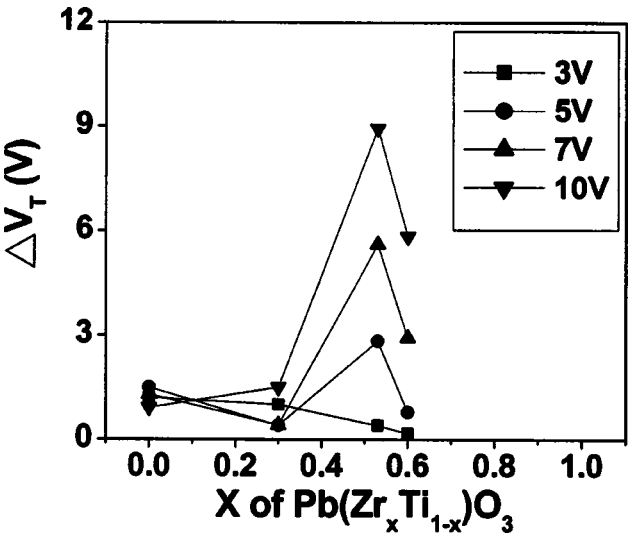


**Figure 6.** Threshold voltage shift of $Pb(Zr_xTi_{1-x})O_3/PbTiO_3/Al_2O_3/Si$ capacitors under different sweep voltages.

effects can be used for memory devices, the observed ferroelectric hysteresis loop may be due to a better ferroelectric material quality than that in the charge trapping case. These results are again consistent with the XRD and SEM results shown previously. However, the strong dependence of ferroelectric property on composition seems to be independent of the $Al_2O_3$ dielectric process, suggesting the excellent quality of the $Al_2O_3$ gate dielectric[14,15] as compared with low temperature deposited silicon nitride.

We have also measured the memory window of $PZT/PTO/Al_2O_3/Si$ capacitors at different program/erase voltages. Figure 5a, b summarize the measured threshold voltage shift ($\Delta V_T$) for Ti-rich and Zr-rich $PZT/PTO/Al_2O_3/Si$ capacitors, respectively. A positive threshold voltage shift is attributed to the ferroelectric effect, while a negative threshold shift is due to the charge trapping effect. Note that the threshold voltage shift of Ti-rich PZT capacitors changes from positive to negative as increasing bias voltage, which may be due to the increasing leakage current and charge trapping at high voltages. A memory window of 1.7 V is measured for PZT(0/100) capacitors at $\pm 5$ V bias voltage, indicating a good material quality for Ti-rich PZT formed at 650°C. Besides, the larger memory window at $x = 0$ may be due to the smaller dielectric constant ($k$) that may cause a larger electric field drop in PZT than that in the $Al_2O_3$ dielectric.[8] Additionally, other reasons may be the larger grain size of Ti-rich PZT and that it has the same tetragonal unit cell as that of the bottom seeding layer. In contrast, only a negative threshold voltage shift is found for Zr-rich PZT capacitors. However, a similar trend of increasing memory window with increasing write voltages also occurs in this case, which depicts that the charge injection dominates the memory effect at high voltages regardless of the different composition of PZT capacitors.

We have summarized the composition dependence of PZT on threshold voltage shift, and the result is shown in Fig. 6. The horizontal axis from 0 to 1 represents the gradual composition change from PZT(0/100) to PZT(100/0). The similar trend of the larger threshold voltage shift with increasing write voltage is observed for all PZT capacitors due to the charge trapping contribution. However, from the memory device point of view, a desired large memory window is the key factor regardless of the effect from either the ferroelectric or charge trapping mechanism. Therefore, the PZT capacitors with composition close to that of the MPB would be the most suitable ferroelectric material for memory application, and a memory window as large as 9 V is obtained.

We have also measured the J-V characteristics to further study the memory characteristics. Figure 7a, b show the J-V characteristics

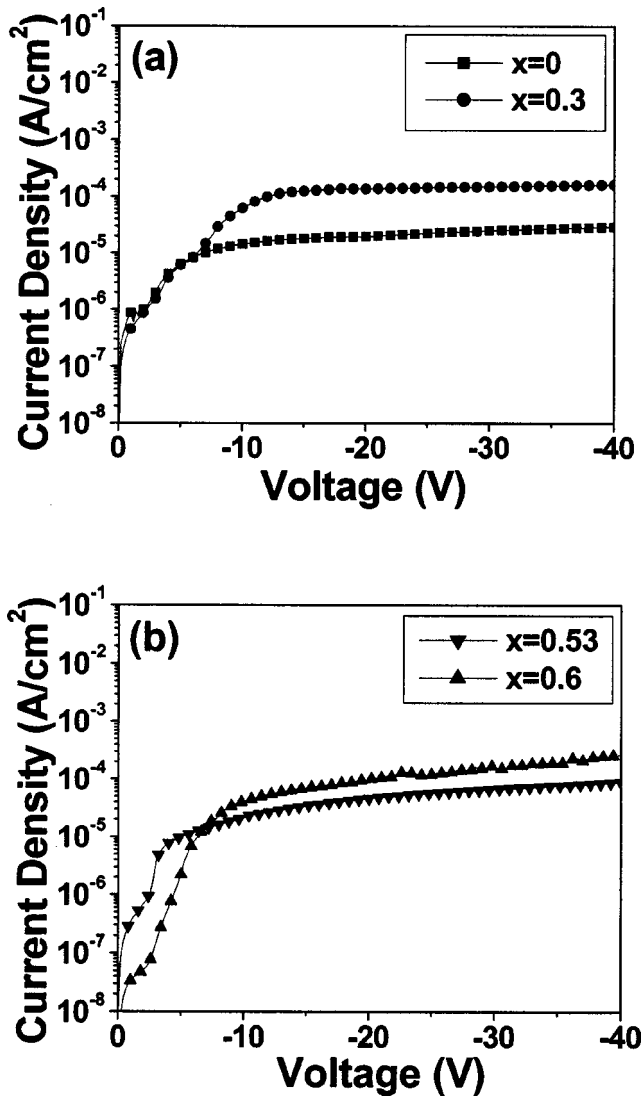


**Figure 7.** J-V characteristics of $Pb(Zr_xTi_{1-x})O_3/PbTiO_3/Al_2O_3/Si$ with (a) $x = 0$ and 0.3 and (b) $x = 0.53$ and 0.6.

of Ti-rich and Zr-rich PZT capacitors, respectively. No breakdown phenomenon occurs in the high voltage region up to $-20$ V for all four PZT capacitors, indicating that $Al_2O_3$ would be a suitable insulator material. The leakage current of PZT capacitor with $x = 0$ is $2.2 \times 10^{-6}$ A/cm$^2$ at $-5$ V, which is lower than that of other PZT capacitors. This result suggests that the difference in crystal systems between PZT films and the seeding layer may induce some interface traps that increase the leakage current.

Table I summarizes the characteristics of PZT capacitors with different Zr/Ti ratios. By the addition of a seeding layer on amorphous $Al_2O_3$ substrates, the transformation temperature are reduced. Furthermore, the relatively lower $k$ is desirable for Ti-rich PZT in a stacked gate dielectric because a larger electric field will drop on PZT, giving a larger memory window.

## Conclusions

We have compared the characteristics of PZT with different compositions on $Al_2O_3/Si$ and $PTO/Al_2O_3/Si$ substrates. A PTO seeding layer can lower the perovskite transformation temperatures and help the nucleation of the perovskite phase. However, Zr-rich PZT films on $PTO/Al_2O_3/Si$ substrates have dielectric constants that are lower than expected values due to the small grain size. In compari-

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**Table I. Characteristics of $Pb(Zr_xTi_{1-x})O_3/PbTiO_3/Al_2/O_3/Si$ capacitors.**

| $x$ | $\Delta V_T$ (V) at $\pm 5$ V | $\Delta V_T$ (V) at $\pm 10$ V | $k$ of stacked PZT films | Capacitance (pF) of gate dielectrics | Leakage current density at 165 kV/cm ($A/cm^2$) |
|---|---|---|---|---|---|
| 0 | 1.49 | 0.91 | 56.03 | 37 | $6.24 \times 10^{-6}$ |
| 0.3 | 0.40 | −1.50 | 336.89 | 146 | $6.12 \times 10^{-6}$ |
| 0.53 | −2.83 | −8.94 | 303.03 | 137 | $9.86 \times 10^{-6}$ |
| 0.6 | −0.78 | −5.83 | 225.06 | 113 | $2.20 \times 10^{-6}$ |

son with Zr-rich PZT/PTO/$Al_2O_3$/Si capacitors, the memory properties of Ti-rich PZT/PTO/$Al_2O_3$/Si capacitors are ferroelectric C-V hysteresis loops, and the lower leakage current is due to the lower dielectric constant of Ti-rich PZT and the same crystal system of Ti-rich PZT and PTO.

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