Device and Circuit Simulation of Anomalous DX Trap Effects in DCFL and SCFL HEMT Inverters

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***Abstract*—An integrated device and circuit analysis has been developed to evaluate the DX trap induced anomalous transient phenomena in DCFL and SCFL AlGaAs/GaAs HEMT inverters. The slow transient effect and the hysteretic characteristics of the input-output voltage transfer function in the inverters are simulated. The result shows that in comparison with the DCFL inverter, the DX trap effects are much improved in the SCFL inverter due to its particular operational principle.**

I. Introduction

THE EXISTENCE of DX traps in the Si-doped $Al_xGa_{1-x}As$ layer is widely known to be the origin of performance degradation in $Al_xGa_{1-x}As$/GaAs HEMT devices and circuits. The major detrimental effects include low temperature current collapse [1], low frequency noise [2], device threshold voltage shift [3] and remarkable "slow" current transients when a device is subject to a gate or drain voltage pulse [4]. Previous experimental study has also shown that deep traps may result in the hysteretic characteristics in the input-output voltage transfer function and a significant variation of the output pulse width in a string of direct coupled FET logic (DCFL) inverters [5]. Such phenomena may impose a severe limitation on full utilization of DCFL HEMT technology in high precision analog and certain digital applications.

Recently, GaAs source coupled FET logic (SCFL) has been proposed because of its tolerance to device threshold voltage and better driving capability [6], [7]. In this paper, we intend to evaluate the DX trap caused performance problems in the SCFL HEMT inverters and to make a comparison of the slow transient effects in the DCFL and SCFL inverters. Since the current HEMT SPICE models do not include the DX traps, a mixed level device and circuit simulation is proposed to combine circuit simulation with a complete description of DX trap physics in the HEMT devices.

II. Physical Model and Simulation Method

In our device model, a DX trap rate equation based on the Shockley-Read-Hall theory is included to study the slow transient phenomena.

$$\frac{\partial N_{dd}^+}{\partial t} = e_n\left(1 + \frac{n_s}{n_c}\right)(N_{dd} - N_{dd}^+) - c_n(n_c + n_s)N_{dd}^+ \quad (1)$$

where N_{dd} is the concentration of the DX centers, n_s is the electron concentration in the shallow donor states, and n_c is the electron concentration in the conduction band. c_n and e_n are the electron capture rate coefficient and the emission rate coefficient respectively. In this analysis, the DX rate equation is first evaluated at each time step to obtain the electron occupation of the DX traps in the AlGaAs layer. The distribution of the ionized DX centers is then used in the Poisson equation at each cross-section $x = x_i$ of a device.

$$\frac{\partial}{\partial y}\left[\epsilon(y)\frac{\partial}{\partial y}\phi(x_i, y)\right] = -q[N_{dd}^+(x_i, y) + N_{sd}^+(x_i, y) - n_c(x_i, y)] \quad (2)$$

where $\phi(x_i, y)$ is the electrostatic potential, $N_{sd}^+(x_i, y)$ is the ionized shallow donor concentration, x is in the channel direction and y is in the direction perpendicular to the channel. x_i denotes the ith cross section. In order to derive the two-dimensional electron gas (2DEG) distribution at each x_i, the quantization effects of the 2DEG in the GaAs quantum well are calculated from the Schrödinger equation:

$$\left[-\frac{\hbar^2}{2m^*}\frac{\partial^2}{\partial y^2} + V(x_i, y)\right]\psi_n(x_1, y) = e_n\psi_n(x_i, y) \quad (3)$$

and

$$V(x_i, y) = -q\phi(x_i, y) + V_h(y) + V_{ex}(x_i, y) \quad (4)$$

where $2\pi\hbar$ is the Planck constant, e_n is the nth eigen-state energy, ψ_n is the nth state wave-function, $V_h(y)$ is the heterojunction conduction band discontinuity and $V_{ex}(x_i, y)$ represents the local exchange-correlation potential [8]. The readers should be reminded that (2) and (3) have to be solved self-consistently at each x_i and at each time step. In other words, the equations are both time- and x-dependent. During the transient simulation, the initial condition of the DX traps varies at each grid point of a device and must be determined by the device bias history.

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The detailed mathematical description and the DX trap parameters used in the simulation can be found in [9].

In the calculation of the drain current, a two region Grebene–Ghandhi I-V model [10] is utilized to manifest the current transients as a gate pulse or a drain pulse is applied. Intrinsic device capacitances are not taken into account in the model since the intrinsic device delay is in the picosecond range while the DX traps have a time constant of several micro-seconds. The mutual interation of the gate pulse and the drain pulse incurred current transients [3], [4] is complicated in a circuit level. The mixed mode feature of this approach enables us to correlate the fundamental physical effects with the circuit behavior directly. In our calculation, connections between individual HEMT devices are treated as nodes of circuit equations governed by the Kirchhoff current and voltage laws. The device and circuit equations are grouped separately in the present simulation and are iteratively solved until all of them are satisfied.

III. Results and Discussions

The doping concentration in the $Al_xGa_{1-x}As$ layer of the simulated HEMT's is 1×10^{18} cm^{-3}. The aluminum composition x is 0.3. The Schottky-barrier height on $Al_{0.3}Ga_{0.7}As$ is 1.0 eV. Parasitic source and drain resistances are chosen to be 1.0 Ωmm. In a DCFL inverter, the AlGaAs thickness is 310 Å in an enhancement type FET (E-FET) and 470 Å in a depletion type FET (D-FET) including a 30 Å undoped spacer each. All of the HEMT's in the SCFL inverter have an AlGaAs thickness of 340 Å including a 30 Å spacer. Fig. 1 shows the device I-V characteristics in an E-FET under the steady-state and the fast transient conditions. The steady-state characteristics is obtained with the DX traps always in thermal equilibrium. The transient result is simulated with the DX traps held the same as their zero-bias ($V_{GS} = 0$, $V_{DS} = 0$) steady-state condition because the gate and the drain voltages vary rapidly. The channel electron concentration in the transient simulation is therefore different from that in the steady-state simulation under the same bias condition and so is the drain current. Another salient feature between the fast transient and the steady-state characteristics is the transconductance. Fig. 2 shows the steady-state transconductance and the high-frequency transconductance of the E-FET. The high-frequency transconductance is calculated by adding a small amount of the gate bias ΔV_{GS} and the drain current is simulated at $V_{GS} + \Delta V_{GS}$ with no variation of the DX trap condition. The result shows that the high-frequency transconductance can be significantly increased due to the presence of the DX traps especially at a large gate bias. This feature is consistent with the experimental result in [11]. Fig. 3 depicts the input and the output voltage waveforms in a DCFL inverter. In the inset of the figure is the DCFL circuit diagram. V_{DD} is 1.0 V. An output voltage undershoot is observed. The "slow" transient persists ~ 10 μs, which is about the DX trap time constant. The corre-

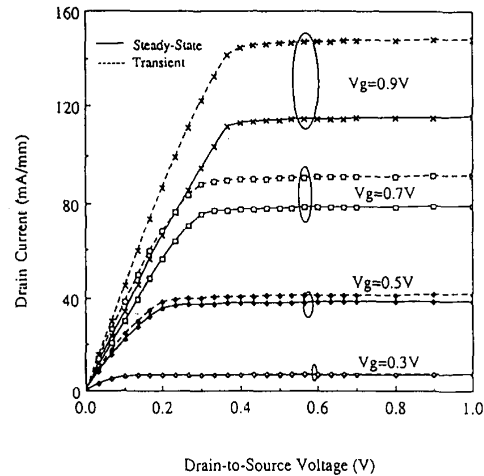

Fig. 1. The simulated steady-state and fast transient I–V characteristics in an E-FET.

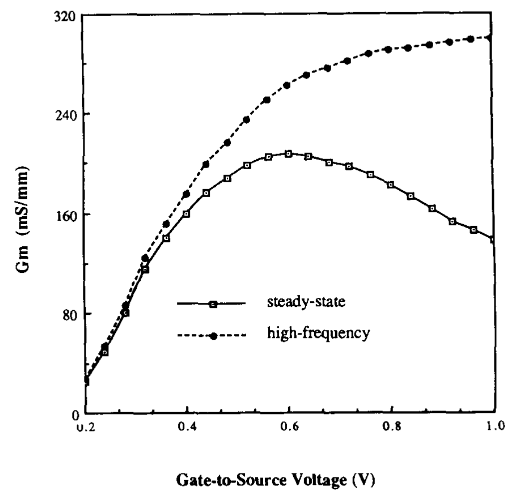

Fig. 2. The simulated steady-state and high-frequency transconductances plotted against a gate bias at $V_{DD} = 1.0$ V.

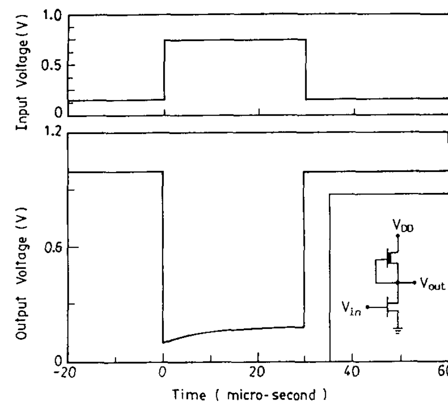

Fig. 3. The input and output voltage waveforms of a DCFL inverter are plotted against time. The DCFL inverter circuit diagram is drawn in the inset of the figure. $V_{DD} = 1.0$ V.

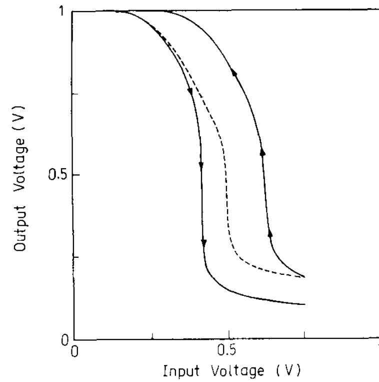

Fig. 4. Simulated input-output voltage transfer curve of a DCFL inverter. The dashed line represents the static voltage transfer curve.

sponding input-output voltage transfer curve (VTC) of the inverter is simulated in Fig. 4. The dashed line represents the static VTC. The hysteresis arises from the variation of the electron occupation of the DX traps during the pulse excitation. The opening of the hysteresis loop at the input voltage of 0.75 V accounts for the output voltage undershoot in Fig. 3. The shift of the logic threshold voltage in the simulated DCFL inverter is 0.19 V.

As a comparison, the transient characteristics of the output voltage in a SCFL inverter are shown in Fig. 5. No noticeable slow transient is observed. The circuit diagram of the SCFL inverter is shown in the inset of Fig. 5, which consists of a differential amplifier and two source-follower buffers with diode level shifters. In the simulation, $V_{CS} = -2.5$ V, $V_{SS} = -3.0$ V, $V_R = -1.65$ V, $R_1 = R_2 = 2.2$ kΩ. The VTC of the SCFL inverter is shown in Fig. 6. The amount of logic threshold voltage shift is only about 15 mV in comparison with 190 mV in the DCFL inverter. The inherent advantage of the SCFL inverters with respect to the immunity from the slow transient effects can be explained as follows; In a SCFL inverter, as the input switches from a low voltage to a high voltage, the transistor Q_3 serves as a current source with a current I_3 (referring to the inset of Fig. 5). Since Q_3 is always operated in the saturation region, *the electron occupation of the DX traps in the pinch-off region of Q_3 is insensitive to the change of the drain bias*. Consequently, the transient current ΔI_3 due to the variation of the DX traps is minimal during the switching. The voltage at the drain of Q_1 is approximately fixed at $-I_3R_1$ in the transient while the DX traps in Q_1 have not reached their equilibrium condition. Similarly, Q_5 and Q_7 are also always operated in the saturation region. The same argument applies to them as well. In other words, the DX trap conditions in Q_5 and Q_7 do not have a noticeable change during the switching. As a result, the output voltage of the SCFL inverter does not exhibit an undershoot. The voltage at the drain of Q_3, however, varies to react to the change of the DX traps occupation in Q_1 during the transient.

Since the DX trap concentration in the AlGaAs layer is

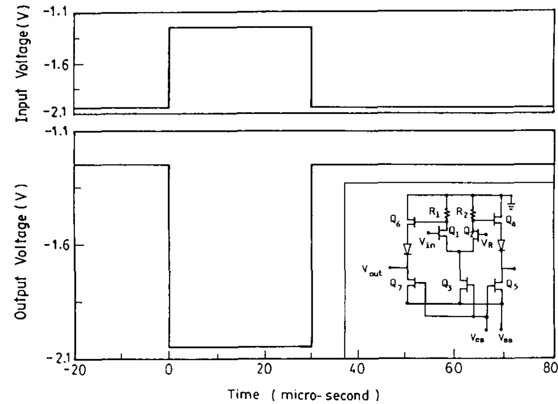

Fig. 5. The input and output voltage waveforms of a SCFL inverter are plotted against time. The SCFL inverter circuit diagram is shown in the inset of the figure. $V_{SS} = 3$ V, $V_{CS} = -2.5$ V, $V_R = -1.65$ V, $R_1 = R_2 = 2.2$ kΩ.

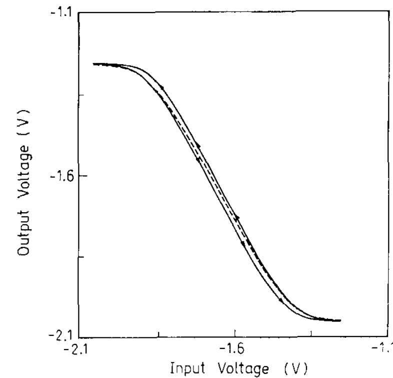

Fig. 6. Simulated input-output voltage transfer curve of a SCFL inverter. The dashed line represents the static voltage transfer curve.

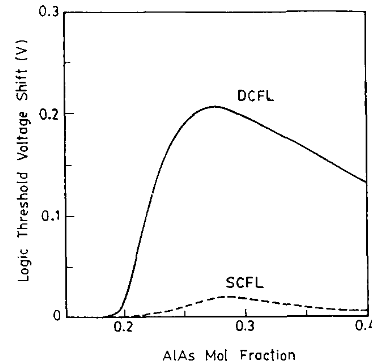

Fig. 7. Logic threshold voltage shift as a function of AlAs mol fraction in the DCFL and SCFL inverters.

related to aluminum composition, the dependence of the logic threshold voltage shift on aluminum composition x in the DCFL and SCFL inverters is shown in Fig. 7. The maximum voltage shift in the DCFL inverter is about 210 mV at $x = 0.28$ and the maximum value in the SCFL inverter is ten times lower. In order to study the influence

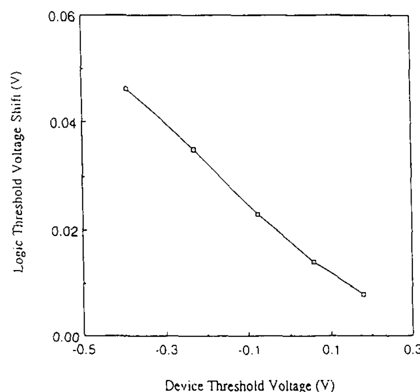

Fig. 8. Logic threshold voltage shift as a function of a device threshold voltage in a SCFL inverter.

of the FET characteristics on the slow transient effects in the SCFL inverters, we calculate the logic threshold voltage shift as a function of a device threshold voltage in Fig. 8 for the same voltage swing. The result indicates that the logic threshold voltage shift decreases with an increasing device threshold voltage. The reason is that a smaller device threshold voltage corresponds to a wider AlGaAs layer, which contains more DX traps. Therefore, smaller threshold voltage FET's are more susceptible to the DX trap effects. It should be emphasized that even in the worst case in Fig. 8 the logic threshold voltage shift of the SCFL is still significantly lower than that of a DCFL inverter.

As a conclusion, our study shows that the SCFL inverter is inherently immune from the DX trap incurred slow transient problems due to its particular operational principle. The pulse width variation observed in a string of the DCFL inverters is expected to be much improved in the SCFL circuits even with aluminum composition $x \geq 0.2$. The feasibility of choosing a higher aluminum content in the SCFL lends itself an advantage to achieve better quantum confinement of two-dimensional electrons and thus better device performance.

Acknowledgment

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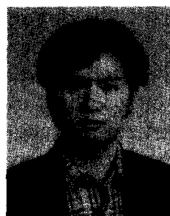

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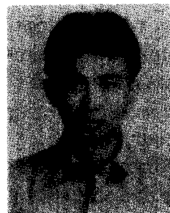

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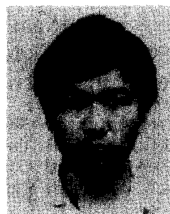

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