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Electrical and structural characteristics of $PbTiO_3$ thin films with ultra-thin Al_2O_3 buffer layers

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Abstract

Polycrystalline $PbTiO_3$ thin films have been prepared on Si substrates with ultra-thin SiO_2 and Al_2O_3 buffer layers by chemical solution deposition, respectively. Although capacitance–voltage characteristics show hysteresis loops in both cases, the memory window of $PbTiO_3/Al_2O_3$ stacked dielectric is 3.3 V larger than that on SiO_2. In addition, well-behaved capacitance–voltage characteristics are only obtained in $PbTiO_3/Al_2O_3$ and the $PbTiO_3$ films on Al_2O_3 have the dielectric constant of 116 larger than 42 of $PbTiO_3$ films on SiO_2. The leakage current density of $PbTiO_3/Al_2O_3$ dielectric is 1.3×10^{-7} A cm^{-2} at −2.5 V, which is low enough for deep sub-μm application.
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1. Introduction

Recently, ferroelectric devices have attracted much attention for future generation memory application [1–4]. In fact, one transistor and one ferroelectric capacitor (1T1C) structure has already been used for memory product. However, in order to minimize the device area, ferroelectric thin films have to be directly integrated to MOSFET to form a new ferroelectric MOSFET structure [5,6]. Although this 1T memory has strong advantages, the process integration issues are very difficult. The basic challenge is due to the reaction of ferroelectric material with Si that would form an interfacial layer of a non-ferroelectric pyrochlore phase even at temperatures as low as 500 °C [7]. The formation of this unwanted pyrochlore phase would lower the yield and damage the performance of devices seriously. To overcome this difficulty, many kinds of materials such as Y_2O_3 [8], CeO_2 [9], MgO [10], and $SrTiO_3$ [11] have been investigated as the insulating buffer layer between ferroelectric material and Si. However, these insulating buffer layers still have other integration concern. It is obvious that thinner insulating buffer layers and larger capacitance are required for next generation high performance and low voltage operation. However, little research has been available with thin insulating buffer layers. Although it was reported that SiO_2 with thickness lower than 10 nm can be used between Pb(Zr, Ti)O_3 films and Si by pulsed laser deposition (PLD) [12], this equivalent oxide thickness is still too large for advanced CMOS integration [13]. In this paper, we have developed the ultra-thin Al_2O_3 films with the thickness of 4 nm as the buffer layers [14]. This ultra-thin insulator films could prevent the formation of interfacial pyrochlore phase and further decrease the working voltage of this device. Good capacitance–voltage characteristics, low leakage current, and large memory window are simultaneously obtained for $PbTiO_3$ (PTO)/Al_2O_3 gate dielectric.

2. Experimental procedure

Four-inch, p-type (1 0 0) Si wafers were used in this work with a resistivity of 10 Ω cm. A HF-vapor passivation [14,15] was used to suppress the native oxide formation before other treatment. In comparison to Al_2O_3, conventional thermal SiO_2 grown on Si of 4 nm was grown in oxygen ambient and annealed at 900 °C for 5 min. On the other hand, after in situ native oxide desorption, amorphous Al layer was thermally evaporated on wafers. The Al layer was oxidized at a temperature of 400 °C for 2 h to form 4 nm Al_2O_3 and finally annealed at 900 °C for 30 min in nitrogen ambient. Before ferroelectric thin film deposition, the chemical solutions have to be synthesized. Following the method [16,17], lead acetate trihydrate and titanium isopropoxide were used as

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precursors and dissolved in the acetic acid and methanol, respectively. These precursor solutions were then mixed at any proportion to obtain the desired $PbTiO_3$ (PT) compositions. The PT thin film were fabricated on ultra-thin SiO_2 or Al_2O_3 buffered Si by multiple spin coating at 4000 rpm for 30 s. Between each coating, the wet films were dried at 150 °C to drive off the solvent and then pyrolyzed at 350 °C for several minutes. After multiple coating, the films were directly annealed at 550 °C in air for 1 h. We used X-ray diffraction (XRD) to determine the phase and the crystallinity of ferroelectric thin films. The surface morphology and the thickness of ferroelectric films were observed by scanning electron microscopy (SEM). For electrical properties measurement, gold was deposited as upper electrode with area of 5×10^{-4} cm^2 and Al contact was made at the bake side of Si substrates. Capacitance–voltage (*C–V*) characteristics were measured for ±10 V sweep voltages. Moreover, current density–voltage (*J–V*) characteristics were measured from 0 to −20 V to check the stacked gate dielectric quality.

3. Results and discussion

We have first checked the high frequency *C–V* characteristics of 4 nm Al_2O_3 gate dielectric. As shown in Fig. 1, good *C–V* characteristic at 1 MHz is observed and dielectric constant of about 9 is obtained from the measured capacitance value that is two times larger than that of SiO_2. An equivalent oxide thickness of 1.7 nm is obtained for 4 nm Al_2O_3 that could be used for sub-μm technology generation. The good gate dielectric property would be further considered to integrate PTO thin films on Al_2O_3 gate dielectric.

Fig. 2(a) and (b) show the XRD patterns of PTO films deposited on 4 nm SiO_2 and Al_2O_3 gate dielectrics on Si, respectively. As shown in Fig. 2(a), the relative intensity of (1 0 0) peak is much higher than other directions so that PTO films grown on SiO_2 are (1 0 0)-oriented. Fig. 2(b) displays XRD pattern of PTO films on ultra-thin 4 nm Al_2O_3. The result reveals that PTO films on Al_2O_3 are also polycrystalline but the XRD pattern is similar to that of bulk materials without preferred orientation. According to the results of Fig. 2(a) and (b), both PTO films have stable ferroelectric perovskite phase rather than undesirable non-ferroelectric pyrochlore phase although the buffer layer thickness is just 4 nm.

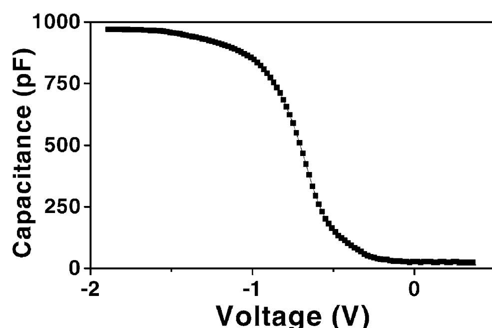

Fig. 1. *C–V* characteristics of 4 nm Al_2O_3 at 1 MHz.

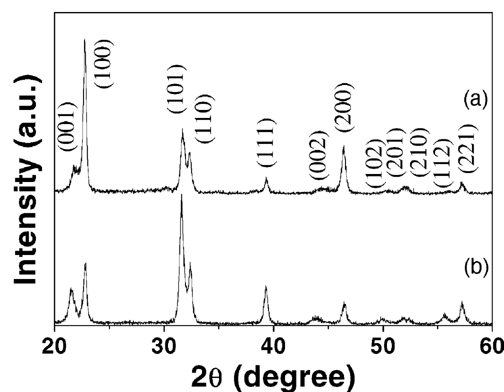

Fig. 2. XRD patterns of 250 nm $PbTiO_3$ on: (a) SiO_2 and (b) Al_2O_3 buffered Si substrates.

We have further used SEM to observe the microstructure of PTO films. The thickness of PTO films is determined to be 250 nm by the SEM cross-sectional images. The surface morphology images are shown in Fig. 3(a) and (b) for PTO films on SiO_2 and Al_2O_3 gate dielectrics, respectively. As shown in Fig. 3(a), the PTO films on SiO_2 are polycrystalline and have smooth surface without cracks. Additionally, polycrystalline structure and continuous films are also observed

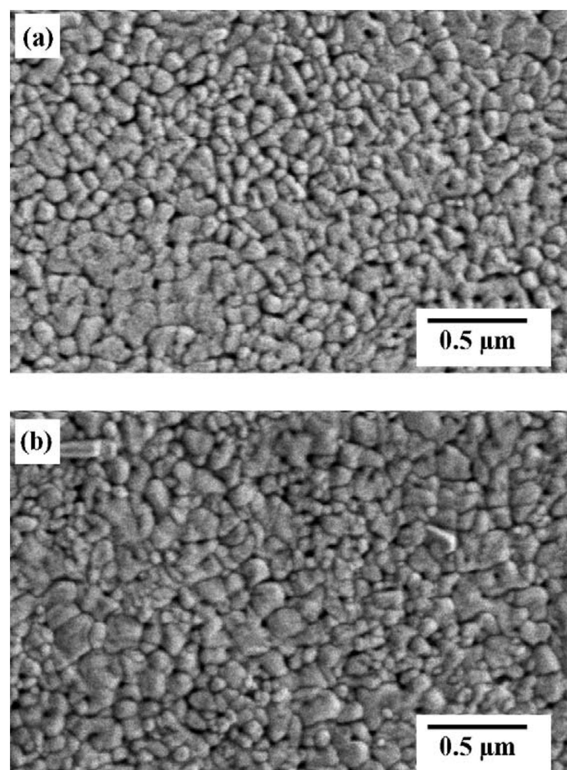

Fig. 3. SEM pictures of 250 nm $PbTiO_3$ on: (a) SiO_2 and (b) Al_2O_3 buffered Si substrates.

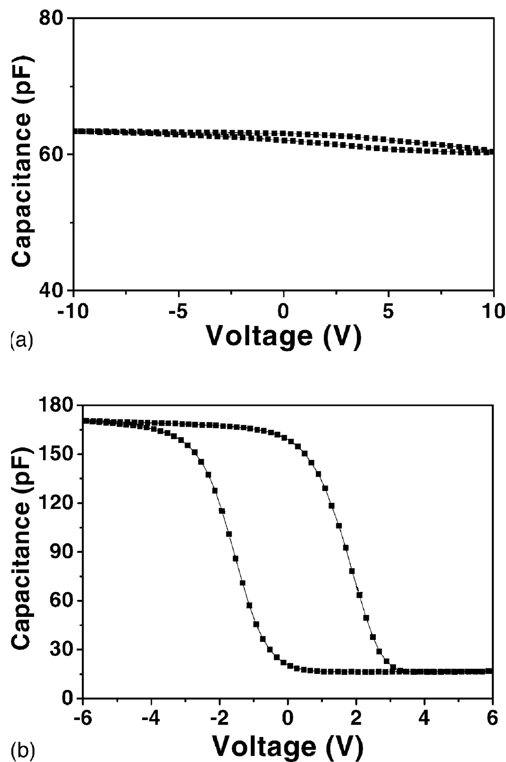

Fig. 4. *C–V* characteristics of 250 nm $PbTiO_3$ on: (a) SiO_2 and (b) Al_2O_3 buffered Si substrates at 1 MHz.

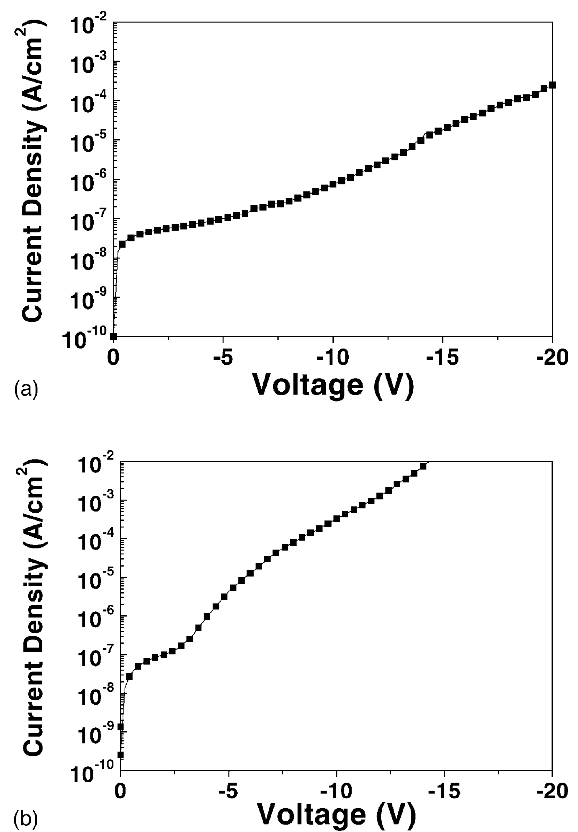

Fig. 5. *J–V* characteristics of 250 nm $PbTiO_3$ on: (a) SiO_2 and (b) Al_2O_3 buffered Si substrates.

for PTO films on Al_2O_3 shown in Fig. 3(b). The grain size and distribution in both cases are similar that would not be affected by the different buffer layers. The dense polycrystalline microstructure in both cases suggests that PTO films could be integrated on Si with either ultra-thin SiO_2 or Al_2O_3 buffer layers.

The electrical properties of PTO films are further examined by *C–V* measurement. Fig. 4(a) and (b) show the *C–V* characteristics of PTO/SiO_2 and PTO/Al_2O_3 stacked dielectrics, respectively. The sweep voltages in this measurement change between +10 and −10 V back and forth at the frequency of 1 MHz. For PTO/SiO_2 stacked dielectric, as shown in Fig. 4(a), an accumulation capacitance of only 64 pF is measured. Besides, the transition between accumulation and depletion regions is elongated and distorted from the typical high frequency *C–V* curves. The obvious distortion in *C–V* curves indicates that more interface trap density was generated in the Au/PTO/SiO_2/Si capacitor. In other words, the PTO probably tends to react with SiO_2 to form a non-ferroelectric pyrochlore phase at PTO/SiO_2 interface even at temperatures as low as 550 °C [7]. The dielectric constant of PTO films on SiO_2 is about 42, which is relatively low as compared to the data reported in literature [18]. This result suggests that different buffer layers would affect the electrical properties of the ferroelectric films. In contrast, as shown in Fig. 4(b), PTO films on Al_2O_3 have the higher capacitance value of 170 pF and the higher dielectric constant of 116. In addition to the well-behaved *C–V* curves and the higher dielectric constant of PTO films, the larger memory window of 3.3 V is also obtained for PTO/Al_2O_3 dielectric. These excellent results indicate that PTO films could be integrated on Si if using high *k* Al_2O_3 rather than SiO_2 gate dielectric as the buffer layer.

Both *J–V* characteristics of PTO/SiO_2 and PTO/Al_2O_3 are shown in Fig. 5(a) and (b), respectively. Typical Fowler–Nordheim (F–N) tunneling currents at high voltage region are observed in both cases and it indicates the good quality of both stacked dielectrics on Si with little dielectric defect-induced leakage current. The current density of 5.6×10^{-8} and 1.3×10^{-7} A cm^{-2} are measured at an applied voltage of −2.5 V for PTO/SiO_2 and PTO/Al_2O_3 and they are acceptable for gate dielectric application. Because the grain sizes in both PTO films are very similar, the larger leakage current in PTO/Al_2O_3 is not due to PTO structure itself but due to the slightly inferior quality of Al_2O_3 gate dielectric to thermal SiO_2. However, the leakage current is still low enough for advanced deep sub-μm application.

4. Conclusions

In conclusion, we have studied the characteristics of ferroelectric PTO thin films on both ultra-thin SiO_2 and Al_2O_3 gate dielectrics buffered Si. The PTO on Al_2O_3 has much

better memory performance than that on thermal SiO_2. The excellent memory characteristics are evidenced from the large 3.3 V threshold voltage difference, well-behaved *C–V* curves, and small leakage current.

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References

[1] S.L. Miller, P.J. MacWhorter, J. Appl. Phys. 72 (1992) 5999.
[2] A. Chin, M.Y. Yang, S.B. Chen, C.L. Sun, S.Y. Chen, in: Proceedings of the 59th Device Research Conf. Dig., Notre Dame, IN, USA, 2001, p. 18.
[3] N.W. Jang, Y.J. Song, H.H. Kim, D.J. Jung, B.J. Koo, S.Y. Lee, S.H. Joo, K.M. Lee, K. Kim, in: Proceedings of the Symposium on VLSI Technology, Honolulu, HI, USA, 2000, p. 34.
[4] A. Chin, M.Y. Yang, C.L. Sun, S.Y. Chen, IEEE Electron Device Lett. 22 (2001) 336.
[5] M.Y. Yang, S.B. Chen, A. Chin, C.L. Sun, B.C. Lan, S.Y. Chen, in: Tech. Dig.-Int. Electron Devices Meet., Washington, DC, USA, 2001, p. 36_03.1.
[6] C.L. Sun, S.Y. Chen, M.Y. Yang, A. Chin, J. Electrochem. Soc. 148 (2001) F203.
[7] Y. Shichi, S. Tanimoto, T. Goto, K. Kuroiwa, Y. Tarui, Jpn. J. Appl. Phys. 33 (1994) 5172.
[8] B.E. Park, S. Shouriki, E. Tokumitsu, H. Ishiwara, Jpn. J. Appl. Phys. 37 (1998) 5145.
[9] B.E. Park, I. Sakai, E. Tokumitsu, H. Ishiwara, Appl. Surf. Sci. 117 (1997) 423.
[10] J. Senzaki, O. Mitsunaga, T. Uhcida, T. Ueno, K. Kuroiwa, Jpn. J. Appl. Phys. 35 (1996) 4195.
[11] E. Tokumitsu, R.I. Nakamura, H. Ishiwara, IEEE Electron Device Lett. 18 (1997) 160.
[12] Y. Lin, B.R. Zhao, H.B. Peng, B. Xu, H. Chen, F. Wu, H.J. Tao, Z.X. Zhao, J.S. Chen, Appl. Phys. Lett. 73 (1998) 2781.
[13] A. Chin, C.C. Liao, C.H. Lu, W.J. Chen, C. Tsai, in: Proceedings of the Symposium on VLSI Technology, Kyoto, Japan, 1999, p. 135.
[14] A. Chin, W.J. Chen, T. Chang, R.H. Kao, B.C. Lin, C. Tsai, J.C.-M. Huang, IEEE Electron Device Lett. 18 (1997) 417.
[15] Y.H. Wu, W.J. Chen, S.L. Chang, A. Chin, S. Gwo, C. Tsai, IEEE Electron Device Lett. 20 (1999) 200.
[16] S.Y. Chen, I.W. Chen, J. Am. Ceram. Soc. 81 (1998) 97.
[17] S.Y. Chen, C.L. Sun, J. Appl. Phys. 90 (2001) 2970.
[18] E. Sato, Y. Huang, M. Kosec, A. Bell, N. Setter, Appl. Phys. Lett. 65 (1994) 2678.